CoolSET™ F3R80
ICE3AR1080VJZ

Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS™ and Startup cell (input OVP & frequency jitter) in DIP-7

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Major changes since previous revision

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20 Jan 2014	2.0		Release of first version

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Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS™ and Startup cell (input OVP & frequency jitter) in DIP-7

Product Highlights

- **800V avalanche rugged CoolMOS™ with startup cell**
- **Active Burst Mode to reach the lowest Standby Power <100mW**
- **Selectable entry and exit burst mode level**
- **Adjustable blanking Window for high load jumps**
- **Frequency jitter and soft driving for low EMI**
- **Adjustable input OVP**
- **Auto Restart protection for over load, over temperature and over voltage**
- **Low Operating temperature down to -40°C**
- **Pb-free lead plating, halogen free mold compound, RoHS compliant**

PG-DIP7

Features

- 800V avalanche rugged CoolMOS™ with Startup Cell
- Active Burst Mode for lowest Standby Power
- Selectable entry and exit burst mode level
- 100kHz internally fixed switching frequency with jittering feature
- Auto Restart Protection for Over load, Open Loop, VCC Under voltage & Over voltage and Over temperature
- Over temperature protection with 50°C hysteresis
- Built-in 10ms Soft Start
- Built-in 20ms and extendable blanking time for short duration peak power
- Propagation delay compensation for both maximum load and burst mode
- Adjustable input OVP
- Overall tolerance of Current Limiting < ±5%
- BiCMOS technology for low power consumption and wide VCC voltage range
- Soft gate drive with 50Ω turn on resistor

Description

The ICE3AR1080VJZ is a modified version of ICE3ARxx80JZ (CoolSET™-F3R 800V) in DIP-7 package. It adds in the input OVP feature but removes the brownout feature and external protection enable feature. In summary, the ICE3AR1080VJZ is a device running at 100kHz, implemented with input OVP feature, installed with 800V MOSFET with startup cell and housed in DIP-7 package. It provides good voltage margin of MOSFET, lowest standby power, selectable burst level, reduced output ripple during burst mode, robust protection with input OVP feature, accurate maximum power control for both maximum power and burst power, low EMI with frequency jittering and soft gate drive, built-in and flexible protections, etc.

Applications

- Adapter/Charger
- Blue Ray/DVD player, Set-top Box, Digital Photo Frame
- Auxiliary power supply for Server, PC, Printer, TV, Home theater/Audio System, White Goods, etc

Figure 1: Typical Application

Type	Package	Marking	V_{DS}	F_{OSC}	R_{DSon} 1)	230VAC ±15% 2)	85-265 VAC 2)
ICE3AR1080VJZ	PG-DIP-7	3AR1080VJZ	800V	100kHz	1.0	71W	45W

1) typ @ T=25°C

2) Calculated maximum input power rating at T_a=50°C, Ti=125°C and without copper area as heat sink.

1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DIP-7

Pin	Symbol	Function
1	BV	extended Blanking time & input OVP
2	FBB	Feedback & Burst entry/exit control
3	CS	Current Sense/ 800V CoolMOS™ Source
4	n.c.	not connected
5	Drain	800V CoolMOS™ Drain
6	-	(no pin)
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

Figure 2: Pin configuration PG-DIP-7(top view)

1.2 Pin Functionality

BV (extended Blanking time & input OVP)

The BV pin combines the functions of input OVP and extendable blanking time for over load protection. The input OVP feature is to stop the switching pulse when the input line voltage is higher than the V_{OVP_ref} after the resistor divider (Refer to Figure 3). The extendable blanking time function is to extend the built-in 20 ms blanking time for over load protection by adding an external capacitor to ground.

FBB (Feedback & Burst entry control)

The FBB pin combines the feedback function and the burst entry/exit control. The regulation information is provided by the FBB pin to the internal Protection Unit and the internal PWM-Comparator to control the duty cycle. The FBB-signal is the only control signal in case of light load at the Active Burst Mode. The burst entry/ exit control provides an access to select the entry/exit burst mode level.

CS (Current Sense)

The Current Sense pin senses the voltage developed on the shunt resistor inserted in the source of the integrated CoolMOS™. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM comparator to realize the Current Mode.

Drain (Drain of integrated CoolMOS™)

Pin Drain is the connection to the Drain of the integrated CoolMOS™.

VCC (Power Supply)

The VCC pin is the positive supply of the IC. The operating range is between 10.5V and 25V.

GND (Ground)

The GND pin is the ground of the controller.

2 Representative Block Diagram

Figure 3: **Representative Block Diagram**

3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 Introduction

ICE3AR1080VJZ input OVP and jitter 800V version is the modified version of the ICE3ARxx80JZ. It is particular good for high voltage margin low power SMPS application such as white goods, auxiliary power supply for PC and server. The major characteristics are that the IC is developed with 800V CoolMOS™ with start up cell, having adjustable input OVP feature, running at 100kHz switching frequency and packed in DIP-7 package.

The familiar features are BiCMOS technology to reduce power consumption and increase the Vcc voltage range, cycle by cycle current mode control, built-in 10ms soft start to reduce the stress of switching elements during start up, built-in 20ms and extended blanking time for short period of peak power before entering protection, active burst mode for lowest standby power and propagation delay compensation for close power limit between high line and low line, frequency jittering for low EMI performance, the built-in auto-restart mode protections for open loop, over load, Vcc OVP, Vcc under voltage, etc.

Besides, it also includes narrowing the feedback voltage swing from 0.5V to 0.3V during burst mode so that the output voltage ripple can be reduced by 40%, reduction of the fast voltage fall time of the MOSFET by increasing the soft turn-on time and addition of 50Ω turn-on resistor, faster start up time by optimizing the Vcc capacitor to 10uF and over temperature protection with 50°C hysteresis.

Furthermore, it includes adjustable input OVP to suppress the abnormal input stress to damage the device, selectable entry and exit burst mode for smaller entry/exit power to burst mode or even no burst mode is possible and the propagation delay compensation for burst mode so that the entry/exit burst mode power is close between high line and low line.

In summary, the ICE3AR1080VJZ provides good voltage margin of MOSFET, lowest standby power, flexible burst level, reduced output ripple during burst mode, robust for abnormal input stress with input OVP feature, accurate power limit for both maximum power and burst power, low EMI with frequency jittering and soft gate drive, built-in and flexible protections, etc. Therefore, ICE3AR1080VJZ is a complete solution for the low power SMPS application typically for white goods.

3.2 Power Management

Figure 4: Power Management

The Undervoltage Lockout monitors the external supply voltage $V_{VCC.}$ When the SMPS is plugged to the main line the internal Startup Cell is biased and starts to charge the external capacitor C_{VCC} which is connected to the VCC pin. This

VCC charge current is controlled to 0.9mA by the Startup Cell. When the V_{VCC} exceeds the on-threshold V_{CCon}=17V the bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the Drain voltage. To avoid uncontrolled ringing at switch-on, a hysteresis start up voltage is implemented. The switch-off of the controller can only take place when V_{VCC} falls below 10.5V after normal operation was entered. The maximum current consumption before the controller is activated is about 200µA.

When V_{VCC} falls below the off-threshold V_{CCoff}=10.5V, the bias circuit is switched off and the soft start counter is reset. Thus it ensures that at every startup cycle the soft start starts at zero.

The internal bias circuit is switched off if Auto Restart Mode is entered. The current consumption is then reduced to 320µA.

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require re-cycling the AC line.

When Active Burst Mode is entered, the internal Bias is switched off most of the time but the Voltage Reference is kept alive in order to reduce the current consumption below 620µA.

3.3 Improved Current Mode

Figure 5: Current Mode

Current Mode means the duty cycle is controlled by the slope of the primary current. This is done by comparing the FBB signal with the amplified current sense signal.

Figure 6: Pulse Width Modulation

In case the amplified current sense signal exceeds the FBB signal the on-time t_{on} of the driver is finished by resetting the PWM-Latch (Figure 6).

The primary current is sensed by the external series resistor R_{Sense} inserted in the source of the integrated CoolMOS™. By means of Current Mode regulation, the secondary output voltage is insensitive to the line variations. The current waveform slope will change with the line variation, which controls the duty cycle.

The external R_{Sense} allows an individual adjustment of the maximum source current of the integrated CoolMOS™.

To improve the Current Mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch T2, the voltage source V1 and a resistor R1 (see Figure 7). Every time the oscillator shuts down for maximum duty cycle limitation the switch T2 is closed by V_{OSC}. When the oscillator triggers the Gate Driver, T2 is opened so that the voltage ramp can start.

Figure 7: Improved Current Mode

In case of light load the amplified current ramp is too small to ensure a stable regulation. In that case the Voltage Ramp is a well defined signal for the comparison with the FBB-signal. The duty cycle is then controlled by the slope of the Voltage Ramp.

By means of the time delay circuit which is triggered by the inverted V_{OSC} signal, the Gate Driver is switched-off until it reaches approximately 156ns delay time (Figure 8). It allows the duty cycle to be reduced continuously till 0% by decreasing V_{FBB} below that threshold.

Figure 8: Light Load Conditions

3.3.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor R_{Sense} connected to pin CS. R_{Sense} converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.25 by PWM OP. The output of the PWM-OP is connected to the voltage source V_1. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM-Comparator C8 and the Soft-Start-Comparator (Figure 9).

3.3.2 PWM-Comparator

The PWM-Comparator compares the sensed current signal of the integrated CoolMOS™ with the feedback signal V_{FBB} (Figure 9). V_{FBB} is created by an external optocoupler or external transistor in combination with the internal pull-up resistor R_{FB} and provides the load information of the feedback circuitry. When the amplified current signal of the integrated CoolMOS™ exceeds the signal V_{FBB} the PWM-Comparator switches off the Gate Driver.

Figure 9: PWM Controlling

3.4 Startup Phase

Figure 10: Soft Start

In the Startup Phase, the IC provides a Soft Start period to control the primary current by means of a duty cycle limitation. The Soft Start function is a built-in function and it is controlled by an internal counter.

Figure 11: Soft Start Phase

When the V_{VCC} exceeds the on-threshold voltage, the IC starts the Soft Start mode (Figure 10).
The function is realized by an internal Soft Start resistor, a current sink and a counter. And the amplitude of the current sink is controlled by the counter (Figure 12).

Figure 12: Soft Start Circuit

After the IC is switched on, the V_{SoftS} voltage is controlled such that the voltage is increased step-wisely (32 steps) with the increase of the counts. The Soft Start counter would send a signal to the current sink control in every 300µs such that the current sink decrease gradually and the duty ratio of the gate drive increases gradually. The Soft Start will be finished in 10ms ($t_{Soft\text{-}Start}$) after the IC is switched on. At the end of the Soft Start period, the current sink is switched off.
Within the soft start period, the duty cycle is increasing from zero to maximum gradually (see Figure 13).

Figure 13: Gate drive signal under Soft-Start Phase

In addition to Start-Up, Soft-Start is also activated at each restart attempt during Auto Restart.

Figure 14: Start Up Phase

The Start-Up time $t_{Start-Up}$ before the converter output voltage V_{OUT} is settled, must be shorter than the Soft-Start Phase $t_{Soft-Start}$ (Figure 14). By means of Soft-Start there is an effective minimization of current and voltage stresses on the integrated CoolMOS™, the clamp circuit and the output rectifier and it helps to prevent saturation of the transformer during Start-Up.

3.5 PWM Section

Figure 15: PWM Section Block

3.5.1 Oscillator

The oscillator generates a fixed frequency of 100kHz with frequency jittering of ±4% (which is ±4KHz) at a jittering period of 4ms.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max}=0.75.

Once the Soft Start period is over and when the IC goes into normal operating mode, the switching frequency of the clock is varied by the control signal from the Soft Start block. Then the switching frequency is varied in range of 100kHz ± 4KHz at period of 4ms.

3.5.2 PWM-Latch FF1

The output of the oscillator block provides continuous pulse to the PWM-Latch which turns on/off the integrated CoolMOS™. After the PWM-Latch is set, it is reset by the PWM comparator, the Soft Start comparator or the Current -Limit comparator. When it is in reset mode, the output of the driver is shut down immediately.

3.5.3 Gate Driver

Figure 16: Gate Driver

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the integrated CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (Figure 17) and adding a 50Ω gate turn on resistor (Figure 15). Thus the leading switch on spike is minimized.

Figure 17: Gate Rising Slope

Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.
During power up, when VCC is below the undervoltage lockout threshold $V_{VCCoff,}$ the output of the Gate Driver is set to low in order to disable power transfer to the secondary side.

3.6 Current Limiting

Figure 18: Current Limiting Block

There is a cycle by cycle peak current limiting operation realized by the Current-Limit comparator C10. The source current of the integrated CoolMOS™ is sensed via an external sense resistor $R_{Sense.}$ By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense} which is fed into the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage $V_{csth,}$ the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1.

A Propagation Delay Compensation is added to support the immediate shut down of the integrated CoolMOS™ with very short propagation delay. Thus the influence of the AC input voltage on the maximum output power can be reduced to minimal. This compensation applies to both the peak load and burst mode.

In order to prevent the current limit from distortions caused by leading edge spikes, a Leading Edge Blanking (LEB) is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the Gate G10 if Active Burst Mode is entered. When it is activated, the current limiting is reduced to V_{csth_burst}. This voltage level determines the maximum power level in Active Burst Mode.

3.6.1 Leading Edge Blanking

Figure 19: Leading Edge Blanking

Whenever the integrated CoolMOS™ is switched on, a leading edge spike is generated due to the primary-side capacitances and reverse recovery time of the secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220ns for normal load and t_{LEB} = 180ns for burst mode.

3.6.2 Propagation Delay Compensation (patented)

In case of overcurrent detection, there is always propagation delay to switch off the integrated CoolMOS™. An overshoot of the peak current I_{peak} is induced to the delay, which depends on the ratio of dI/ dt of the peak current (Figure 20).

Figure 20: Current Limiting

The overshoot of Signal2 is larger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{csth} and the switching off of the integrated CoolMOS™ is compensated over temperature within a wide input range. Current Limiting is then very accurate.

For example, I_{peak} = 0.5A with R_{Sense} = 2. The current sense threshold is set to a static voltage level V_{csth}=1V without Propagation Delay Compensation. A current ramp of dI/dt = 0.4A/µs, or dV_{Sense}/dt = 0.8V/µs, and a propagation delay time of $t_{Propagation\ Delay}$ =180ns leads to an I_{peak} overshoot of 14.4%. With the propagation delay compensation, the overshoot is only around 2% (Figure 21).

Figure 21: Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (Figure 22). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

Figure 22: Dynamic Voltage Threshold Vcsth

Similarly, the same concept of propagation delay compensation is also implemented in burst mode with reduced level, V_{csth_burst} (Figure 18). With this implementation, the entry and exit burst mode power can be very close between low line and high line input voltage.

3.7 Control Unit

The Control Unit contains the functions for Active Burst Mode and Auto Restart Mode. The Active Burst Mode and the Auto Restart Mode both have 20ms internal blanking time. For the over load Auto Restart Mode, the 20ms blanking time can be further extended by adding an external capacitor at BV pin. With the blanking time, the IC avoids entering into those two modes accidentally. That buffer time is very useful for the application which works in short duration of peak power occasionally.

3.7.1 Basic and Extendable Blanking Mode

Figure 23: Basic and Extendable Blanking Mode

There are 2 kinds of Blanking mode; basic mode and the extendable mode. The basic mode is a built-in 20ms blanking time while the extendable mode can extend this blanking time by connecting an external capacitor to the BV pin. For the extendable mode, the gate G5 remains blocked even though the 20ms blanking time is reached. After reaching the 20ms blanking time the counter is activated and the switch S1 is turned on to charge the voltage of BV pin by the constant current source, I_{chg_EB}. When the voltage of BV pin hits 4.5V, which is sensed by

comparator C11, the counter will increase the counter by 1. Then it switches off the switch S1 and turns on the switch S2. The voltage at BV pin will be discharged through a 500Ω resistor. When the voltage drops to 0.9V which is sensed by comparator C3, the switch S2 will be turned off and the switch S1 will be turned on. Then the constant current I_{chg_EB} will charge the C_{BK} capacitor again. When the voltage at BV hits 4.5V which is sensed by comparator C11, the counter will increase the count to 2. The process repeats until it reaches total count of 256 (Figure 24). Then the counter will release a high output signal. When the AND gate G5 detects both high signals at the inputs, it will activate the 30µs spike blanking circuit and finally the auto-restart mode will be activated.

Figure 24: Waveform at extended blanking time

For example, if C_{BK}=0.1µF, I_{chg_EB}=720µA, R_{OV2}=15KΩ,

$I_{chg_EB}'=I_{chg_EB}-(4.5V+0.9V)/(2*R_{OV2})$=540 µA

Extended blanking time = $256*(C_{BK}*(4.5V-0.9V)/ I_{chg_EB}'+ C_{BK}*500*ln(4.5/0.9))$ = 192ms

Total blanking time = 20ms+192 = 212ms

where I_{chg_EB}'=net charging current to C_{BK}

Note: The above calculation does not include the effect of the input OVP circuit where there is extra biasing current flowing from the input. That means the extended blanking time will be shortened with the line voltage change if input OVP circuit is implemented.

3.7.2 Active Burst Mode (patented)

To increase the efficiency of the system at light load, the most effective way is to operate at burst mode. Starting from CoolSET™™ F3, the IC has been employing the active burst mode and it can achieve the lowest standby power. ICE3AR1080VJZ adopts the same concept with some more innovative improvements to the feature. It includes the adjustable entry burst level, close power control between high line and low line and the smaller output ripple during burst mode.

Most of the burst mode design in the market will provide a fixed entry burst mode level which is a ratio to the maximum power of the design. ICE3AR1080VJZ provides a more flexible level which can be selected externally. The provision also includes not entering burst mode.

Propagation delay is the major contributor for the power control variation for DCM flyback converter. It is proved to be effective in the maximum power control. ICE3AR1080VJZ also apply the same concept in the burst mode. Therefore, the entry and exit burst mode power is also finely controlled during burst mode.

The feedback control swing during burst mode will affect the output ripple voltage directly. ICE3AR1080VJZ reduces the swing from 0.5V to 0.3V. Therefore, it would have around 40% improvement for the output ripple.

Figure 25: Active Burst Mode

The Active Burst Mode is located in the Control Unit. Figure 24 shows the related components.

3.7.2.1 Selectable burst entry level

The burst mode entry level can be selected by changing the different capacitor C_{FB} at FBB pin. There are 4 levels to be selected with different capacitor which are targeted for 10%, 6.67%, 4.38% and 0% of the maximum input power. At the same time, the exit burst levels are targeted to 20%, 13.3%, 9.6% and 0% of the maximum power accordingly. The corresponding capacitance range is from 6.8nF to 100pF. The below table is the recommended capacitance range for the entry and exit level with the C_{FB} capacitor.

CFB	Entry level		Exit level	
	% of Pin_max	VFB_burst	% of Pin_max	Vcsth_burst
>=6.8nF (5%,X7R)	10%	1.60V	20%	0.45V
1nF~2.2nF (1%,COG)	6.67%	1.42V	13.3%	0.37V
220pF~470pF (1%,COG)	4.38%	1.27V	9.6%	0.31V
<=100pF (1%,COG)	0%	never	0%	always

The selection is at the 1st 1ms of the UVLO “ON” (Vcc > 17V) during the 1st start up but it does not detect in the subsequent re-start due to auto-restart protection. In case there is protection triggered such as input OVP before starts up, the detection will be held until the protection is removed. When the Vcc reaches the UVLO “ON” in the 1st start up, the capacitor C_{FB} at FBB pin is charged by a 5V voltage source through the R_{FB} resistor. When the voltage at FBB pin hits 4.5V, the FF4 will be set, the switch S9 is turned “ON” and the counter will increase by 1. Then the C_{FB} is discharged through a 500Ω resistor. After reaching 0.5V, the FF4 is reset and the switch S9 is turned “OFF”. Then the C_{FB} capacitor is charged by the 5V voltage source again until it reaches 4.5V. The process repeats until the end of 1ms. Then the detection is ended. After that, the total number of count in the counter is compared and the $V_{FB\text{-}burst}$ and the V_{cs_burst} are selected accordingly (Figure 26)

Figure 26: Entry Burst Mode detection

3.7.2.2 Entering Active Burst Mode

The FBB signal is kept monitoring by the comparator C5 (Figure 25). During normal operation, the internal blanking time counter is reset to 0. When FBB signal falls below V_{FB_burst}, it starts to count. When the counter reaches 20ms and FBB signal is still below V_{FB_burst}, the system enters the Active Burst Mode. This time window prevents a sudden entering into the Active Burst Mode due to large load jumps.

After entering Active Burst Mode, a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC to about 620µA.

It needs the application to enforce the VCC voltage above the Undervoltage Lockout level of 10.5V such that the Startup Cell will not be switched on accidentally. Or otherwise the power loss will increase drastically. The minimum VCC level during Active Burst Mode depends on the load condition and the application. The lowest VCC level is reached at no load condition.

3.7.2.3 Working in Active Burst Mode

After entering the Active Burst Mode, the FBB voltage rises as V_{OUT} starts to decrease, which is due to the inactive PWM section. The comparator C6a monitors the FBB signal. If the voltage level is larger than 3.5V, the internal circuit will be activated; the Internal Bias circuit resumes and starts to provide switching pulse. In Active Burst Mode the gate G10 is released and the current limit is reduced to V_{csth_burst} (Figure 3 and Figure 25). In one hand, it can reduce the conduction loss and the other hand, it can reduce the audible noise. If the load at V_{OUT} is still kept unchanged, the FBB signal will drop to 3.2V. At this level the C6b deactivates the internal circuit again by switching off the Internal Bias. The gate G11 is active again as the burst flag is set after entering Active Burst Mode. In Active Burst Mode, the FBB voltage is changing like a saw tooth between 3.2V and 3.5V (Figure 27).

3.7.2.4 Leaving Active Burst Mode

The FBB voltage will increase immediately if there is a high load jump. This is observed by the comparator C13 (Figure 25). Since the current limit is reduced to 31%~45% of the maximum current during active burst mode, it needs a certain load jump to raise the FBB signal to exceed 4.0V. At that time the comparator C5 resets the Active Burst Mode control which in turn blocks the comparator C12 by the gate G10. The maximum current can then be resumed to stabilize V_{OUT}.

Figure 27: ***Signals in Active Burst Mode***

3.7.3 Protection Modes

The IC provides Auto Restart mode as the major protection feature. Auto Restart mode can prevent the SMPS from destructive states. There are 3 kinds of auto restart mode; normal auto restart mode, odd skip auto restart mode and non switch auto restart mode. Odd skip auto restart mode is that there is no detect of fault and no switching pulse for the odd number restart cycle. At the even number of restart cycle the fault detect and soft start switching pulses maintained. If the fault persists, it would continue the auto-restart mode. However, if the fault is removed, it can release to normal operation only at the even number auto restart cycle (Figure 28).

Figure 28: **Odd skip auto restart waveform**

Non switch auto restart mode is similar to odd skip auto restart mode except the start up switching pulses are also suppressed at the even number of the restart cycle. The detection of fault still remains at the even number of the restart cycle. When the fault is removed, the IC will resume to normal operation at the even number of the restart cycle (Figure 29).

Figure 29: Non switch auto restart waveform

The main purpose of the odd skip auto restart is to extend the restart time such that the power loss during auto restart protection can be reduced. This feature is particularly good for smaller Vcc capacitor where the restart time is shorter.
The following table lists the possible system failures and the corresponding protection modes.

VCC Over voltage (1)	Odd skip Auto Restart Mode
VCC Over voltage (2)	Odd skip Auto Restart Mode
Over load	Odd skip Auto Restart Mode
Open Loop	Odd skip Auto Restart Mode
VCC Undervoltage	Normal Auto Restart Mode
Short Optocoupler	Normal Auto Restart Mode
Over temperature	Non switch Auto Restart Mode

3.7.3.1 Vcc OVP, OTP and Vcc under voltage

Figure 30: Vcc OVP and OTP

There are 2 types of Vcc over voltage protection; Vcc OVP (1) and Vcc OVP (2). The Vcc OVP (1) takes action only during the soft start period. The Vcc OVP (2) takes the action in any conditions.
Vcc OVP (1) condition is when V_{VCC} voltage is > 20.5V, V_{FBB} voltage is > 4.5V and during soft start period, the IC enters into odd skip Auto Restart Mode. This condition likely happens during start up at open loop fault (Figure 30).

Vcc OVP (2) condition is when V_{VCC} voltage is > 25.5V, the IC enters into odd skip Auto Restart Mode (Figure 30).
The over temperature protection OTP is sensed inside the controller IC. The Thermal Shutdown block keeps on monitoring the junction temperature of the controller. After detecting a junction temperature higher than 130°C, the IC will enter into the non switch Auto Restart mode. The ICE3AR1080VJZ has also implemented with a 50°C hysteresis. That means the IC can only be recovered when the controller junction temperature is dropped 50°C lower than the over temperature trigger point (Figure 30).

The VCC undervoltage and short opto-coupler will go into the normal auto restart mode inherently.

In case of VCC undervoltage, the Vcc voltage drops indefinitely. When it drops below the Vcc under voltage lock out "OFF" voltage (10.5V), the IC will turn off the IC and the startup cell will turn on again. Then the Vcc voltage will be charged up to UVLO "ON" voltage (17V) and the IC turns on again provided the startup cell charge up current is not drained by the fault. If the fault is not removed, the Vcc will continue to drop until it hits UVLO "OFF" voltage and the restart cycle repeats.

Short Optocoupler can lead to Vcc undervoltage because once the opto-coupler (transistor side) is shorted, the feedback voltage will drop to zero and there will be no switching pulse. Then the Vcc voltage will drop same as the Vcc undervoltage.

3.7.3.2 Over load, open loop protection

Figure 31: Over load, open loop protection

In case of Overload or Open Loop, the FBB exceeds 4.5V which will be observed by comparator C4. Then the built-in blanking time counter starts to count. When it reaches 20ms, the extended blanking time counter CT1 is activated. The switch S2 is turned on and the voltage at the BV pin will be discharged through 500Ω resistor. When it drops to 0.9V, the switch S2 is turned off and the Switch S1 is turned on. Then a constant current source I_{chg_EB} will start to charge up BV pin. When the voltage hits 4.5V which is monitored by comparator C11, the switch S1 is turned off and the count will increase by 1. Then the switch S2 will turn on again and the voltage will drop to 0.9V and rise to 4.5V again. The count will then increase by 1 again. When the total count reaches 256, the counter CT1 will stop and it will release a high output signal. When both the input signals at AND gate G5 is high, the odd skip Auto Restart Mode is activated after the 30µs spike blanking time (Figure 31).

The total blanking time depends on the addition of the built-in and the extended blanking time. If there is no C_{BK} capacitor at BV pin, the count will finish within 0.1ms and the equivalent blanking time is just the built-in time of 20ms.

Since the BV pin is a multi-function pin, it would share with different functions. The resistor R_{OV2} from input OVP feature application may however affect the extendable blanking time (Figure 31). Thus it should take the R_{OV2} into the calculation of the extendable blanking time. For example the extended blanking time may be changed from 181ms to 212ms for 42.2KΩ to 15KΩ R_{OV2} resistor. The list below shows one particular C_{BK}, R_{OV2} vs blanking time.

C_{BK}	R_{OV2}	Extended blanking time	Overall blanking time
0.1uF	42.2KΩ	161ms	181ms
0.1uF	39.6KΩ	162ms	182ms
0.1uF	15KΩ	192ms	212ms

Another factor to affect the extended blanking time is the input voltage through the R_{OV1} and R_{OV2}. It would, on the contrary, reduce the extended blanking time.

3.7.4 Input OVP Mode

When the AC input voltage is out of the designed operating range (e.g. > 300Vac), the voltage at the input bulk capacitor will increase at the same time. If the MOSFET keeps on switching, the drain voltage may be too high and the MOSFET will exceed the maximum voltage rating and causes damages. The input OVP mode is to prevent this phenomenon. The IC will sense the input voltage through the input bulk capacitor to the BV pin by 2 potential divider resistors, R_{OV1} and R_{OV2} (Figure 32). During normal operation, the BV pin voltage is lower than V_{OVP_ref} (1.98V). The output of C14a is low and the output of G21 is high. Together with UVLO high signal (IC operating) the “S” input of FF5 is low. The “Q” output of FF5 is low and the input OVP mode remains not activated. When there is an input over voltage case, the input bulk capacitor voltage is increased and the BV voltage is increased to larger than V_{OVP_ref}. The output of C14a is high and the output of G21 is low. If the OVP persists for 400µs (blanking time) and the UVLO signal is still high, the output of G20 is high. Then the “S” input of FF5 is high and the “Q” output of FF5 is high. The input OVP mode is set. The case of UVLO signal low is not considered as it means the IC is not working.

Figure 32: Input OVP detection circuit

Once the system enters the input OVP mode, there will be no switching pulse and the IC keeps on monitoring the BV signal. If the input OVP signal is not reset, there is no switching pulse in each restart cycle (Figure 33).

Figure 33: Input OVP mode waveform

The IC implemented with hysteresis voltage to leave the input OVP protection. The hysteresis voltage at BV pin is V_{OVP_hys} (0.07V) and the input OVP reset voltage at BV pin is V_{OVP_ref} - V_{OVP_hys}; i.e. 1.91V. After the input OVP protection is triggered, the voltage at BV pin needs to drop V_{OVP_hys} from V_{OVP_ref} before it can be reset.
When the BV voltage drops below 1.91V, the output of C14b and G22 are high (Figure 32). The "R" input of the FF5 is high. Then the "Q" output of FF5 is low. The input OVP is reset. The system will turn on with soft start in the coming restart cycle when Vcc reaches the Vcc "ON" voltage at 17V.

The input OVP feature can also be applied to customer defined protection circuit by pulling up the BV pin to larger than V_{OVP_ref}.

The formula to calculate the R_{OV1} and R_{OV2} are as below.

Set R_{OV1} to a particular value.

$$R_{OV2} = R_{OV1} * V_{OVP_ref} / (V_{OVP} - V_{OVP_ref})$$

The formula to calculate the input OVP reset voltage is as below.

$$V_{OVP_reset} = (V_{OVP_ref} - V_{OVP_hys}) * (R_{OV1} + R_{OV2}) / R_{OV2}$$

where V_{OVP}: input over voltage; V_{OVP_reset}: input over reset voltage; V_{OVP_ref}: IC reference voltage for OVP; V_{OVP_hys}: IC hysteresis voltage for OVP; R_{OV1} and R_{OV2}: resistors divider from input voltage to BV pin.

For example,

V_{OVP_ref}=1.98V, V_{OVP_hys}=0.07V

If input OVP voltage, V_{OVP}=424Vdc (300Vac), R_{OV1}=9MΩ, R_{OV2}=42.2KΩ
Input OVP reset, V_{OVP_reset}=408Vdc (289Vac)

To disable input OVP feature, the BV pin must be connected with a resistor R_{OV2}≥15KΩ to IC ground and remove R_{OV1}.

(Remark: R_{OV2} must be always ≥15KΩ in all conditions, otherwise overload protection may not work)

3.7.5 Action sequence at BV pin

Since there are 2 functions at the same BV pin; input OVP and extended blanking time, the action of sequence is whichever starts first takes the priority. When the "Extended blanking time" is triggered by OLP and follows with the "Input OVP" triggering, then the OLP will continue to work until it ends. The IC would recheck the signal at BV pin after one skip cycle. If the BV signal exceeds the input OVP threshold, it would go to input OVP mode.

Figure 34: Input OVP during extended blanking time

One typical case happened is that the overload happened first and it follows with the “Input OVP” feature at the 1st 20ms blanking time. Since the overload protection is still not triggered at the 1st 20ms blanking time period and the extended blanking time is not running, the input OVP mode will trigger right away.

Figure 35: Input OVP during first 20ms blanking time

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit. T_a=25°C unless otherwise specified.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Drain Source Voltage	V_{DS}	-	800	V	
Pulse drain current, t_p limited by T_{jmax}	$I_{D\ Puls}$	-	11.5	A	
Avalanche energy, repetitive t_{AR} limited by max. T_j=150°C[1)]	E_{AR}	-	0.1	mJ	
Avalanche current, repetitive t_{AR} limited by max. T_j=150°C	I_{AR}	-	3.5	A	
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
FBB Voltage	V_{FBB}	-0.3	5.5	V	
BV Voltage	V_{BV}	-0.3	5.5	V	
CS Voltage	V_{CS}	-0.3	5.5	V	
Junction Temperature	T_j	-40	150	°C	Controller & CoolMOS™
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction -Ambient	R_{thJA}	-	96	K/W	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	260	°C	1.6mm (0.063in.) from case for 10s
ESD Capability (incl. Drain Pin)	V_{ESD}	-	2	kV	Human body model[2)]

1) Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$

2) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5KΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	25	V	Max value limited due to Vcc OVP
Junction Temperature of Controller	T_{jCon}	-40	130	°C	Max value limited due to thermal shut down of controller
Junction Temperature of CoolMOS™	$T_{jCoolMOS}$	-40	150	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 17 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCCstart}$	-	200	300	µ A	V_{VCC} =16V
VCC Charge Current	$I_{VCCcharge1}$	-	-	5.0	mA	V_{VCC} = 0V
	$I_{VCCcharge2}$	0.55	0.9	1.60	mA	V_{VCC} = 1V
	$I_{VCCcharge3}$	0.38	0.7	-	mA	V_{VCC} =16V
Leakage Current of Start Up Cell and CoolMOS™	$I_{StartLeak}$	-	0.2	50	µ A	V_{Drain} = 650V at T_j=100°C[1)]
Supply Current with Inactive Gate	$I_{VCCsup1}$	-	1.9	3.2	mA	
Supply Current with Active Gate	$I_{VCCsup2}$	-	5.7	7.8	mA	I_{FBB} = 0A
Supply Current in Auto Restart Mode with Inactive Gate	$I_{VCCrestart}$	-	320	-	µ A	I_{FBB} = 0A
Supply Current in Active Burst Mode with Inactive Gate	$I_{VCCburst1}$	-	620	950	µ A	V_{FBB} = 2.5V
	$I_{VCCburst2}$	-	620	950	µ A	V_{VCC} = 11.5V, V_{FBB} = 2.5V
VCC Turn-On ThresholdVCC Turn-Off Threshold VCC Turn-On/Off Hysteresis	V_{VCCon} V_{VCCoff} V_{VCChys}	16.0 9.8 -	17.0 10.5 6.5	18.0 11.2 -	V V V	

1) The parameter is not subjected to production test - verified by design/characterization

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	V_{REF}	4.90	5.00	5.10	V	measured at pin FBB $I_{FBB} = 0$

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Oscillator Frequency	f_{OSC1}	87	100	113	kHz	
	f_{OSC2}	90	100	108	kHz	$T_j = 25°C$
Frequency Jittering Range	f_{jitter}	-	±4.0	-	kHz	$T_j = 25°C$
Frequency Jittering period	T_{jitter}	-	4.0	-	ms	$T_j = 25°C$
Max. Duty Cycle	D_{max}	0.70	0.75	0.80		
Min. Duty Cycle	D_{min}	0	-	-		$V_{FBB} < 0.3V$
PWM-OP Gain	A_V	3.05	3.25	3.45		
Voltage Ramp Offset	$V_{Offset\text{-}Ramp}$	-	0.60	-	V	
V_{FBB} Operating Range Min Level	V_{FBmin}	-	0.7	-	V	
V_{FBB} Operating Range Max level	V_{FBmax}	-	-	4.3	V	CS=1V, limited by Comparator C4[1)]
FBB Pull-Up Resistor	R_{FB}	9.0	15.4	23.0	k Ω	

1) The parameter is not subjected to production test - verified by design/characterization

4.3.4 Soft Start time

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft Start time	t_{SS}	-	10	-	ms	

4.3.5 Control Unit

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Input OVP reference voltage for comparator C14a		V_{OVP_ref}	1.90	1.98	2.06	V	T_j = 25°C
Input OVP hysteresis C14b		V_{OVP_hys}		0.07		V	T_j = 25°C
Blanking time voltage lower limit for Comparator C3		V_{BKC3}	0.80	0.90	1.00	V	
Blanking time voltage upper limit for Comparator C11		V_{BKC11}	4.28	4.50	4.72	V	
Over Load Limit for Comparator C4		V_{FBC4}	4.28	4.50	4.72	V	
Entry Burst select High level for Comparator C19		V_{FBC19}	4.28	4.50	4.72	V	
Entry Burst select Low level for Comparator C20		V_{FBC20}	0.40	0.50	0.60	V	
Active Burst Mode Entry Level for Comparator C5	10% P_{in_max}	V_{FB_burst1}	1.51	1.60	1.69	V	< 7 counts
	6.67% P_{in_max}	V_{FB_burst2}	1.34	1.42	1.50	V	8 ~ 39 counts
	4.38% P_{in_max}	V_{FB_burst3}	1.20	1.27	1.34	V	40 ~ 191 counts
Active Burst Mode High Level for Comparator C6a		V_{FBC6a}	3.35	3.50	3.65	V	In Active Burst Mode
Active Burst Mode Low Level for Comparator C6b		V_{FBC6b}	3.06	3.20	3.34	V	
Active Burst Mode Level for Comparator C13		V_{FBC13}	3.85	4.00	4.15	V	
Overvoltage Detection Limit for Comparator C1		$V_{VCCOVP1}$	19.5	20.5	21.5	V	V_{FBB} = 5V, during soft start
Overvoltage Detection Limit for Comparator C2		$V_{VCCOVP2}$	25.0	25.5	26.3	V	
Charging current for extended blanking time		I_{chg_EB}	460	720	864	µA	
Thermal Shutdown1)		T_{jSD}	130	140	150	°C	Controller
Hysteresis for thermal Shutdown1)		T_{jSD_hys}	-	50	-	°C	
Built-in Blanking Time for Overload Protection or enter Active Burst Mode		t_{BK}	-	20	-	ms	
Timer for entry burst select		t_{EBS}	-	1	-	ms	
Spike Blanking Time for Auto-Restart Protection		t_{Spike}	-	30	-	µs	

1) The parameter is not subjected to production test - verified by design/characterization. The thermal shutdown temperature refers to the junction temperature of the controller.

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP} *and* V_{VCCPD}

4.3.6 Current Limiting

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay)		V_{csth}	0.98	1.06	1.13	V	dV_{sense} / dt = 0.6V/µs (Figure 21)
Peak Current Limitation during Active Burst Mode	20% P_{in_max}	V_{csth_burst1}	0.37	0.45	0.51	V	< 7 counts
	13.3% P_{in_max}	V_{csth_burst2}	0.30	0.37	0.44	V	8 ~ 39 counts
	9.6% P_{in_max}	V_{csth_burst3}	0.23	0.31	0.37	V	40 ~ 191 counts
Leading Edge Blanking	Normal mode	t_{LEB_normal}	-	220	-	ns	
	Burst mode	t_{LEB_burst}	-	180	-	ns	
CS Input Bias Current		I_{CSbias}	-1.5	-0.2	-	µ A	V_{CS} =0V

4.3.7 CoolMOS™ Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	800 870	- -	- -	V V	T_j = 25°C T_j = 110°C[1)]
Drain Source On-Resistance	R_{DSon}	- -	1.00 2.24	1.11 2.46	Ω Ω	T_j = 25°C T_j=125°C[1)] at I_D = 1.35A
Effective output capacitance, energy related	$C_{o(er)}$	-	24	-	pF	V_{DS} = 0V to 480V
Rise Time	t_{rise}	-	30[2)]	-	ns	
Fall Time	t_{fall}	-	30[2)]	-	ns	

1) The parameter is not subjected to production test - verified by design/characterization

2) Measured in a Typical Flyback Converter Application

5 Typical Controller Performance Characteristics

Characterisrtic graphs are normalized at T_a=25°C

Figure 36: Line OVP (V_{OVP_ref}) vs. T_a

Figure 37: Hystersis of Line OVP (V_{OVP_hys}) vs. T_a

6 CoolMOS™ Performance Characteristics

Figure 38: Safe Operating Area (SOA) curve for ICE3AR1080VJZ

Figure 39: SOA temperature derating coefficient curve

Figure 40: **Power dissipation; $P_{tot}=f(T_a)$**

Figure 41: **Drain-source breakdown voltage; $V_{BR(DSS)}=f(T_j)$, I_D=0.25mA**

7 Input Power Curve

Two input power curves giving the typical input power versus ambient temperature are showed below; Vin=85Vac~265Vac (Figure 42) and Vin=230Vac+/-15% (Figure 43). The curves are derived based on a typical discontinuous mode flyback model which considers either 50% maximum duty ratio or 100V maximum secondary to primary reflected voltage (higher priority). The calculation is based on no copper area as heatsink for the device. The input power already includes the power loss at input common mode choke, bridge rectifier and the CoolMOS™. The device saturation current (I_{D_Puls} @ T_j=125°C) is also considered.

To estimate the output power of the device, it is simply multiplying the input power at a particular operating ambient temperature with the estimated efficiency for the application. For example, a wide range input voltage (Figure 42), operating temperature is 50°C, estimated efficiency is 85%, then the estimated output power is 38W (45W * 85%).

Figure 42: Input power curve Vin=85~265Vac; P_{in}=f(T_a)

Figure 43: Input power curve Vin=230Vac; P_{in}=f(T_a)

8 Outline Dimension

1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.57	-	0.180
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.70	-	0.067
c	0.20	0.36	0.008	0.014
D	9.10	9.77	0.358	0.385
E	7.49	8.26	0.295	0.325
E1	6.10	6.60	0.240	0.260
e	2.54 BSC		0.1 BSC	
N	7		7	
eB	7.90	10.90	0.311	0.429
L	2.92	-	0.115	-

DOCUMENT NO.
Z8B00155542

SCALE 0 1.0 0 1.0 2mm

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Figure 44: PG-DIP-7 (Pb-free lead plating Plastic Dual-in-Line Outline)

9 Marking

Figure 45: Marking for ICE3AR1080VJZ

10 Schematic for recommended PCB layout

Figure 46: Schematic for recommended PCB layout

General guideline for PCB layout design using F3 CoolSET™ (refer to Figure 46):

1. "Star Ground "at bulk capacitor ground, C11:

   "Star Ground "means all primary DC grounds should be connected to the ground of bulk capacitor C11 separately in one point. It can reduce the switching noise going into the sensitive pins of the CoolSET™ device effectively. The primary DC grounds include the followings.

   a. DC ground of the primary auxiliary winding in power transformer, TR1, and ground of C16 and Z11.
   b. DC ground of the current sense resistor, R12
   c. DC ground of the CoolSET™ device, GND pin of IC11; the signal grounds from C13, C14, C15 and collector of IC12 should be connected to the GND pin of IC11 and then "star "connect to the bulk capacitor ground.
   d. DC ground from bridge rectifier, BR1
   e. DC ground from the bridging Y-capacitor, C4

2. High voltage traces clearance:

   High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.

   a. 400V traces (positive rail of bulk capacitor C11) to nearby trace: > 2.0mm
   b. 600V traces (drain voltage of CoolSET™ IC11) to nearby trace: > 2.5mm

3. Filter capacitor close to the controller ground:

   Filter capacitors, C13, C14 and C15 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.

Guideline for PCB layout design when >3KV lightning surge test applied (refer to Figure 46):

1. Add spark gap

   Spark gap is a pair of saw-tooth like copper plate facing each other which can discharge the accumulated charge during surge test through the sharp point of the saw-tooth plate.

   a. Spark Gap 3 and Spark Gap 4, input common mode choke,
   L1: Gap separation is around 1.5mm (no safety concern)

   b. Spark Gap 1 and Spark Gap 2, Live / Neutral to GROUND:
   These 2 Spark Gaps can be used when the lightning surge requirement is>6KV.
   230Vac input voltage application, the gap separation is around 5.5mm
   115Vac input voltage application, the gap separation is around 3mm

2. Add Y-capacitor (C2 and C3) in the Live and Neutral to ground even though it is a 2-pin input
3. Add negative pulse clamping diode, D11 to the Current sense resistor, R12:

   The negative pulse clamping diode can reduce the negative pulse going into the CS pin of the CoolSET™ and reduce the abnormal behavior of the CoolSET™. The diode can be a fast speed diode such as 1N4148.

   The principle behind is to drain the high surge voltage from Live/Neutral to Ground without passing through the sensitive components such as the primary controller, IC11.

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