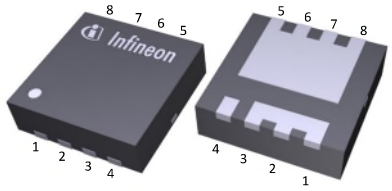
MOSFET

OptiMOS™5 Power-Transistor, 80 V

PG-TSDSON-8 FL



Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, logic level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1)] for target applications
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability with enlarged source interconnection

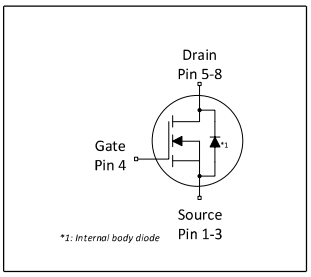


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	7.0	mΩ
I_D	74	A
Q_{oss}	29	nC
Q_G(0V..4.5V)	14	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ070N08LS5	PG-TSDSON-8 FL	070N08L	-

[1)] J-STD20 and JESD22

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	74 47 13	A	T_C=25 °C T_C=100 °C T_A=25 °C, R_{thJA}=60 K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	296	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	104	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	69	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.1	1.8	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	60	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=36 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	7.4 5.9	9.4 7.0	mΩ	V_{GS}=4.5 V, I_D=10 A V_{GS}=10 V, I_D=20 A
Gate resistance[1)]	R_G	-	1.3	2	Ω	-
Transconductance	g_{fs}	26	52	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1800	2340	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	280	364	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	12	21	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	6.1	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	4.8	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	24.6	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	5.8	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1)]	Q_{gd}	-	5	7	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	6.9	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	14.1	18	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	25	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	29	39	nC	V_{DD}=40 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test
[2)] See "Gate charge waveforms" for parameter definition

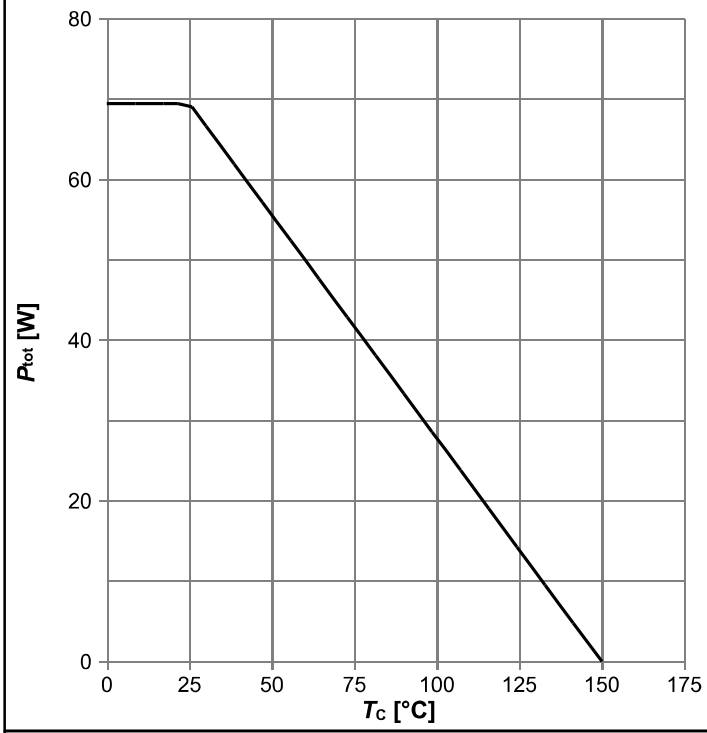
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	48	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	296	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.85	1.2	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	32	64	ns	V_R=40 V, I_F=20 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	27	54	nC	V_R=40 V, I_F=20 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test

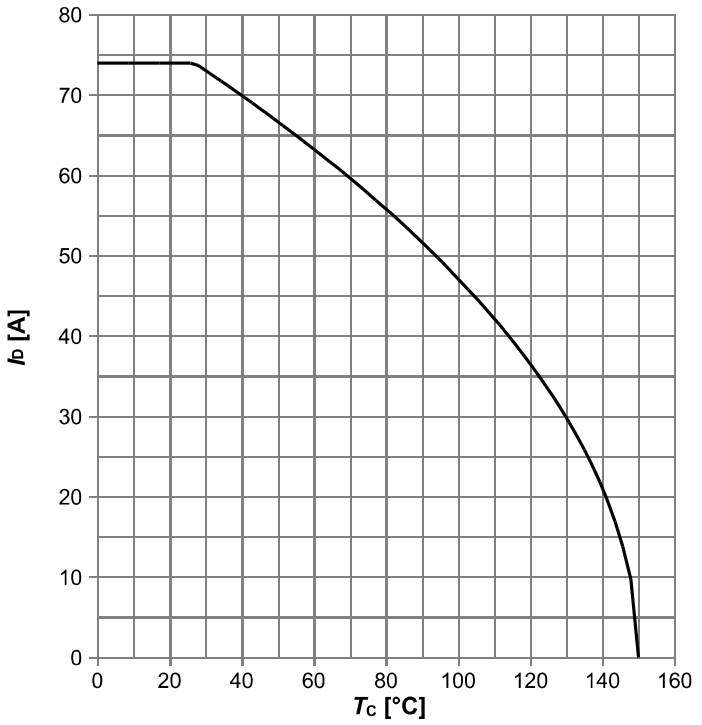
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



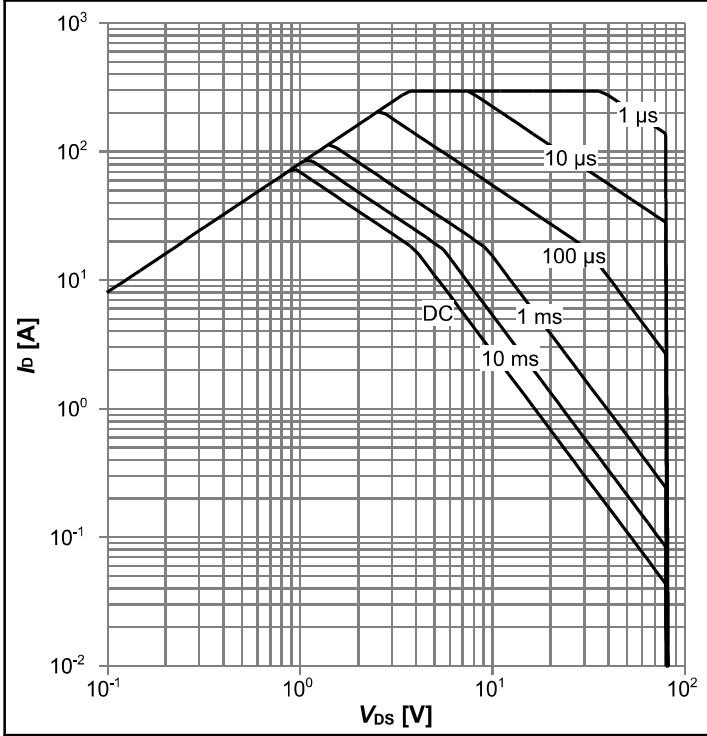
$P_{tot}=f(T_C)$

Diagram 2: Drain current



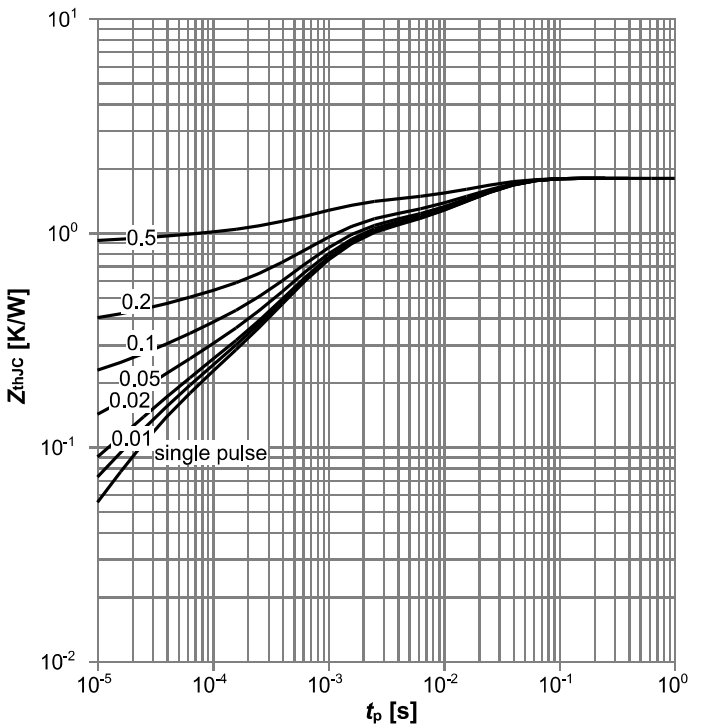
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



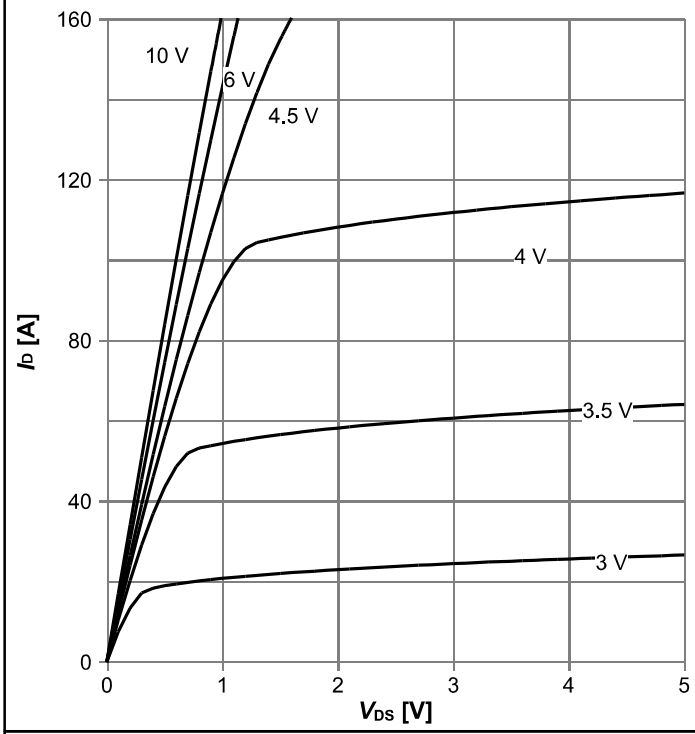
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



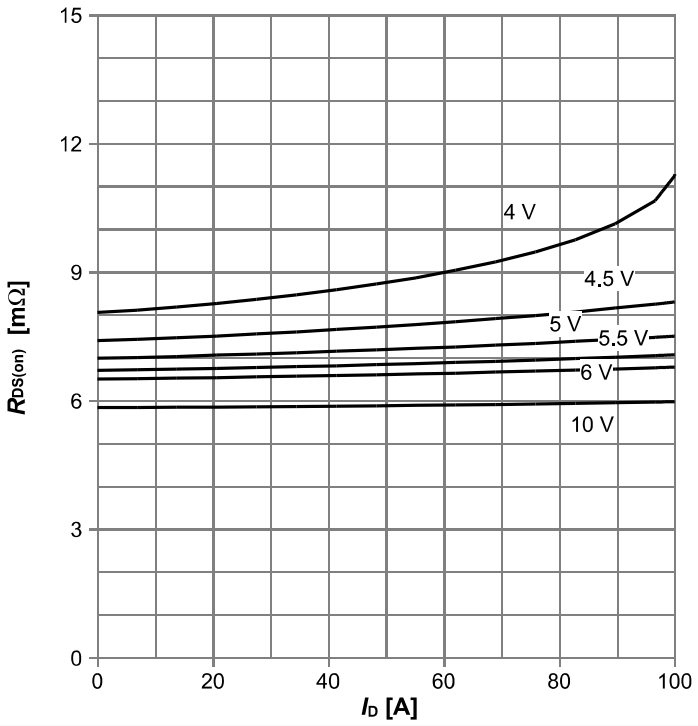
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



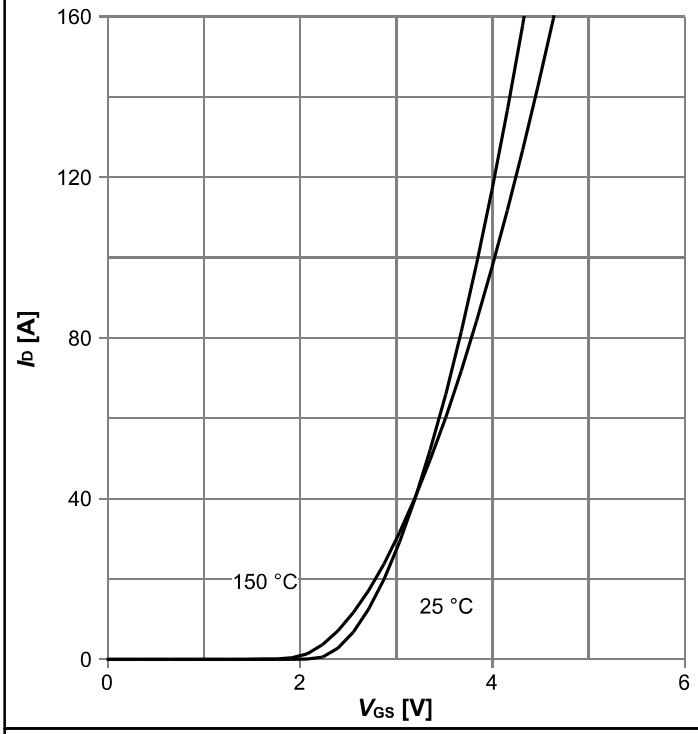
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



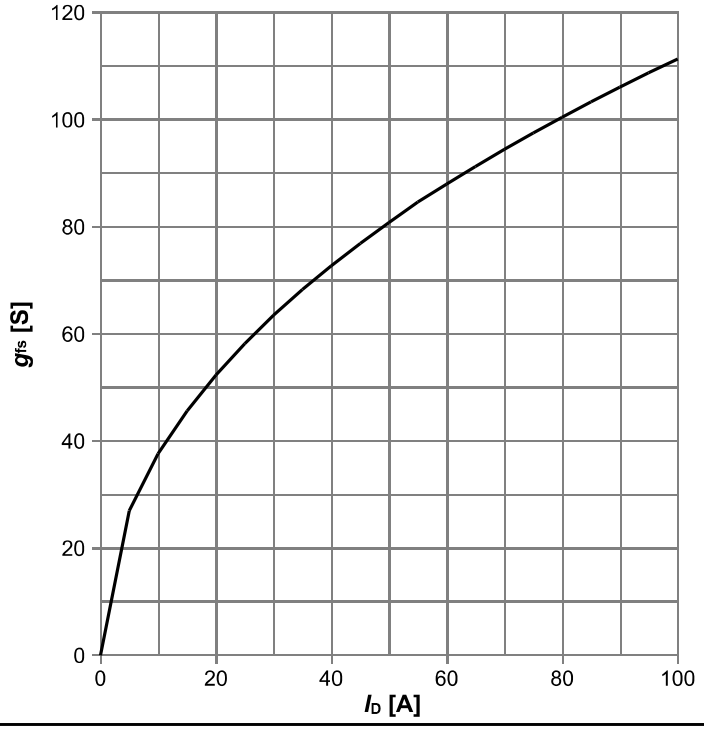
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



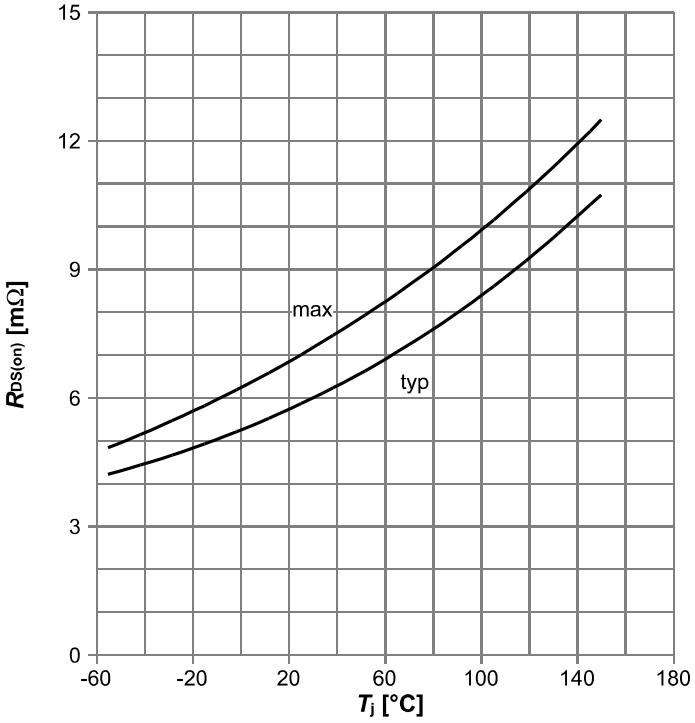
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



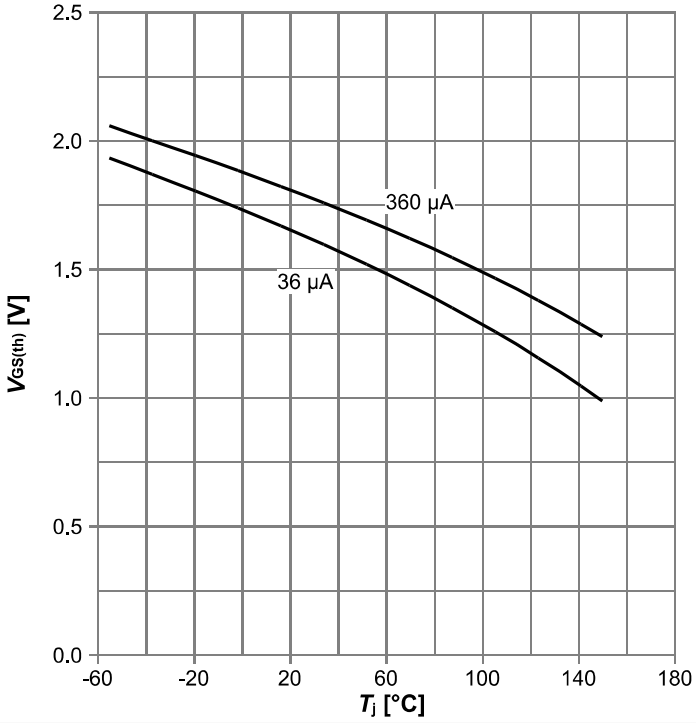
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



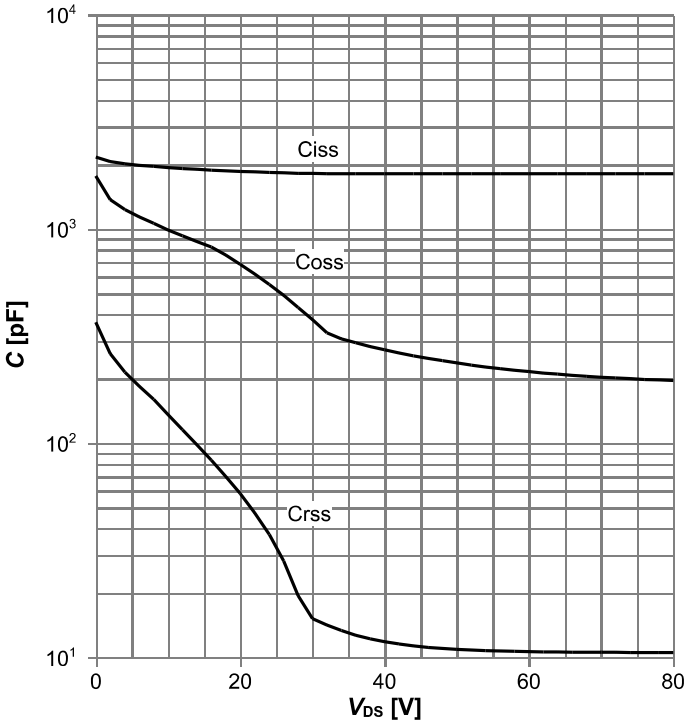
$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



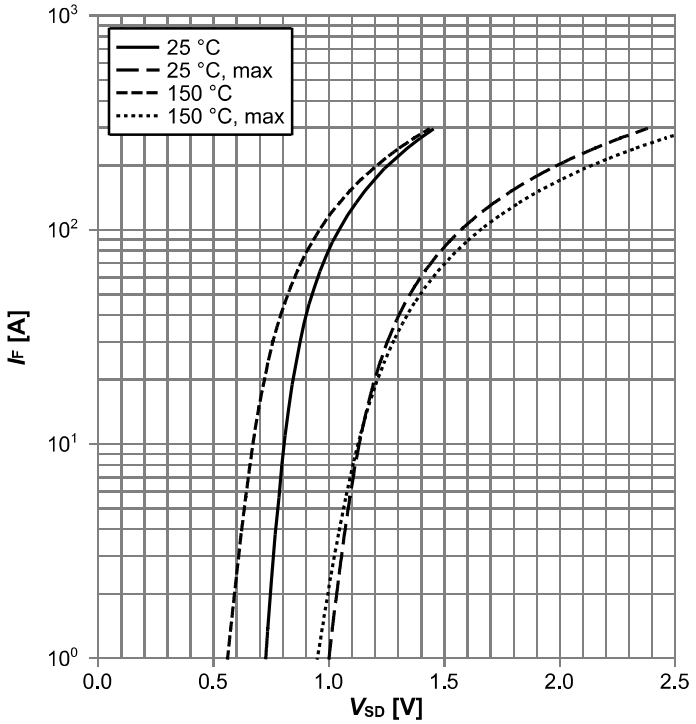
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



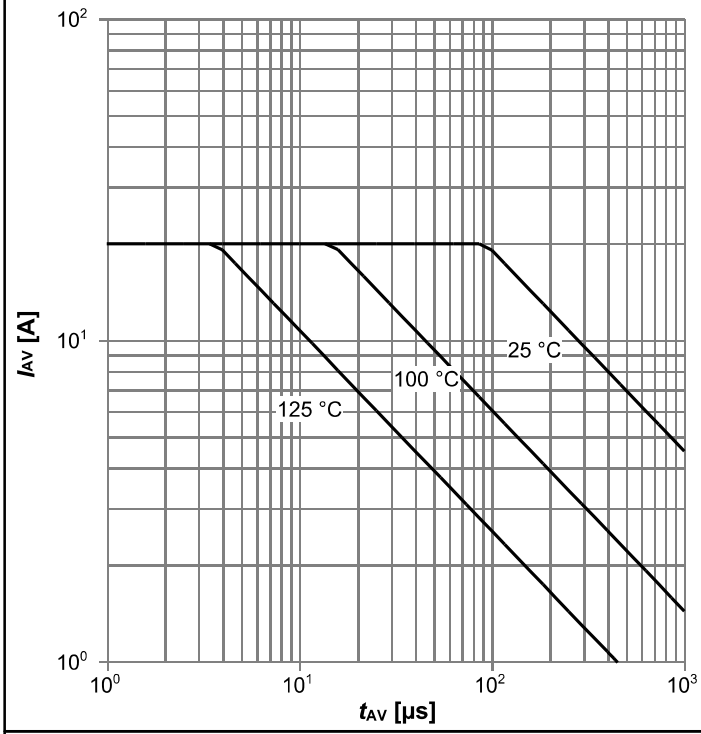
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



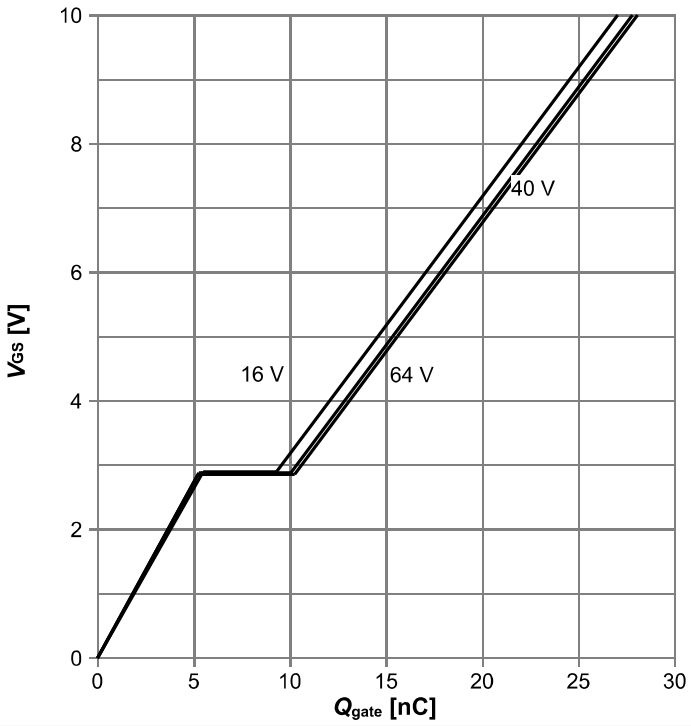
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



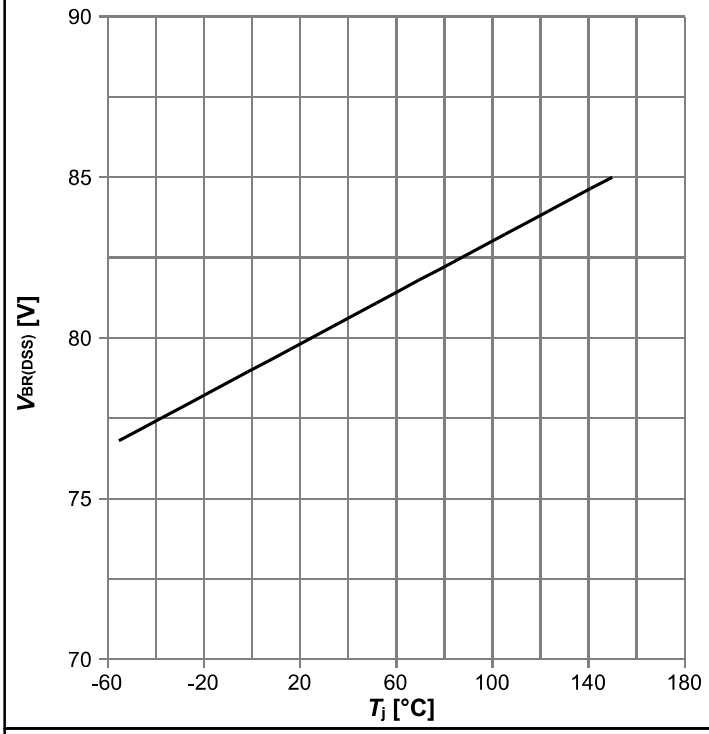
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



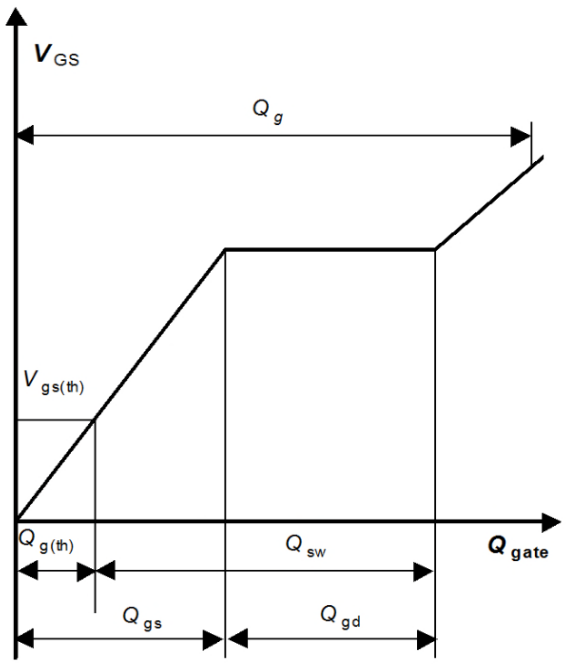
$V_{GS}=f(Q_{gate})$; $I_D=20$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

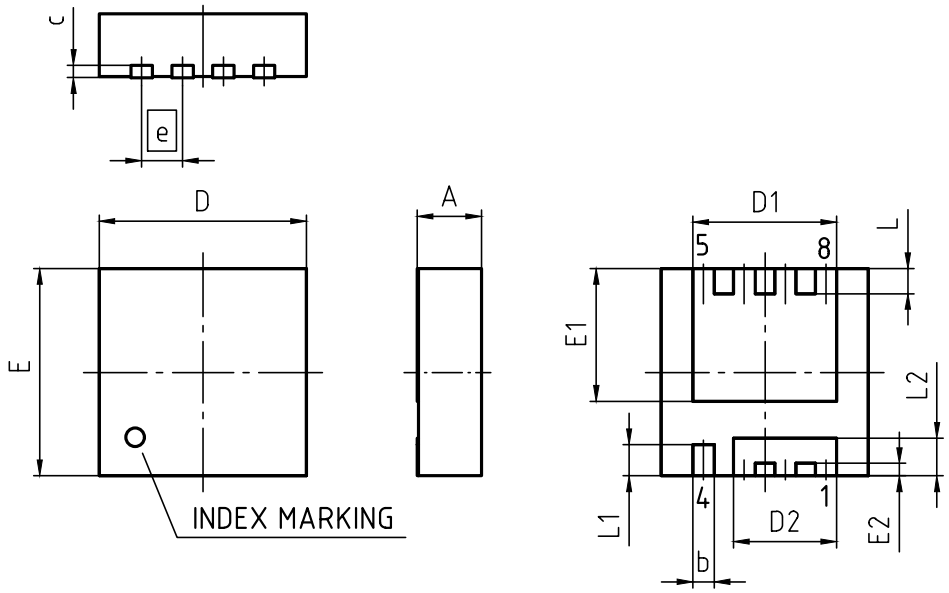


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
REVISION: 03	DATE: 20.10.2020	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

BSZ070N08LS5

Revision: 2021-04-16, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-03-23	Release of final version
2.1	2016-04-21	Update "Gate threshold voltage"
2.2	2016-08-18	Update Qsw
2.3	2021-04-16	Update current rating and package drawing

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