Short Circuit Behaviour of IGBT³ 600 V

With the development of eupec's and Infineon's latest 600 V IGBT³ technology the short circuit specification of this new chip generation was changed compared to the other eupec / Infineon chip generations. This is a result of extensive discussions with customers about application requirements.
The short circuit withstand time of the IGBT³ 600 V is specified at 6 µs. This is the best choice between low on-state losses and short circuit withstand time in order to deliver maximum possible device efficiency to the customer. Modern short circuit detection methods are fast enough to recognise and turn-off a short circuit within 6 µs.

IGBT³ Technology:

For the 1200 V voltage class, the IGBT chip of the third generation is well established.
With additional benefits, an IGBT³ 600 V chip is available. Both, IGBT³ 600 V and its corresponding free wheeling diode EmCon3 are qualified for a maximum junction temperature of 175 °C and a maximum operating junction temperature under switching conditions of 150 °C. This is an increase by 25 K compared to former chip generations.
The IGBT chip of the third generation has a trench structure and combines the advantages of PT and NPT technologies thanks to an additional n-doped layer, known as the Field Stop (FS) layer, within the NPT structure.

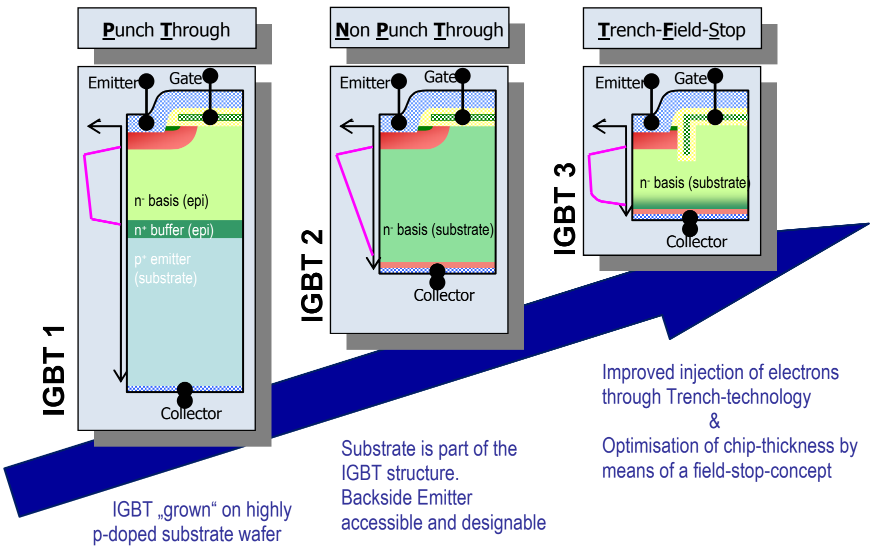

Fig. 1: Evolution of IGBT chip technologies

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The IGBT³ technology allows both, static and dynamic losses to be minimised. In combination with higher current density and higher junction temperature of the IGBT³, an increased current range of eupec IGBT modules and higher inverter power ratings can be realised.

Short Circuit Specification:

The IGBT³ 600 V is specified with a short circuit robustness up to t_{SCmax} = 6 µs at T_j = 150 °C, V_{GE} = 15 V and V_{CC} = 360 V and also up to t_{SCmax} = 8 µs at T_j = 25 °C, V_{GE} = 15 V and V_{CC} = 360 V. Between this to temperatures a linear approximation is allowed. In comparison to the IGBT², the temperature has been increased by 25 K (according to the increased max. operation temperature) and the guaranteed short circuit withstand time has been reduced from 10 µs to 6 µs.
The reduction of the short circuit withstand time is a well chosen operational point on the trade-off curve between device performance (e.g. losses under operation conditions) and short circuit withstand time.

Short Circuit Destruction Modes:

The following short circuit destruction modes of IGBTs are known:

a) Destruction during turn-off due to a latch-up which is related to the device over-temperature.

b) Destruction during the current pulse (current destruction mode) which is not related to the device temperature.

c) Destruction after a successful turn-off (energy destruction) due to a thermal runaway of the device as a consequence of the dissipated energy within this pulse. This destruction mode obviously largely depends on the device temperature prior to the short circuit.

Due to a latch-up free cell design the destruction mode a) is not crucial for the IGBT³ 600 V. The robust chip design also avoids destruction mode b).
With the IGBT³ 600 V only destruction mode c) can be observed.

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IGBT³ 600 V Short Circuit Performance Trade-Off:

The V_{CEsat} value is depending, among others, on the MOS channel width. An increased MOS channel width will lead to a lower V_{CEsat} value (lower on-state losses), but also to higher turn-off losses as well as higher short circuit currents and consequently to a decreased short circuit withstand time.

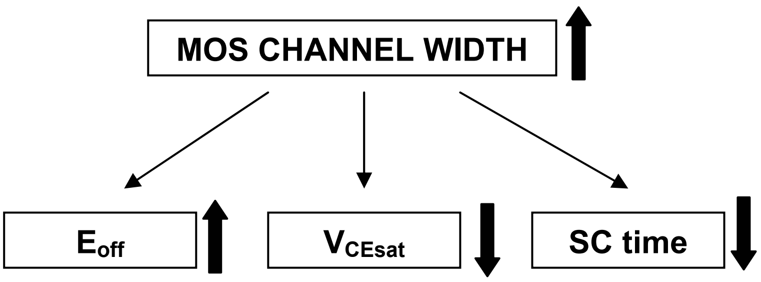

Fig. 2: E_{off}, V_{CEsat} and SC time as a function of MOS channel width

Fig. 3 shows the trade-off curves E_{off} = f (V_{CEsat}) (for a given thickness and a fixed backside emitter of the chip) and t_{SC} = f (V_{CEsat}) in principle. For minimised turn-off losses and also minimised on-state losses a SC time of 6 µs is the best choice to get the best performance.

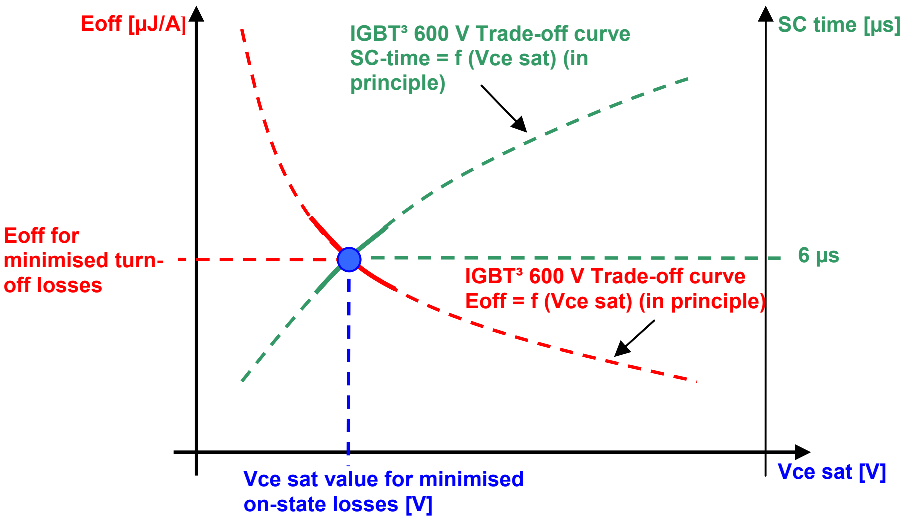

Fig. 3: IGBT³ Trade-off curves in principle

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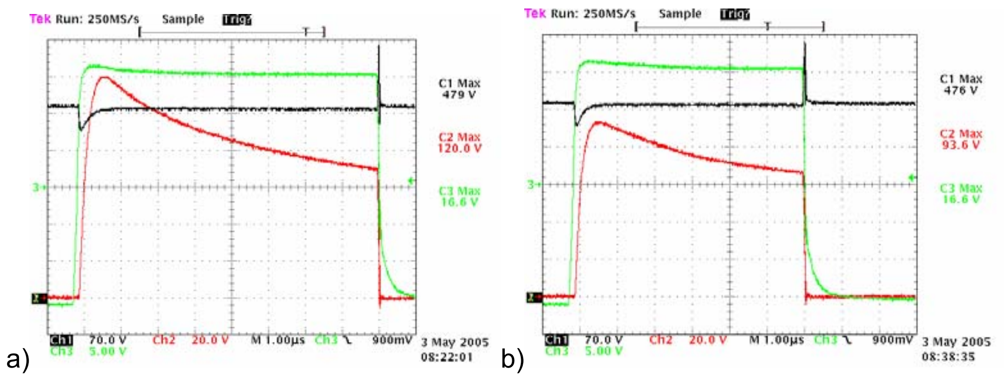

Fig. 4: IGBT³ - 600 V (15 A – Chip) Specified minimum short circuit capability (V_{CE} = 360 V; V_{GE} = 15 V; T_{vj} = 25 °C (a); T_{vj} 150 °C (b); t_{SC} = 8 µs (a); t_{SC} = 6 µs (b)) Red: I_C; Green: V_{GE}; Blue: V_{CE}

Fig. 4 displays the specified minimum short circuit capability @ Tvj = 25 °C as well as the short circuit capability @ Tvj = 150°C. Between these two values a linear interpolation is allowed (Fig. 5).

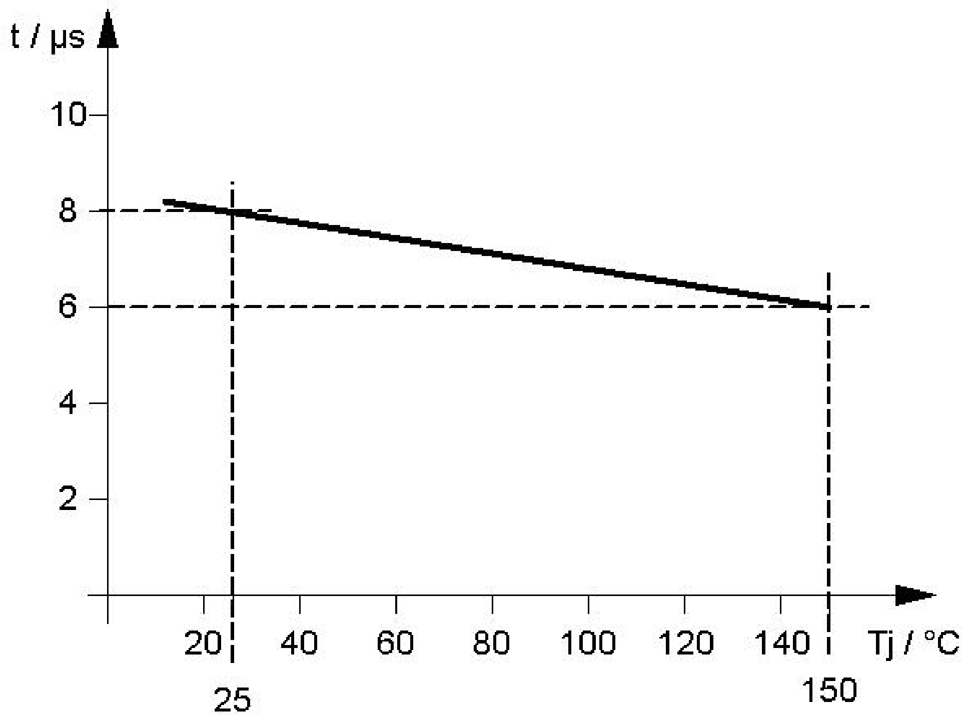

Fig. 5 Derating of the Short Circuit time as a function of the Junction Temperature tsc = f (Tj)

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Conclusion:

The above explanation clarifies that - once the IGBT technology is short-circuit robust - the further adjustment of a short circuit withstand time is a matter of definition.

In agreement with a variety of customers it has been decided to take into account the fact that modern short circuit detection methods are fast enough to recognise and turn-off a short circuit within 6 µs.

The device shows an excellent switching and short circuit robustness, with the specified short circuit time having been adjusted to 6 µs on a trade-off versus optimised device losses.

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