CoolMOS™ CFD2

FIRST 650V RATED SUPER JUNCTION MOSFET WITH FAST BODY DIODE SUITABLE FOR RESONANT TOPOLOGIES

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1. ABSTRACT

Nowadays, there is a growing need of resonant topologies in several applications like telecom, servers, solar and battery charging. This application note sets its focus on describing the new CFD(1) generation of Super Junction MOSFETs(2) which is especially optimized for these applications and is also suitable for non-resonant topologies giving a higher margin in repetitive hard commutation of the body diode limited by the junction temperature. Additionally the CFD generation are the first 650V high voltage devices on the market with an integrated fast body diode. This paper will prove that the two major goals, high efficiency and high reliability, are completely reached and Infineon Technologies sets a new reference in the market for high voltage MOSFETs. Furthermore, a detailed comparison between CFD2 and the former CFD generation will be demonstrated in different kind of application conditions.

2. INTRODUCTION

This application note was designed to give an engineer the opportunity to see improvements of the CFD2 in comparison to CFD. According to the construction of the MOSFET different theoretical improvements will be analyzed and verified by measurements. These improvements are for example a significant reduction of Q_g(3), $t_{rr,max}$(4) and $Q_{rr,max}$(5) values are defined in the datasheet, cost down for customers and other features and benefits which will be described in the next chapters of this application note. The following table shows the typical topologies and applications in which this product comes into operation.

Table 1: target topologies and applications

TOPOLOGY	APPLICATION
ZVS(6) phase shifted full bridge	Telecom
	Server
	Battery charging
	Solar
LLC	Server
	Telecom
	Battery charging
	Solar
	HID(7) lamp ballast
	LED(8) lighting
H4 bridge	Solar
3-level inverter	Solar inverter

Now that the target topologies and applications are listed, the table below illustrates the features and benefits of the CFD2.

Table 2: main features and benefits

FEATURES	BENEFITS
significant Q_g reduction	less gate drive capability necessary
	reduced turn ON and turn OFF time (better usage for ZVS window)
reduced Q_{rr}[9]	repetitive hard commutation (limited by $T_{junction}$[10])
defined $t_{rr,max}$ and $Q_{rr,max}$ values	design advantages
overall	lower price compared to C3[11] based CFD technology
	better lead time due to internal frontend manufacturing

The CFD2 is based on the C6[12] technology which, therefore, includes all improvements of the C6 compared to the previous C3 technology which are described in the application note "650V CoolMOS™ C6/E6".

3. MAIN DIFFERENCES CFD vs. CFD2

This chapter is going to analyze the most important differences between CFD and CFD2.

3.1 VOLTAGE RATING ($V_{(BR)DSS}$)

As visible in the datasheet there is a minimum drain-source breakdown voltage ($V_{(BR)DSS}$[13]) of 600V of CFD and 650V of CFD2. The 650V CFD2 is going to replace the 600V CFD. This increase of the breakdown voltage was decided to address the new solar market which needs 650V devices. This requirement is claimed to have a higher margin on the input stage of a converter due to the occurring voltage peaks from the solar panel bus.

3.2 GATE CHARGE (Q_g)

This section of the application note will describe one of the main improvements of the CFD2, the reduced Q_g. The following figure describes what happens if the MOSFET has a lower Q_g.

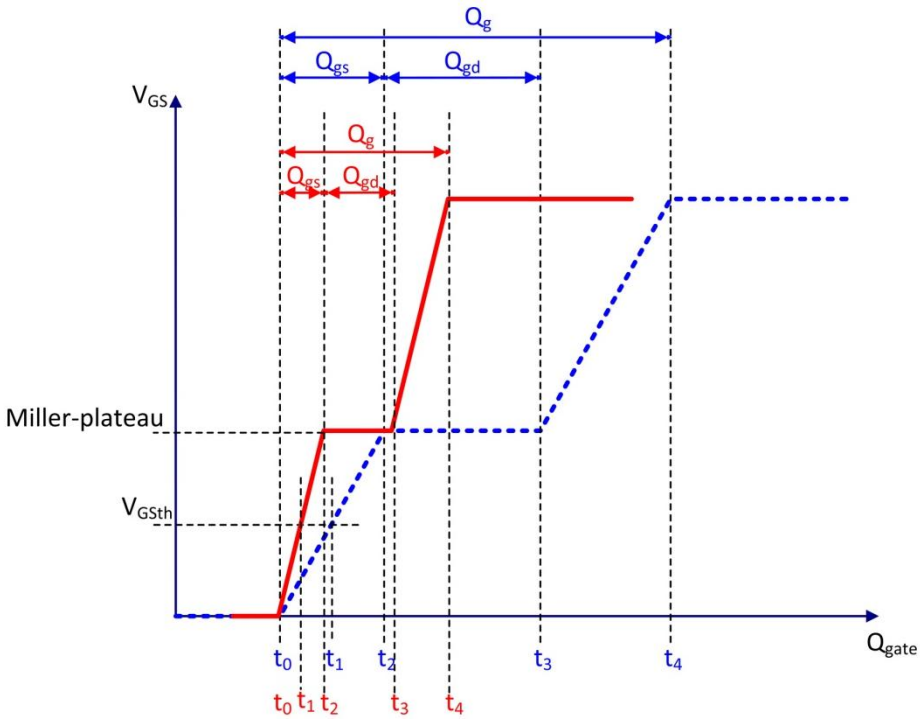

Figure 1: simplified gate charge

As visible in figure 1 due to a reduced gate charge it is possible to switch ON and OFF the device faster or reach the same performance with lower driver capability. The length of the Miller-plateau is dependent on the relation between the internal C_{GS}[14] and C_{GD}[15]. "In order to simplify the clarification of the Miller-plateau it is assumed that the voltage supply has a value of 400V and the gate driver is represented as a constant current source. During t_0 till t_2 the current from the gate driver is charging C_{GS} and discharging C_{GD}. Directly after t_2 the MOSFET switches ON and V_{DS} decreases to nearly 0V.

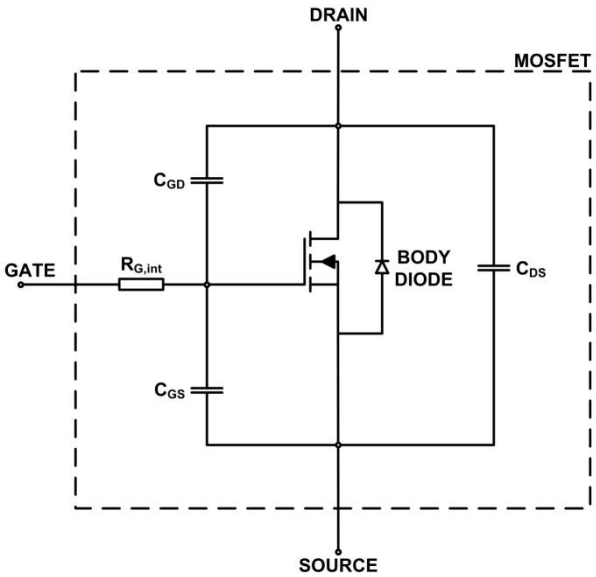

Figure 2: simplified small signal MOSFET equivalent circuit

At this time the V_{GS}[16] has the value of about 5V (this is an assumed value for easier description).During the period from t_2 to t_3 when V_{DS}[17] drops from a supply voltage of 400V, C_{GD} has to be discharged until the voltage over C_{GD} reaches -5V. Because C_{GD} is discharged from 395V to -5V a lot of energy is needed from the driver. For this reason C_{GS} cannot be charged due to the fact that nearly the whole current from the driver flows through C_{GD} until t_3. From t_3 to t_4 V_{DS} stays constant at nearly 0V and the current from the driver is able to charge C_{GS} until the defined voltage is reached."[1]

As mentioned before it is possible to switch the MOSFET ON and OFF faster, which leads to a wider window to achieve zero voltage switching. The next figure is going to represent this behavior in a theoretical way where only the Q_g is decreasing and all other characteristics of the same part stay the same.

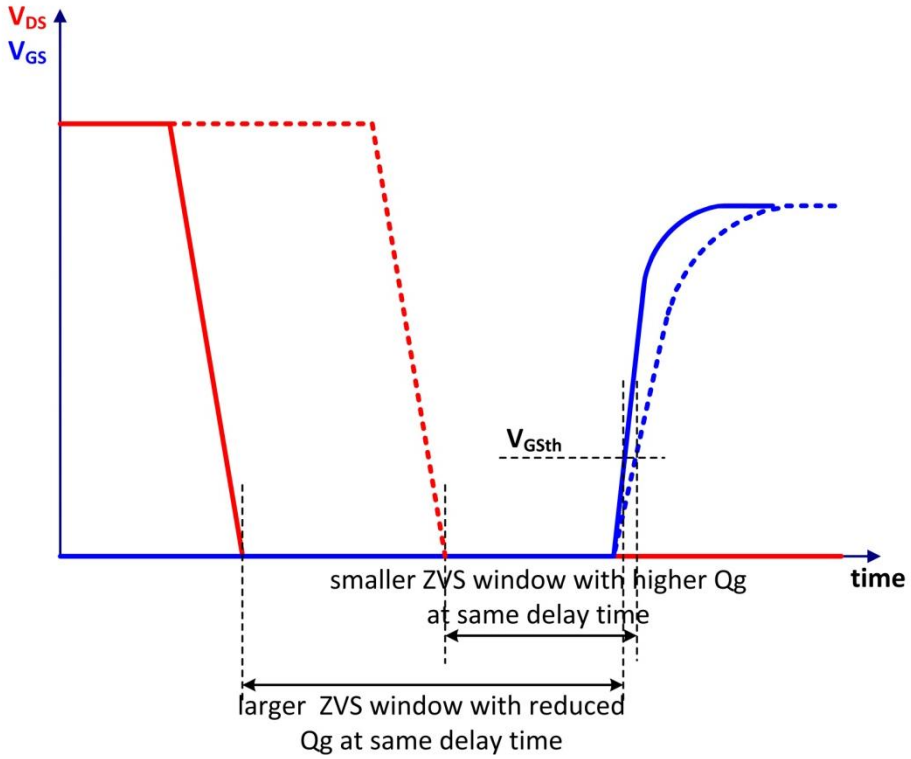

Figure 3: simplified ZVS window depending on Q_g at same delay time

This figure illustrates that with a lower Q_g a larger ZVS window is given with the same delay time at turning OFF. Due to this behavior it is also possible to decrease the delay time which also gives the benefit of a shortening of the conduction time of the body diode. For example, in a phase shifted full bridge this allows to use a higher duty cycle and therefore, an efficiency improvement.

The next figure shows the typical Q_g values of CFD2 in comparison to CFD according to the datasheet of the 80mΩ parts.

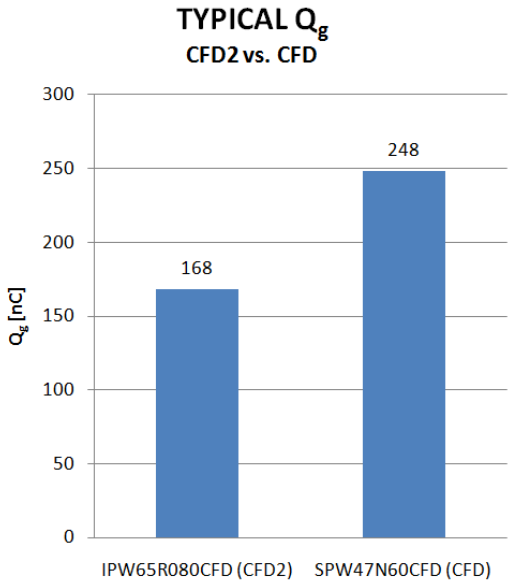

Figure 4: typical Q_g comparison CFD2 vs. CFD

It is shown that the typical value of the necessary gate charge is at about 80nC less on the CFD2. The effect of this lower Q_g is going to be represented in the measurements in chapter 4.

Additionally, the following diagram represents that CFD2 has about 30% lower Q_g in all $R_{DS(on)}$[18] classes compared to CFD.

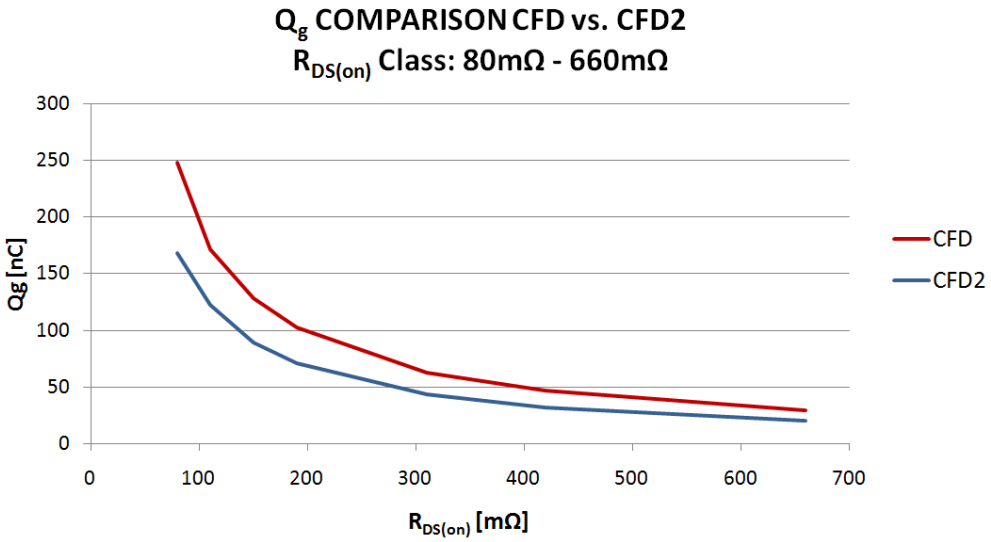

Figure 5: typical Q_g from 80mΩ to 660mΩ of CFD2 vs. CFD

3.3 REVERSE RECOVERY CHARGE, TIME AND CURRENT (Q_{rr}, t_{rr}, I_{rrm})

Compared to CFD, the Q_{rr} of CFD2 was further reduced. As consequence t_{rr}[19] is shortened and the maximum I_{rrm}[20] is also reduced which brings a higher margin in repetitive hard commutation of the body diode limited by the junction temperature which is allowed by the datasheet. The following figure shows the improved behavior of a lowered Q_{rr} in a theoretical way.

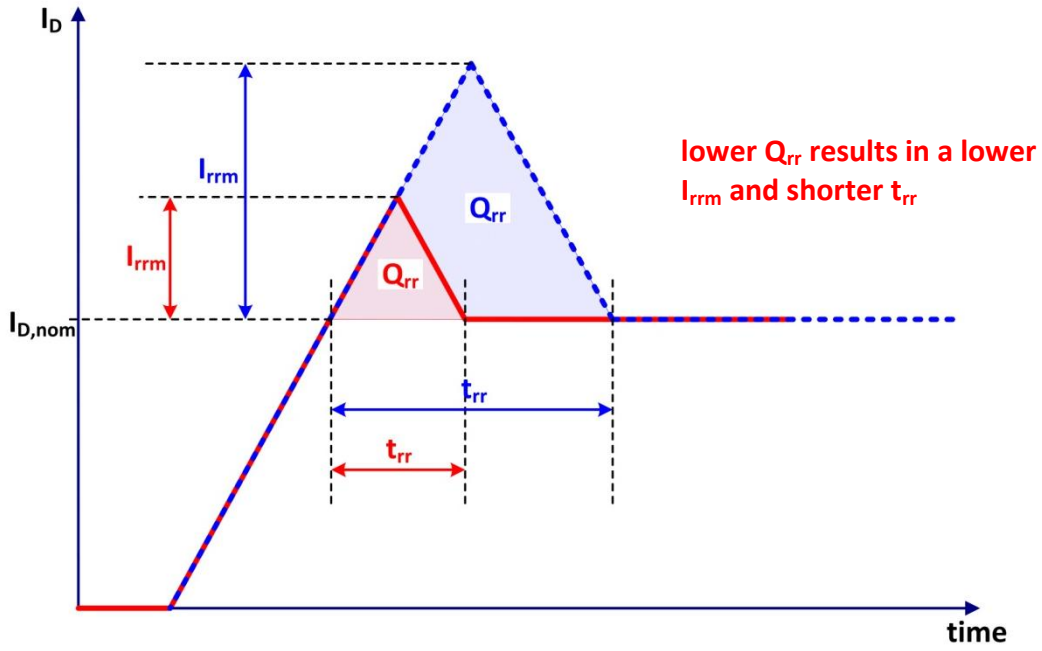

Figure 6: simplified I_D waveform depending on Q_{rr}, t_{rr}, I_{rrm}

The following diagram illustrates the Q_{rr} value of CFD2 in comparison to CFD and a competitor technology by showing the example of an 80mΩ product. It is visible that CFD2 has the lowest Q_{rr} values from 10A to 25A in a half bridge configuration with a supply voltage of 400V. The high side switch is used to load the inductance to the specified current. After switching OFF the high side MOSFET the current is commutating to the body diode of the low side MOSFET which corresponds to the device under test.

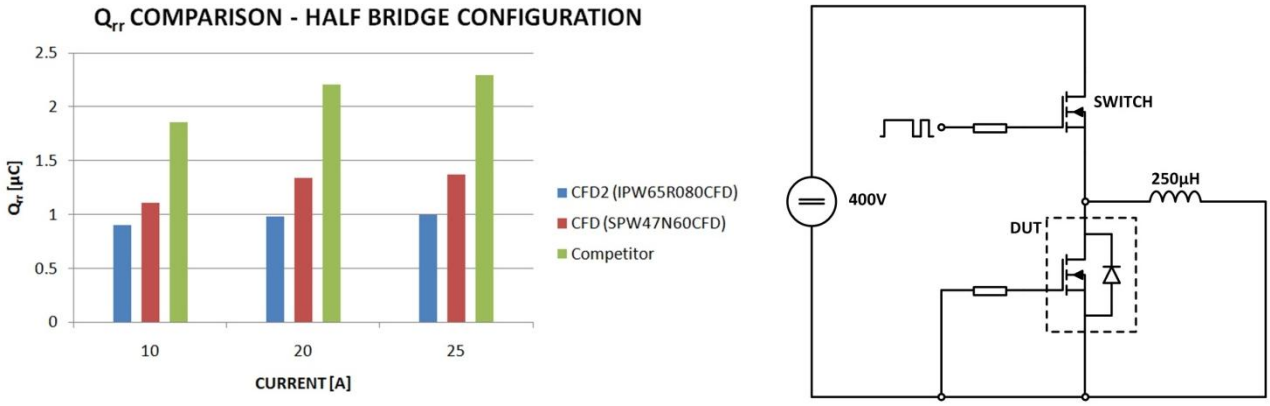

Figure 7: Q_{rr} comparison of low side MOSFET in a half bridge configuration

Furthermore, due to an improved production process of the CFD2 the maximum t_{rr} and Q_{rr} values will be given in the datasheet which results in a major benefit in the design of, e.g. HID lamp ballast applications, where the reduced Q_{rr} and t_{rr} is also of advantage. The following schematic represents a typical HID lamp ballast circuit.

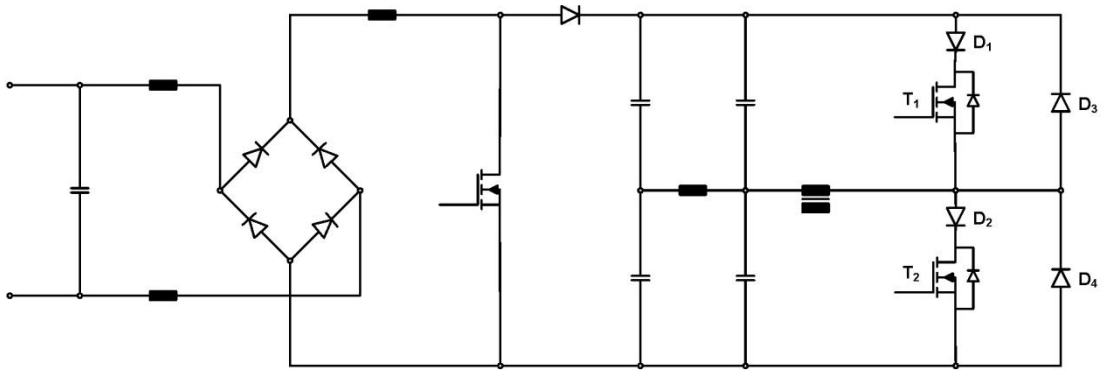

Figure 8: typical simplified HID lamp ballast circuit

Due to the non-optimized performance of the body diode of standard MOSFETs, D_1 and D_2 are used to override the body diodes of MOSFET T_1 and T_2 in the half bridge. For the current commutation it is now obligatory to implement fast or ultra fast diodes parallel to T_1 and T_2 because their t_{rr} is directly involved in the efficiency calculation. One of the main benefits of the lowered Q_{rr} of CFD2 is that it is possible to remove these four diodes and use the implemented body diode with even higher efficiency in the same setup. The main benefit is therefore the reduction of needed components, with advantages in term of cost and space available on the PCB[(21)].

The following table visualizes the measured efficiency values of the represented circuit.

Table 3: efficiency comparison HID lamp ballast

T_1, T_2 half bridge MOSFETs	D_1, D_2, D_3, D_4 diodes	Efficiency [%]
SPD07N60C3	all assembled	91,81
SPD07N60C3	not assembled (only body diode)	89,72
IPD65R660CFD	not assembled (only fast body diode)	92,81

Another very important behavior in an HID application is the long conduction phase of up to 2ms of the body diode of the MOSFET which lowers the losses with a lower Q_{rr}.

3.4 COMMUTATION BEHAVIOR

The behavior analyzed in chapter 3.3 brings a more stable and rugged behavior during commutation of the body diode. The following figure represents the maximum V_{DS} overshoot ($V_{DS,max}$[22]) which occurs during commutation when there is a voltage drop over inductances in the commutation loop due to a change in slope of the current through the body diode.

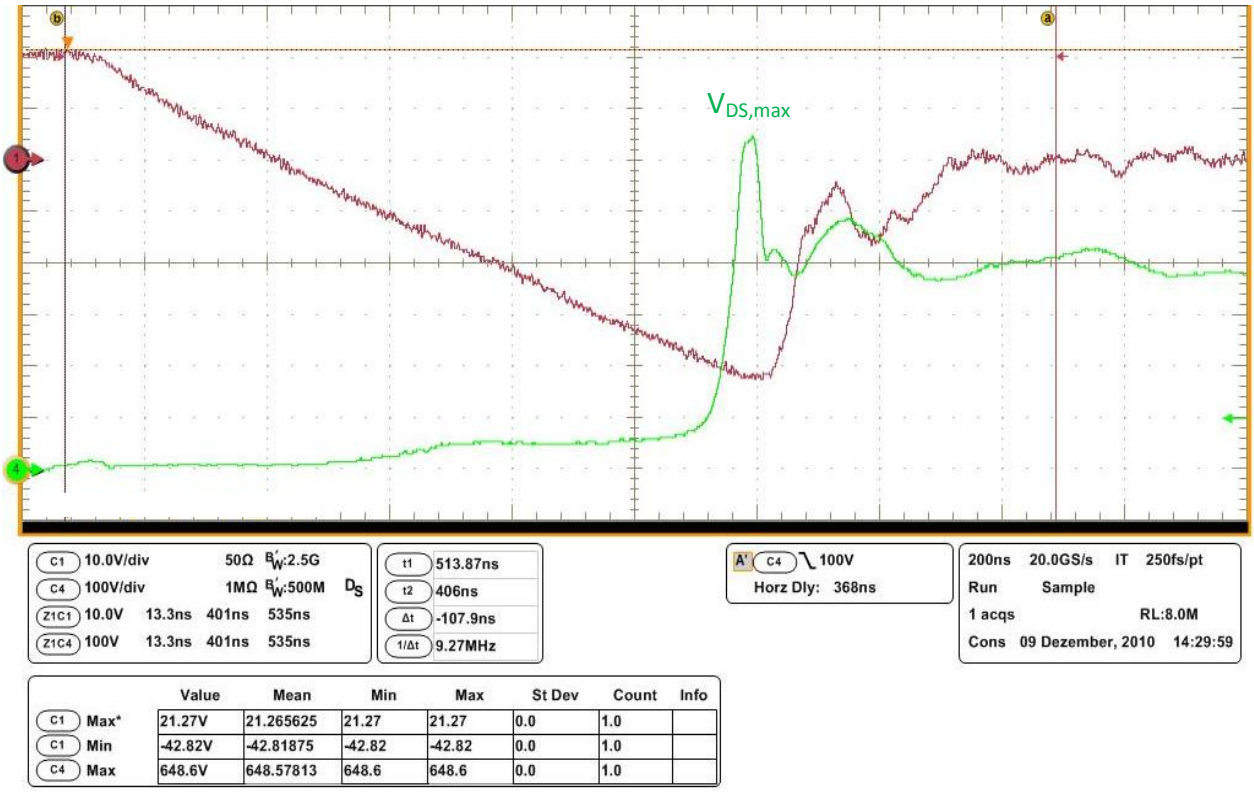

Figure 9: measured $V_{DS,max}$ in a half bridge configuration represented in figure 10 of the IPW65R080CFD

This waveform was acquired in a half bridge configuration where the low side MOSFET is the device under test which is shown in figure 10. This figure also illustrates the values of $V_{DS,max}$ of CFD2 in comparison to CFD and a comparable competitor product with a maximum $R_{DS(on)}$ of 80mΩ.

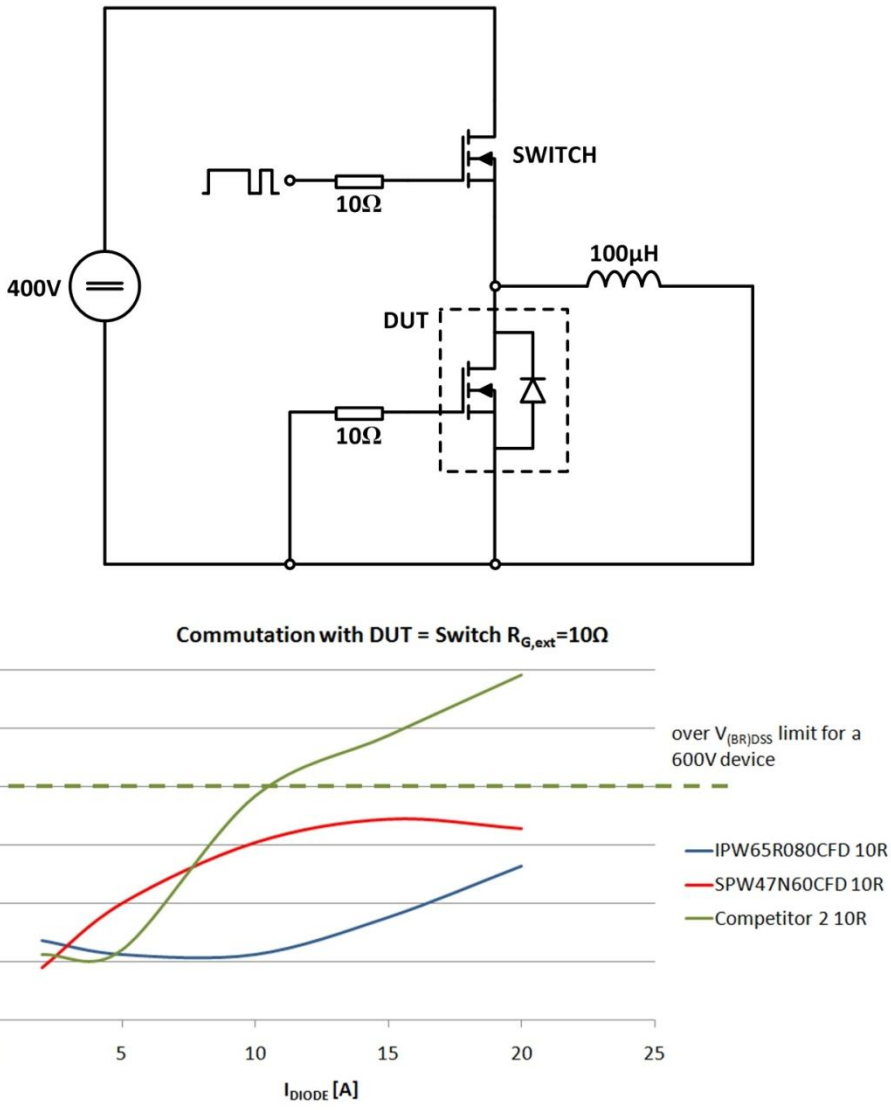

Figure 10: $V_{DS,max}$ comparison CFD2, CFD and Competitor 2

Figure 10 describes that even when reaching high loads (20A) the CFD2 has a voltage peak of only at about 535V which is about 115V lower than the maximum breakdown voltage of 650V (only CFD2). As can be seen in the diagram the competitor product reaches at this about 700V at this high current which is 100V higher than the breakdown voltage of the product ($V_{(BR)DSS}$ = 600V) which could lead to the failure of the device.

3.5 SELF LIMITING di/dt AND dv/dt

CoolMOS™ CFD2 comes with an integrated gate resistor in order to achieve self-limiting di/dt and dv/dt characteristics. This integrated R_G allows fast turn ON and turn OFF at normal operating current conditions but limits the di/dt and dv/dt in case of peak current conditions. The values of integrated R_G[23] scales inversely with the gate charge respectively device capacitances.

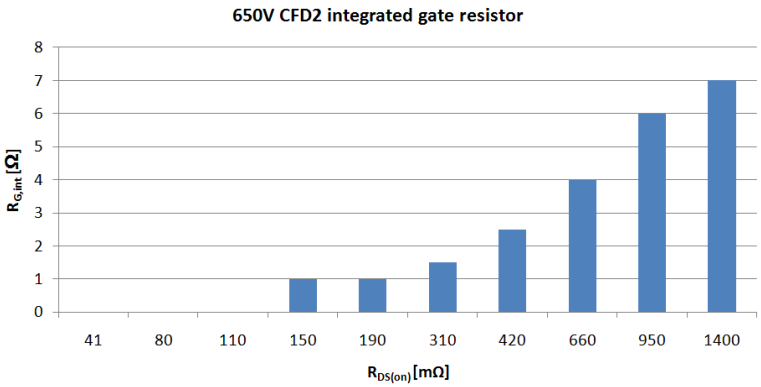

Figure 11: integrated gate resistor for CoolMOS™ CFD2

Please note that the CFD2 devices with $R_{DS(on)}$ values below 150mΩ come with no integrated gate resistances. Low $R_{DS(on)}$ values require larger silicon area and thus exhibit larger device capacitances. For those parts it is not necessary to additionally limit the di/dt and dv/dt values. Low ohmic CFD2 parts are therefore ideally suited for applications with highest efficiency requirements, like e.g. solar inverters.

The C6 has defined “ease of use” requirements which provide a stable switching behavior Due to its self limiting behavior the C6 technology can be easier implemented in a parasitic layout environment. These ease of use requirements are the C_{rss}[24] of C6 is close to C3 level and the implementation of an internal gate resistor brings the advantage of a stable switching and switching losses are comparable to C3. As the CFD2 is based on the C6 technology, it also shows a stable and self-limiting switching behavior and is easy to design-in, even in layouts that are not optimized with respect to their parasitic environment.

The following diagrams represents the di/dt and dv/dt of CFD2 at turn ON and OFF at different $R_{G,ext}$[25].

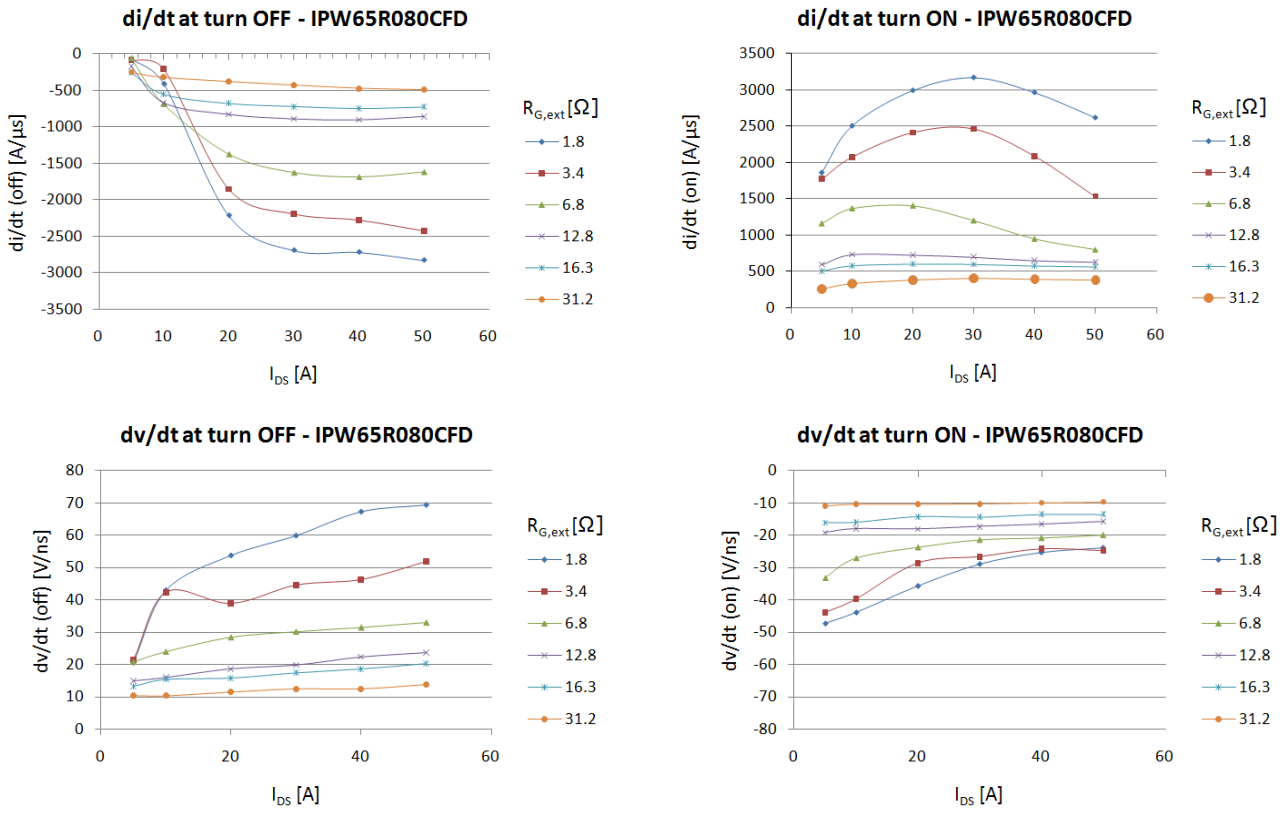

Figure 12: di/dt and dv/dt measurements for CoolMOS™ CFD2

After the analysis of the most important improvements this application note is going to describe some measurements of CFD2 in a target application, the ZVS phase shifted full bridge.

4. MEASUREMENTS ON A ZVS PHASE SHIFTED FULL BRIDGE (REFERENCE DESIGN)

"The ZVS exploits the parasitic circuit elements to guarantee zero voltage across the switching device before turn ON, eliminating hence any power losses due to the simultaneous overlap of switch current and voltage at each transition."[2] This chapter will describe the principal operation of the ZVS phase shifted full bridge and compare efficiency and transition time of the CFD2 versus CFD.

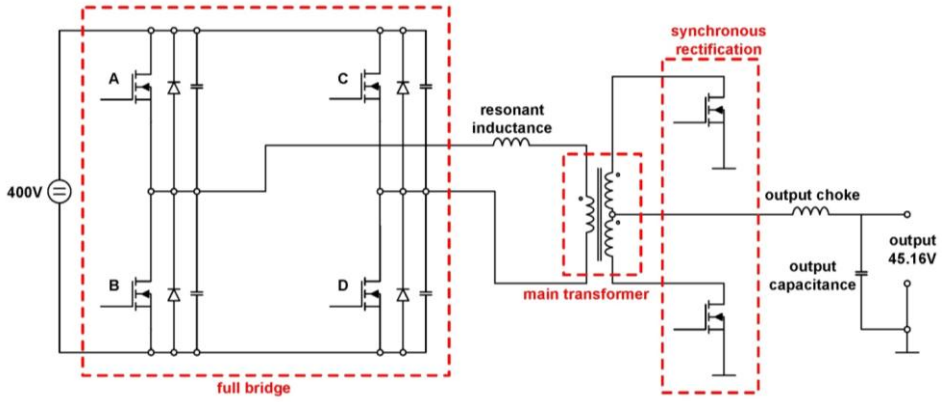

Figure 13: simplified circuit of the ZVS phase shifted full bridge

Figure 13 shows the main parts of the ZVS phase shifted full bridge. The primary side including the full bridge (MOSFET A, B, C, D) in which the usage of CFD2 will be analyzed. Furthermore, the resonant inductance which is necessary to have enough energy stored in the system to reach zero voltage switching and the primary windings of the main transformer. In the used setup the main transformer has a winding partitioning of 18 turns on the primary side and 3 plus 3 turns with a center tap on the secondary side. The synchronous rectification is done with two paralleled 200V MOSFETs from the OptiMOS™ product line. Additionally the output choke with about 10mH inductance can also be decreased (this choke is now a little bit over dimensioned to decrease the current ripple to a minimum) to reduce the copper losses and the output capacitance is represented. This stage is a DC/DC converter from 400V to 45V which is minimum output voltage in a typical application for telecom servers. All the measurements and comparisons are done with the IPW65R080CFD and SPW47N60CFD in the full bridge (MOSFET A, B, C, D).

First the overall efficiency of the whole converter will be analyzed. As visible in figure 14 it is possible to reach efficiency values up to about 94.6% at 45V output when the synchronous rectification is not activated. The efficiency measurements have been performed in this way in order to be independent from the delay time control between the primary and secondary switches, which strictly depends on the characteristics of primary devices used in each test. So, in order to see only the difference on the efficiency due to the different parts used in primary full bridge, it was obligatory only to use the body diodes for rectification.

This system efficiency has currently the highest value which can be achieved with the CFD2. Two ways are possible to improve the efficiency: using a new transformer with better primary-secondary coupling, which will reduce the peak on synchronous rectification MOSFETs, allowing the use of 150V rating for them, with reduced $R_{DS(on)}$ losses. Additionally the output choke with about 10mH inductance can also be decreased (this choke is now a little bit over dimensioned to decrease the current ripple to a minimum) to reduce the copper losses and the output capacitance is represented.

The resonant inductance is dimensioned in order to achieve the best compromise between reaching ZVS at light load and copper losses impacting on the high load efficiency.

The comparative tests have been performed on a platform with V_{OUT}[26]=45.16V and P_{OUT}[27]=1400W.

Further efficiency increase can be realized by increasing the output voltage, increasing the windings of the main transformer to 22 on the primary and 4 plus 4 on the secondary side is a way to achieve a higher duty cycle window available for the regulation.

Nevertheless, current test platform is anyway valid to make a comparative analysis and show main differences between the technologies.

The following figure represents the efficiency of the whole system. The measurement was done in the following way:

1) set the delay times for A/B (figure 13) and C/D (figure 13) to optimize efficiency for CFD and measure efficiency
2) plug in CFD2 in the CFD optimized setup
3) readjust delay times to optimize setup for CFD2
4) implement the synchronous rectification in the CFD2 optimized setup

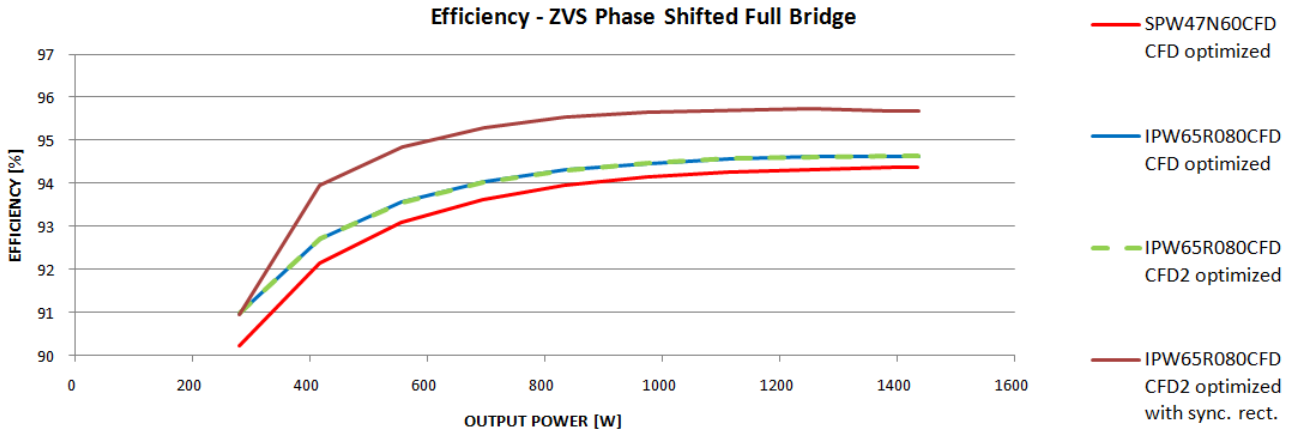

Figure 14: efficiency comparison CFD2 vs. CFD in ZVS phase shifted full bridge (figure 13)

The main difference in the efficiency is given by the lower Q_g of CFD2 which was mentioned in chapter 3.2. The overall efficiency improvement is mainly due to the fact that, at V_{DRIVER}[28]=12V, CFD needs about 32.5mA more current from the gate drive for each MOSFET of the full bridge, that means 130mA for the full bridge. At V_{DRIVER}=12V, this brings 1.56W more losses over the whole operation area.

This result can be also theoretically achieved by calculating the driving losses as function of Q_g by:

$$P_{DRIVING}{}^{(29)} = 2 \cdot Q_g \cdot V_{DRIVER} \cdot f_{sw}{}^{(30)}$$

Where Q_g=168nC for CFD2 and 322nC for CFD (these values correspond to the parameters directly measured on characterized parts), so

$P_{DRIVING}$=1.6128W for CFD2 and 3.0912W for CFD, from this calculation the difference in driving losses is 1.4784W.

The next figure describes the V_{DS} transition time at 7.47A and 1.05A primary current which correspond to the time difference between 90% and 10% of V_{DS}.

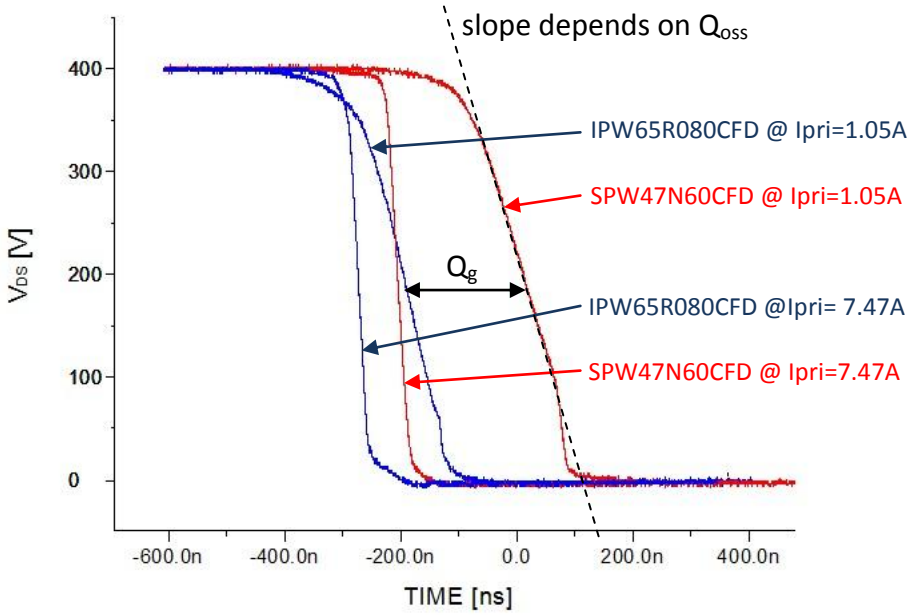

Figure 15: V_{DS} transition time of the low side MOSFET (D) on the primary side of the ZVS phase shifted full bridge (figure 13). Comparison IPW65R080CFD (blue) vs. SPW47N60CFD (red) at different loads

For all technologies, the V_{DS} transition time is independent on R_G and mainly depends on the Q_{oss}[31]. Therefore, it is decreasing with increasing load.

In our case, the V_{DS} transition time is a little bit lower for CFD. This is due to the lower Q_{oss} of CFD compared to CFD2. This lower Q_{oss} can be negligible because firstly there is only a slight influence at low loads (when there is enough energy in the system the advantage of faster removing the charge of the output capacitance of the MOSFET does not exist anymore), secondly the impact of the driving losses is much higher.

On the other hand, for all technologies, t_{d_off}[32] increases with increasing $R_{G\_turn\text{-}off}$[33] and decreases with increasing load. In fact, at very light load, the contribution of V_{DS} transition (from 10% to 90%) is predominant rather than R_G. As soon as the load is increasing, the contribution of R_G becomes more important. So at light load, the turn off time duration is also influenced by Q_g, in fact it is lower for CFD2 compared to CFD, giving benefit in ZVS design at light load.

Furthermore with the CFD2 it is visible that the time window between high load and light load is much narrower than with the CFD.

5. PRODUCT PORTFOLIO AND NAMING SYSTEM

650V CoolMOS™ C6 CFD2 series follows the same naming guidelines as already established with the CP series e.g. IPW65R080CFD:

I … Infineon Technologies
P … power MOSFET
W … package type (TO-247)
65 … voltage class divided by 10
R080 … on-state resistance in milli Ohms
CFD … name of the series

RDS(on) [mΩ]	RG,int [Ω]	 DPAK (TO252)	 D²PAK (TO253)	 TO220FP (TO220)	 TO220 (TO220)	 I²PAK (TO263)	 TO247 (TO247)
1400 mΩ	7 Ω	IPD65R1K4CFD					
950 mΩ	6 Ω	IPD65R950CFD					
660 mΩ	4 Ω	IPD65R660CFD	IPB65R660CFD	IPA65R660CFD	IPP65R660CFD	IPI65R660CFD	IPW65R660CFD
420 mΩ	2.5 Ω	IPD65R420CFD	IPB65R420CFD	IPA65R420CFD	IPP65R420CFD	IPI65R420CFD	IPW65R420CFD
310 mΩ	1.5 Ω		IPB65R310CFD	IPA65R310CFD	IPP65R310CFD	IPI65R310CFD	IPW65R310CFD
190 mΩ	1 Ω		IPB65R190CFD	IPA65R190CFD	IPP65R190CFD	IPI65R190CFD	IPW65R190CFD
150 mΩ	1 Ω		IPB65R150CFD	IPA65R150CFD	IPP65R150CFD	IPI65R150CFD	IPW65R150CFD
110 mΩ	-		IPB65R110CFD	IPA65R110CFD	IPP65R110CFD	IPI65R110CFD	IPW65R110CFD
80 mΩ	-						IPW65R080CFD
41 mΩ	-						IPW65R041CFD

Figure 16: product portfolio

6. LIST OF ABBREVATIONS

(1)	…	CFD	CoolMOS™ Fast Diode	Page	4
(2)	…	MOSFET	Metal Oxide Semiconductor Field Effect Transistor	Page	4
(3)	…	Q_g	gate charge [3]	Page	4
(4)	…	$t_{rr,max}$	maximum reverse recovery time [3]	Page	4
(5)	…	$Q_{rr,max}$	maximum reverse recovery charge [3]	Page	4
(6)	…	ZVS	Zero Voltage Switching	Page	4
(7)	…	HID	High Intensity Discharge	Page	4
(8)	…	LED	Light Emitting Diode	Page	4
(9)	…	Q_{rr}	reverse recovery charge [3]	Page	5
(10)	…	$T_{junction}$	junction temperature of a MOSFET [3]	Page	5
(11)	…	C3	CoolMOS™ technology	Page	5
(12)	…	C6	CoolMOS™ technology	Page	5
(13)	…	$V_{(BR)DSS}$	drain-source-substrate breakdown voltage [3]	Page	5
(14)	…	C_{GS}	internal gate source capacitance $C_{GS}=C_{iss}$ (34) $-C_{rss}$	Page	6
(15)	…	C_{GD}	internal gate drain capacitance $C_{GD}=C_{rss}$	Page	6
(16)	…	V_{GS}	gate source voltage	Page	7
(17)	…	V_{DS}	drain source voltage	Page	7
(18)	…	$R_{DS(on)}$	drain-source on-state resistance [3]	Page	8
(19)	…	t_{rr}	reverse recovery time [3]	Page	9
(20)	…	I_{rrm}	maximum reverse recovery current [3]	Page	9
(21)	…	PCB	Printed Circuit Board	Page	10
(22)	…	$V_{DS,max}$	maximum measured drain source voltage	Page	11
(23)	…	R_G	gate resistor	Page	13
(24)	…	C_{rss}	MOSFET reverse transfer capacitance $C_{rss}=C_{GD}$ [3]	Page	13
(25)	…	$R_{G,ext}$	external gate resistor	Page	14
(26)	…	V_{OUT}	output voltage	Page	16
(27)	…	P_{OUT}	output power	Page	16
(28)	…	V_{DRIVER}	gate drive voltage	Page	17
(29)	…	$P_{DRIVING}$	gate drive power	Page	17
(30)	…	f_{sw}	switching frequency	Page	17
(31)	…	Q_{oss}	output charge	Page	17
(32)	…	t_{d_off}	switching OFF delay time	Page	17
(33)	…	$R_{G\_turn-off}$	gate resistance at turning OFF the device	Page	17
(34)	…	C_{iss}	MOSFET input capacitance $C_{iss}=C_{gs}+C_{gd}$ [3]	Page	19

7. REFERENCES

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[2] … L. Saro, et al., “High-Voltage MOSFET Behavior in Soft-Switching Converter: Analysis and Reliability Improvements”, International Tel-communication Conference, San Francisco, 1998. Page 14

[3] … IPW65R080CFD preliminary datasheet, rev. 1.0 Page 19