CoolMOS™ C7: Mastering the Art of Quickness
A Technology Description and Design Guide

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1 Introduction

This application note describes the characteristics of CoolMOS™ C7, the newest high voltage superjunction MOSFET technology from Infineon, which features major advances in component metrics and achievable application performance. CoolMOS™ C7 will be described in reference to existing CoolMOS™ generations from a technology viewpoint, and also with respect to application performance. Application guidelines will be given for achieving high performance in standard hard switching SMPS topologies with robust designs with safe operation.

2 Towards the ideal 650V silicon MOSFET switch: superjunction (SJ) principle

For conventional high-voltage MOSFETs, the voltage blocking capability in the drain drift region is developed through the combination of a thick epitaxial region and light doping. This results in about 95% of the device resistance in the drain region, which cannot be improved by the approaches used for low-voltage transistors (trench cells with smaller cell pitch), where only about 30% of the transistor resistance is in the drain drift region.

The intrinsic resistance of a conventional epitaxial drift region of optimum doping profile for a given blocking voltage class is shown in Figure 2 as the "silicon limit line," which, in the past, has been a barrier to improved performance in high-voltage MOSFETs. Chen and Hu theoretically derived this limit line in the late 1980's [1]. This aspect of MOSFET design and physics limited achievable performance until the introduction of CoolMOS™ by Siemens (now Infineon), the first commercially available superjunction MOSFETs [2,3].
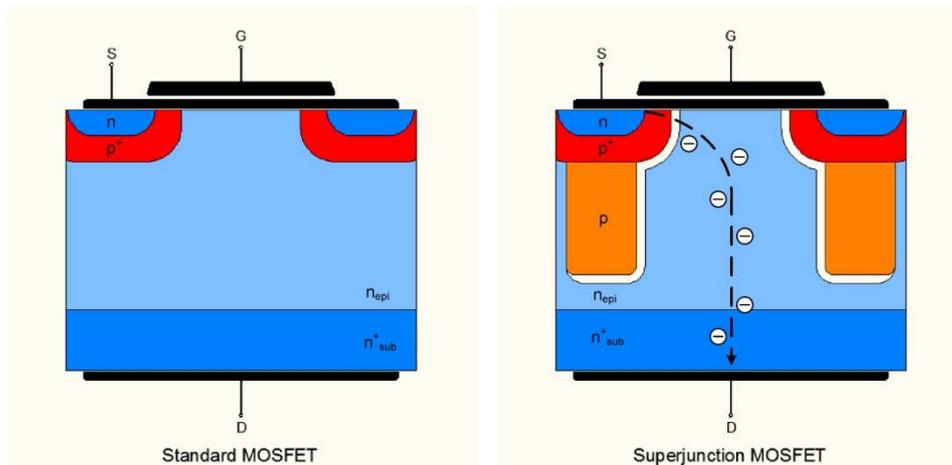
Figure 1: Conventional HV planar MOSFET and superjunction MOSFET cross section

In 1999, CoolMOS™ first employed a novel drain structure employing the superjunction concept (Figure 1).

There are two key principles employed in this transistor design. First, the main current path is much more heavily doped than for a conventional high-voltage MOSFET. This lowers the on-state resistance. But without the p-columns forming a charge compensation structure below the cell structure the transistor would have a much lower blocking voltage capability due to the highly doped n-region. The precisely sized and doped p-columns constitute a "compensation structure", which balances the heavily doped current path and supports a space charge region with zero net charge supporting high blocking voltage.
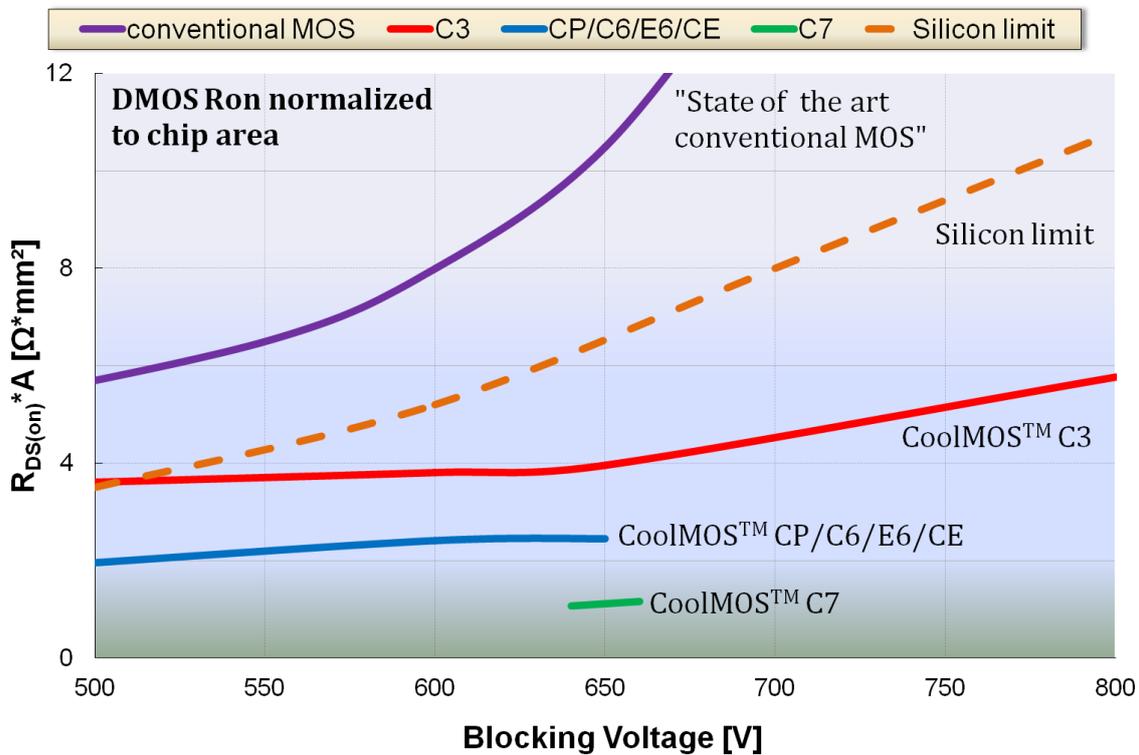
Figure 2: Silicon Limit line and area specific R$_{DS(on)}$ versus blocking voltage capabilities of CoolMOS™ C3, CP, C6, E6, CE and C7 compared noting advances with subsequent generations

This construction enables a reduction in area specific resistance which has obvious conduction loss benefits - the attendant remarkable reduction in chip area for the first generation of CoolMOS™ technology lowered capacitance and dynamic losses as well through the reduction of chip area and capacitance. This technology made it possible to "beat" the silicon limit line (Figure 2) and, with a new finer pitch generation in CoolMOS™ CP, to further improve all aspects of losses [4,5].

This MOSFET technology approach has now been further extended with the development of CoolMOS™ C7, which reduces the typical area specific R$_{DS(on)}$ down below the 1 Ω*mm^2 level for the first time. Together with several cell geometry considerations, this reduces all device capacitances, thus improving the switching related Figures of Merit (FOM) and application performance characteristics substantially as described in the next chapters.

CP structure **C7 structure**
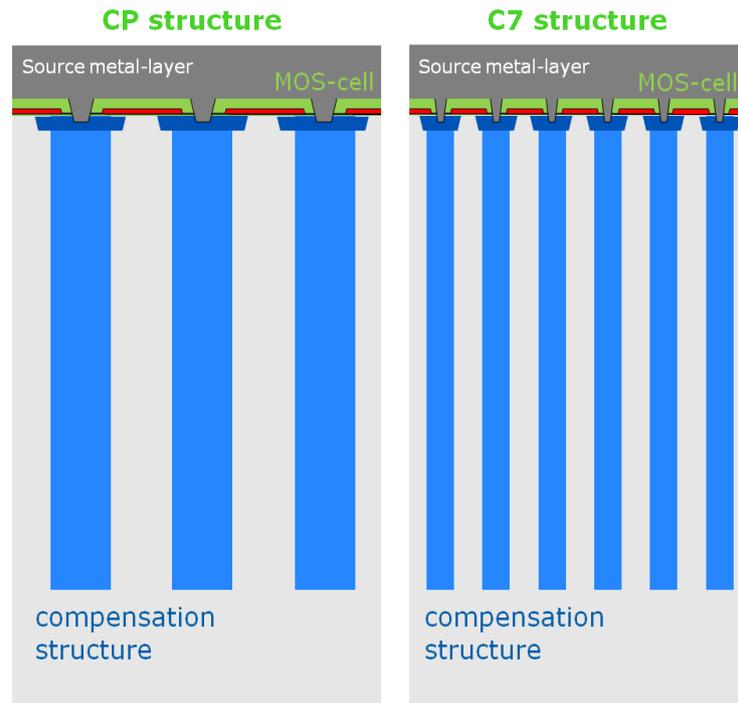
Figure 3: Schematic comparison of CoolMOS™ CP and C7 cross section concepts with high aspect ratio compensation structure

Figure 3 depicts the schematic cell cross-section and compensation structure comparison between CP (left) and C7 (right). This configuration poses significant manufacturing challenges and drew upon process technology experience from a number of areas at Infineon in developing a new approach for this generation of CoolMOS™ but brings considerable technological benefits which are described below.

3 Technology comparison of CoolMOS™ CP, C6, and C7

3.1 Electrical characteristics: General Overview

To make an optimum MOSFET selection for the application and apply it successfully, it is useful to first have a clear understanding of the technology differences to its predecessors. The most obvious advantage of CoolMOS™ C7 is the substantially improved area specific R_{ON} (Table 1) or one can also consider that C7 needs only one half of the chip active area compared to previous generations to achieve a given $R_{DS(on)}$ class. The consequence is then two-fold:

On the one hand, new Best-in-Class products with lower $R_{DS(on)}$ ratings are possible for the different packages, for example 19 mΩ in TO-247 and 45 mΩ in TO-220. Additionally, this also means that certain maximum $R_{DS(on)}$ classes can be offered in packages with lower parasitic inductances, like TO-220 compared to TO-247, which for previous technologies were not possible due to their larger chip sizes. The reduction of the parasitic inductance in the gate driver loop delivers a positive side effect, the reduction of switching losses. Naturally, the possibility to choose smaller packages also supports improving the power density.

Specification	Symbol	IPW60R041C6	IPW60R045CP	IPW65R045C7
Max on State Resistance 25°C	$R_{DS(on)}$	41 mΩ	45 mΩ	45 mΩ
I_D Current Rating; *D=0.75	I_D	77.5 A*	60 A	46 A
I_D Pulse Rating	$I_{D, pulse}$	272 A	230 A	212 A
Area Specific R_{ON} (Ω*cm^2)	Ω*cm^2	24 mΩ*cm^2	24 mΩ*cm^2	10 mΩ*cm^2
Typical Gate to Source, Gate to Drain, Gate charge total	Q_{GS} Q_{GD} Q_G	36 nC 150 nC 290 nC	34 nC 51 nC 150 nC	23 nC 30 nC 93 nC
Typical C_{iss}	C_{iss}	6530 pF	6800 pF	4340 pF
Typical C_{rss} @ 400V	C_{rss}	33 pF	9.4 pF	12 pF
Typical C_{oss} @ 400V	C_{oss}	130 pF	220 pF	70 pF
E_{oss} @ 400V	E_{oss}	22 µJ	28 µJ	12µJ
Typical Effective output capacitance Energy related	$C_{o(er)}$	235 pF	310 pF	146 pF

Table 1: Comparison of CoolMOS^{TM} C6, CP, and C7 for similar $R_{DS(on)}$ ratings

On the other hand, the reduction of the chip size yields a reduction of the intrinsic device capacitances, which has a very positive impact on the switching key parameters which, together with other design considerations, have optimized C7 for fast switching, providing at the same time lowest switching losses and better ease of use than CP

The improvements in dynamic characteristics of C7 are also substantial but require some thought in the application, as did the transition from conventional MOSFETs to the first CoolMOS™ and the introduction of CoolMOS™ CP. The coming sections will address their discussion correspondingly.

3.2   The gate charge improvement

The gate charge improvement of CoolMOS™ C7 is addressed, on the one hand, by means of the reduction of the input capacitance (C_{iss}) in approximately 33% compared to previous generations for a given on-resistance class and, on the other hand, by a reduction of the gate drain capacitance (C_{GD} or C_{rss}) with a particular profile as a function of the drain-source voltage.

As it can be observed in Figure 4, C7 shows an overall lower C_{rss} value than the previous generations. Moreover, the design properties of CoolMOS™ C7 allow that the characteristic capacitance drop of the superjunctions takes place at lower voltages. Both aspects combined reduce the gate-drain charge (Q_{GD}) remarkably, even compared to a fast technology like CP. Furthermore, due to the reduction in C_{rss} turn off delay time is reduced and a gate speedup resistor for turn off is not needed. This simplifies the gate driver circuit and reduces its power consumption.
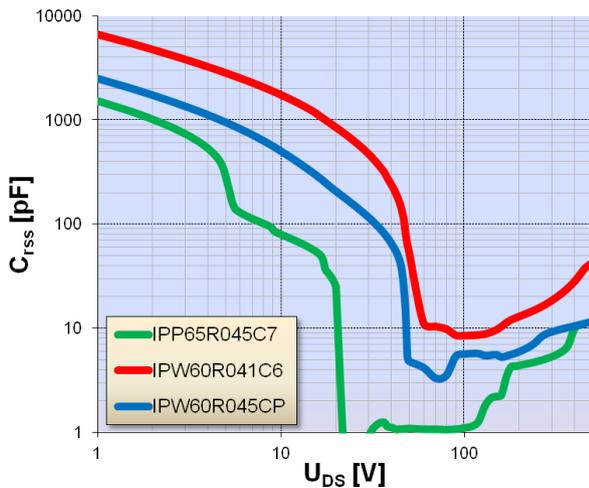
Figure 4: C_{rss} as a function of V_{DS} for C6, CP and C7 in the $R_{DS(on)}$ class of 41-45mΩ.
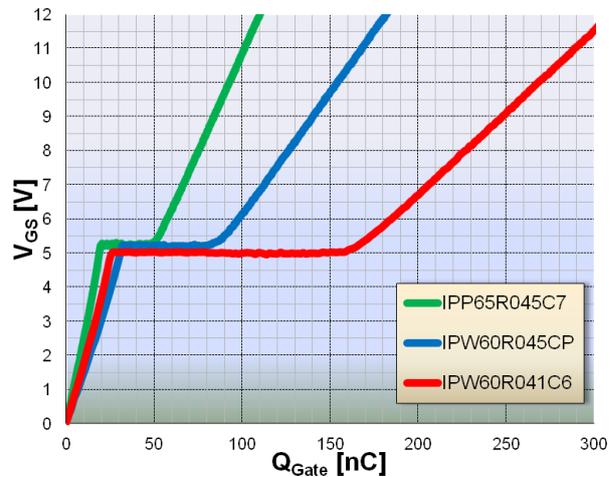
Figure 5: Gate charge comparison @520V for 41-45mΩ CoolMOS™ C6, CP and C7

The combination of both brings the total gate charge level (Q_G) of C7 to less than one third of the C6 charge and leaves the so far fastest generation, CoolMOS ^{TM} CP, with 50% higher Q_G than C7. This can be observed in Figure 5, where the C_{iss} improvement gets reflected as a higher slope in the gate charge curve and the Q_{GD} reduction in the much shorter length of the Miller Plateau compared to previous generations.

The reduced gate charge level is an indication of the improvement of the gate driving related losses as well as of the MOSFET switching losses. However, the latter requires a more detailed description in terms of the capacitance profiles which will be addressed in the coming blocks of this application note.

3.3   The E_{oss} improvement

As already discussed for C_{rss}, as well as for the output capacitance (C_{oss}), the capacitance drop of C7 takes place at lower voltage levels than in previous generations. This, combined with a remarkable reduction of the C_{oss} level at high voltages, which dominates the overall value of the energy stored in the output capacitance, brings the E_{oss} at typical DC link voltages down to roughly one half of the previous generations (see Figure 7). This energy is a fixed contribution to the switching losses in hard switching applications since, after getting stored in the turn-off phase, it gets transformed into losses in the next turn-on transient. This loss is especially significant at low currents where the other switching losses contributions decrease considerably and, thus, the E_{oss} reduction contributes to an improvement of the light load efficiency.
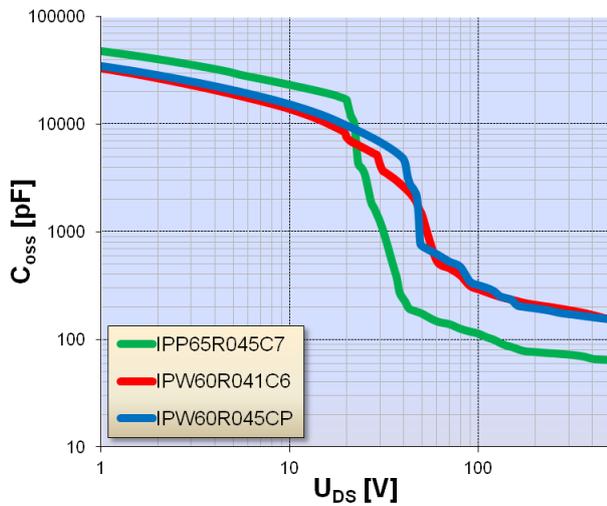
Figure 6: C_{oss} as a function of V_{DS} for C6, CP, and C7 CoolMOS™ in the $R_{DS(on)}$ class of 41–45mΩ.
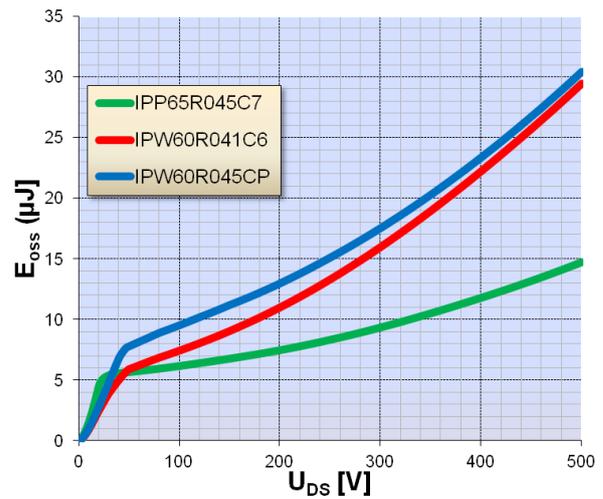
Figure 7: E_{oss} as a function of V_{DS} for C6, CP, and C7 CoolMOS™ in the $R_{DS(on)}$ class of 41–45mΩ.

3.4 The improvement of the capacitance profiles

The previous C_{rss} and C_{oss} comparisons in Figure 4 and Figure 5 are very illustrative of the technology differences between these generations of CoolMOS™ and indirectly highlights the steps needed to achieve lower area specific $R_{DS(on)}$. Lowering the on state resistance fundamentally requires increasing doping of the n-region current path and particularly CoolMOS™ C7 uses a much higher doping level than earlier generations. On the other hand, in order to do this, the cell pitch must be correspondingly reduced so that the zero net charge region can still be formed to achieve the desired high blocking voltage. As a result the overall column aspect ratio of height to width becomes much higher and the capacitance step of the C_{oss} and C_{rss} curves moves to a lower voltage.

This can be easily understood by means of a visualization of the space charge region during turn-off at two different drain to source voltages as an aid in understanding the influence on the shape, thickness, and area of the space charge region and how this affects C_{oss} directly, and C_{rss} indirectly.
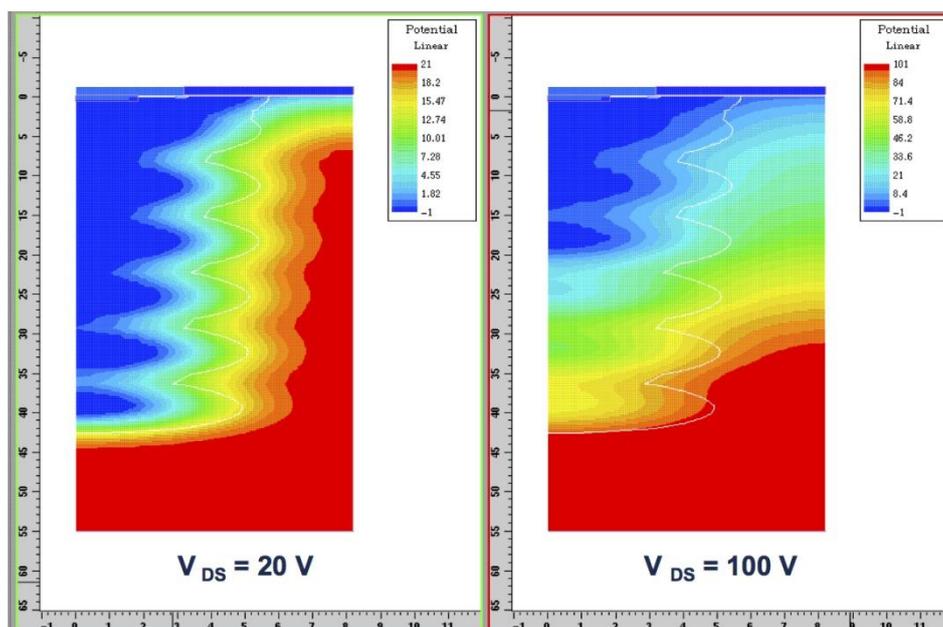
Figure 8: Comparison via Tarus-Medici simulator of space charge depletion layer around compensation structure columns at V_{DS}=20V and V_{DS}=100V for CoolMOS™ C3

Figure 8 illustrates the electric field potential of a superjunction MOSFET, in this case for CoolMOS™ C3 as an example, calculated by means of Taurus-Medici 3D device simulation for two different drain to source voltages, 20V and 100V. The potential lines are shown by color graduations around one half of the p-column compensation structure in the drain epi. In the case of low voltages, left side of the figure, it can be observed that the net space charge thickness is relatively small, compared with the column structure and cell pitch, and that the space charge region folds around the p-columns, thus resulting in a large effective area for the output capacitance. These two factors contribute to the high value of C_{oss} at low voltages. In the case of high voltages, right side of the figure, the shape of the space charge region begins to get transformed, first going through a wavy form following the compensation structures, into a horizontal capacitor with a lower effective area and a larger thickness. Therefore, the output capacitance at high voltages gets reduced in two orders of magnitude.

The capacitance step in the C_{oss} curve, and similarly also in C_{rss}, occurs exactly at the transition of the two states described above.

As observed in the previous subsections for CP and C6 this transition occurs in the region of 40-50V. For the new C7 technology, the complete depletion of the region of the compensation structures, thanks to the remarkable reduction of the pitch distance, can already take place in a more strongly non-linear fashion at a much lower voltages, approximately 20V.

The non-linearity in the capacitance characteristics, even more pronounced with the CoolMOS™ C7 transistors, rather than being a drawback, contributes to achieve low switching losses, especially in hard switching applications. This combination of FOM improvement, very low gate charge, and low output capacitance results in the capability to switch at high voltages in just a few nanoseconds.

For this reason, the dv/dt limit of CoolMOS™ C7 was extended to 100V/ns compared with 50V/ns for the previous generations.

4 Benefits of C7 in the switching losses and the overall efficiency

4.1 Switching losses of CoolMOS™ C6, CP and C7
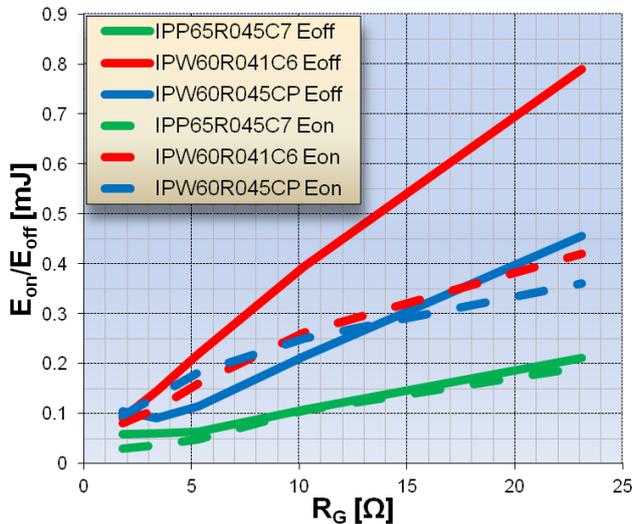
Figure 9: E_{on} and E_{off} for varying R_G at I_D=25A, V_{DS}=400V, V_{GS}=12V, and a range of R_G from 1.8 to 3Ω

The switching losses at turn-on (E_{on}) and at turn-off (E_{off}) drop considerably for C7 compared with C6 and even CP thanks to the technological improvements explained in the previous sections. Figure 9 shows the characterization results of E_{on} and E_{off} measurements for CoolMOS™ C7, CP, and C6 made with 25A drain current load, V_{GS}=12V, V_{DS}=400V, and a range of gate resistor R_G from 1.8Ω to 23Ω. A 600V SiC Schottky diode (IDH12SG60C) was used as the load clamping diode, to minimize the application circuit contribution to the turn-on losses.

All technologies showed the expected losses increase as a function of the gate resistance but C7 shows a clearly lower value for both the E_{on} and the E_{off} losses over the whole R_G range, especially at high values.

These results show the potential to achieve very low switching losses in SMPS applications since faster switching speed with low gate drive power is now possible.

4.2 The trade-off between switching losses and conduction losses

The significance of the balance between area-specific conduction and switching losses for high voltage transistors becomes increasingly important since higher power density is sought through higher efficiency (lower losses) and higher switching frequencies (to reduce passive component size). Higher load currents and lower switching frequency can shift the loss balance point (where conduction and switching losses are roughly equal) for area specific losses in a given MOSEFT technology, but in all cases, MOSFETs with better area-specific $R_{DS(on)}$ and lower capacitance, if used properly, can deliver the lowest losses in high density power systems.

Figure 10, Figure 11 and Figure 12 show the calculation based on the switching losses (simplified to its E_{oss} contribution),

$$P_{Eoss} = f * Eoss$$ **Equation 1**

where f is the applied frequency, and the conduction losses (calculated for a junction temperature of 105°C) for different power levels and at 90VAC input voltage and 176VAC input voltage, which correspond to duty cycles (D) of 0.775 and 0.56 respectively,

$$P_{cond} = I_d{}^2 * R_{DS(on)} * D \qquad\qquad \textbf{Equation 2}$$

for the different technologies devices CP, C6, and C7. This simplified comparison omits contributions related to the gate driver, external and internal gate resistance, effective switching time and package inductance, and focuses just on the unavoidable losses intrinsic to the silicon device.
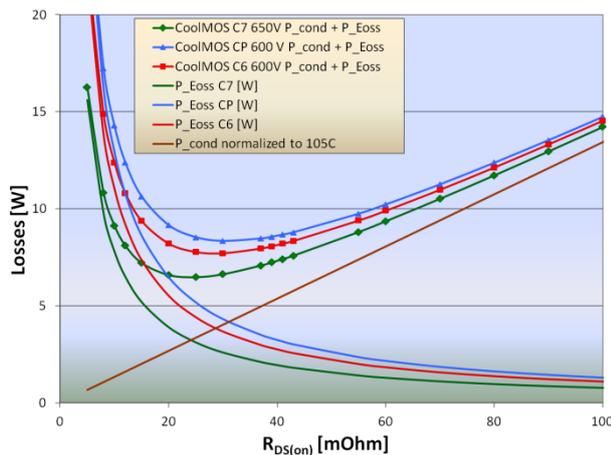
Figure 10: E_oss vs. R_DS(on) loss balance 800W PFC at 130 kHz, 90VAC input
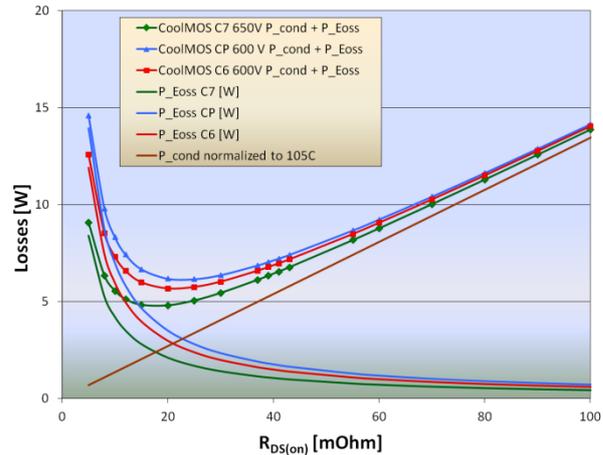
Figure 11: E_oss vs. R_DS(on) loss balance 800W PFC at 70 kHz for 90VAC input

In Figure 10 the characteristics of C7, CP, and C6 are compared at 800W, which correspond to a current level of 8.9A, and a frequency of 130kHz.

In this simplified comparison, both previous generations seem to show the same optimum resistance for the lowest overall losses, namely at approximately 30mΩ. However, the contributions not taken into account (e.g. those C_{GD} related) would bring a less favorable position for C6 with respect to CP. Under these conditions, C7 shows a much lower loss balance point, close to 20mΩ, or, seen from another perspective,

Figure 12: E_oss vs. R_DS(on) loss balance 1400W PFC at 130 kHz for 176VAC input

with CoolMOS™ C7 one can reach the same losses level as the optimum of previous generations with a much smaller chip, i.e. higher on-resistance class, in this case close to 50mΩ. Therefore, it allows either achieving a higher efficiency optimum with the right on-resistance class or keeping the efficiency level of previous generations but at a lower cost (higher on-resistance class) and eventually higher power density (if the smaller chip size makes possible the next smaller package class).

Considering this PFC stage in high line operation, the same stage would be typically required to deliver ~1400W in the high line range from 176VAC to 250VAC (nominal 230VAC).

As is seen in Figure 12, the range of similar loss balance is much wider, due to the lower operating current, approximately 7.9A, and the much lower Duty cycle. If this were the only operating mode for the PFC stage, then the economical choice would be to use a higher R_{on} MOSFET which would be less

expensive. Even in this scenario, C7 shows a clear advantage in losses due to lower E_{oss}, and would deliver higher efficiency peaking at the mid load point of 50% power, due to the lower E_{oss} losses.

These results show a clear performance advantage when power density is needed in the PFC or when the CCM switching mode must be extended to a lower load range by using a higher switching frequency for a given size inductor in order to maintain good power factor.

Current practice often relies on using the lowest possible switching frequency in order to minimize semiconductor switching losses, typically 65-70kHz for the PFC. These lower frequencies allow further reductions in the MOSFET losses, although they may be compensated by additional losses in the inductor required to support this frequency (both due to copper losses and core excitation loss). Also in this 70kHz case a ~25% potential advantage is seen for C7, since this part of the losses can be reduced from ~7 watts down to ~5 watts for a 20mΩ device.

4.3 Efficiency benefits

From the characterization data presented so far, it is clear that C7 has substantially improved dynamic properties and can offer much lower $R_{DS(on)}$ in a given package. Now, the value of $R_{DS(on)}$ which has been best in class for TO-247 is available in a TO-220 package. The significance of this goes beyond space utilization in the converter - the TO-220 package has about one half of the source inductance of the TO-247, and this offers even further performance potential for C7 over its predecessors due to better switching behavior and lower losses.
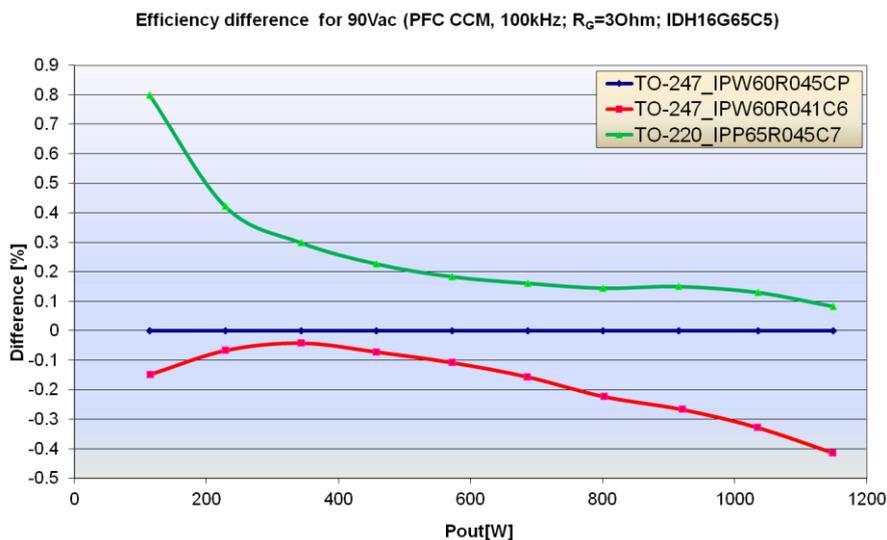
Figure 13: Efficiency comparison of IPW60R045CP, IPW60R041C6, and IPP65R045C7

Figure 13 represents a comparison of the measured efficiency in a PFC between IPW60R045CP, IPW60R041C6 and IPP65R045C7, Where the efficiency of IPW60R045CP is used as a normalized reference and differences in % can be better observed. The maximum output power of 1150W in this graph was chosen in the range where this on-resistance class of MOSFETs is typically used.

Looking at the comparison of CP and C6, the technological differences mirrored in their key electrical parameters (E_{oss} and Q_G) are approaching a breakeven point at 350W. At this power and output current, the E_{oss} advantage of the IPW60R041C6 gets compensated by the lower switching losses at high current of the IPW60R045CP.

Examining the IPP65R045C7 in comparison, a marked advantage in light load efficiency is seen due to the much lower E_{oss} loss and the generally better dynamic properties. At high power, it still maintains an advantage over both CP and C6 despite the proportionally more relevant role of the conduction losses, which are equivalent for all three products since they belong approximately to the same on-resistance class. This means that the switching losses advantage of CoolMOS™ C7 is still very relevant at large currents.

Therefore C7 is an enabler for increasing the frequencies without suffering an efficiency decrease in the application.

5 Further considerations on the dynamic switching behavior of CoolMOS^{TM} C7

MOSFET switching is first governed by the interaction of gate resistance (internal and external) and MOSEFT capacitances (gate to source C_{GS}, gate to drain C_{GD}, and drain to source C_{DS},) (Figure 14). Package inductance and PCB parasitic impedance have usually played a secondary role in previous generations with high switching losses. But with the speed of the CoolMOS^{TM} CP and the newest generation of CoolMOS™ C7, secondary effects become more important, including the influence of source circuit inductance and drain to source output capacitance. The behavior of these fast superjunction devices differs in many aspects from the conventional MOSFETs.

Understanding these behaviors and using them to advantage within safe limits in the application requires a deeper look into the MOSFET switching behavior. Note that for correlation with standard data sheet terms, $C_{iss} = C_{GS} + C_{GD}$, $C_{rss} = C_{GD}$, and $C_{oss} = C_{DS} + C_{GD}$. Turn-on behavior is usually strongly influenced by the application circuit and associated components, but turn-off behavior is mainly controlled just by the MOSFET characteristics, so this is the mode that will be examined closely.
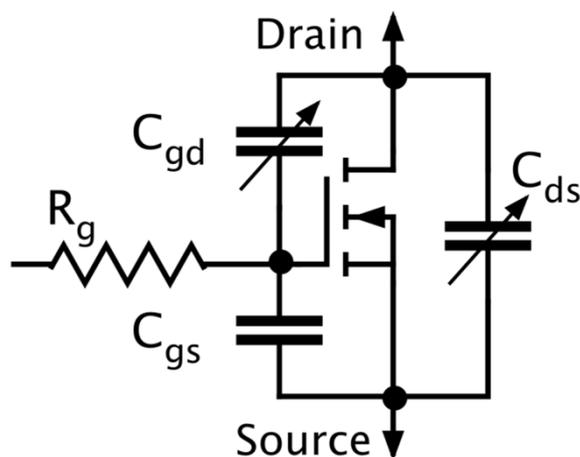
Figure 14: Basic elements controlling MOSFET switching

5.1 Gate controlled MOSFET switching

Considering the diagram of Figure 15 the gate controlled MOSFET turn-off occurs in three fairly discrete intervals, and the behavior and losses for each interval is described separately.

In the interval t1, the driver discharges the gate voltage to the current plateau level, with a time determined largely by the C_{iss} (consisting of C_{GD} and a high value of C_{GS}), the gate input resistance R_G, the operating voltage levels for the gate drive and the plateau voltage determined by the MOSFET G_{fs} and load current:
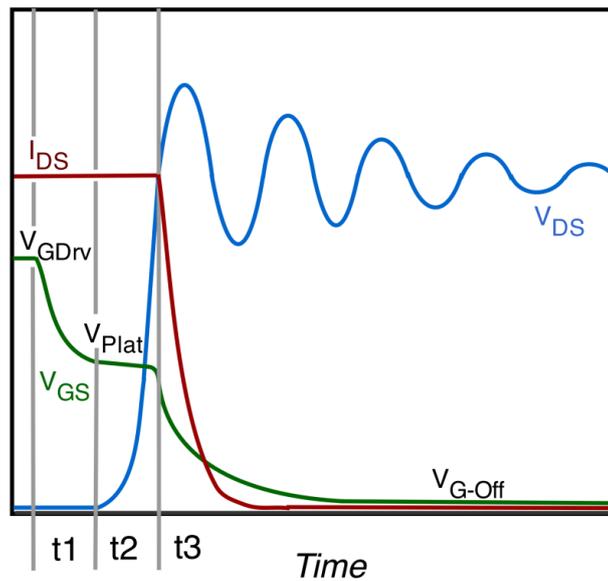
Figure 15: Gate Controlled turn-off switching

$$t1 = R_G * C_{iss} * \ln\left(\frac{V_{G_{Drv}} - V_{G_{off}}}{V_{G_{Plat}} - V_{G_{off}}}\right)$$

Equation 3

$$t1_{C7\_045} = 1.8\Omega * 4340pF * \ln\left(\frac{12V - 0V}{5.4V - 0V}\right) = 6.24\text{ns}$$

During the time interval t1 the C_{iss} gets discharged until it reaches the Gate voltage where the Transistor gets into saturation for the actual load current. During this time there are no switching losses generated since neither V_{DS} voltage nor I_D current has changed induced by the MOS.

In the interval t2, the MOSFET is acting like an integrating amplifier, and the gate current supplied through R_G is that needed to charge C_{GD} as V_{DS} rises, even while full drain current flows:

$$t2 = \frac{R_G * C_{rss(fV_{DS})} * V_{DS}}{V_{G\_Plat} - V_{G\_off}}$$

Equation 4

During this gate-controlled interval, where dv_{DS}/dt is controlled by gate drive, the actual rate of change can be described by:

$$\frac{dV_{DS}}{dt} = \frac{V_{G\_Plat} - V_{G\_off}}{R_G * C_{rss}}$$

Equation 5

In the final portion t3 of turn-off, the gate drops below the plateau region, as R_G discharges C_{iss} further, and drain current falls following the MOSFET transfer function for I_D as a function of V_{GS}.

$$t3 = R_G * C_{iss} * \ln\left(\frac{V_{G\_Plat} - V_{G\_off}}{V_{th} - V_{G\_off}}\right)$$

Equation 6

This turn-off behavior is shown in Figure 16, displaying the comparative gate input waveform, driver voltage, and gate current illustrating the difference in switching speed as a result of the differences in gate charge and drain to source C_{oss}. In this mode, the gate drive retains complete control over the dv/dt of the MOSFET, and is directly sizable by adjusting the size of the gate input resistor.
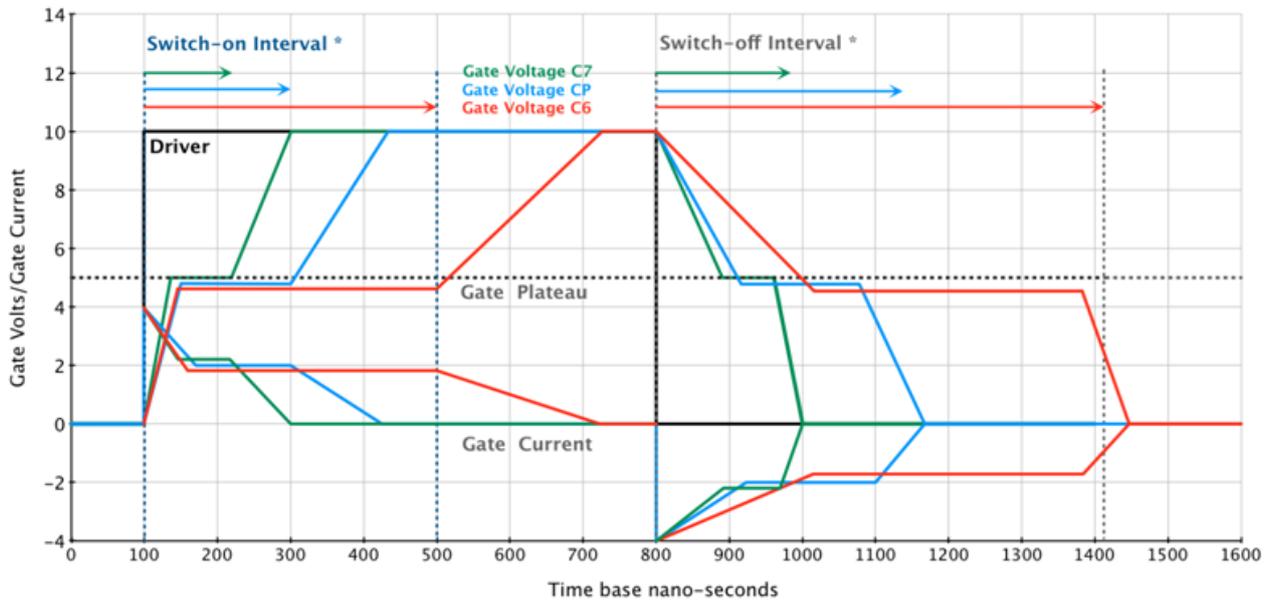
Figure 16: Comparison of CoolMOS™ C7, CP, and C6 for turn-on and turn-off timing
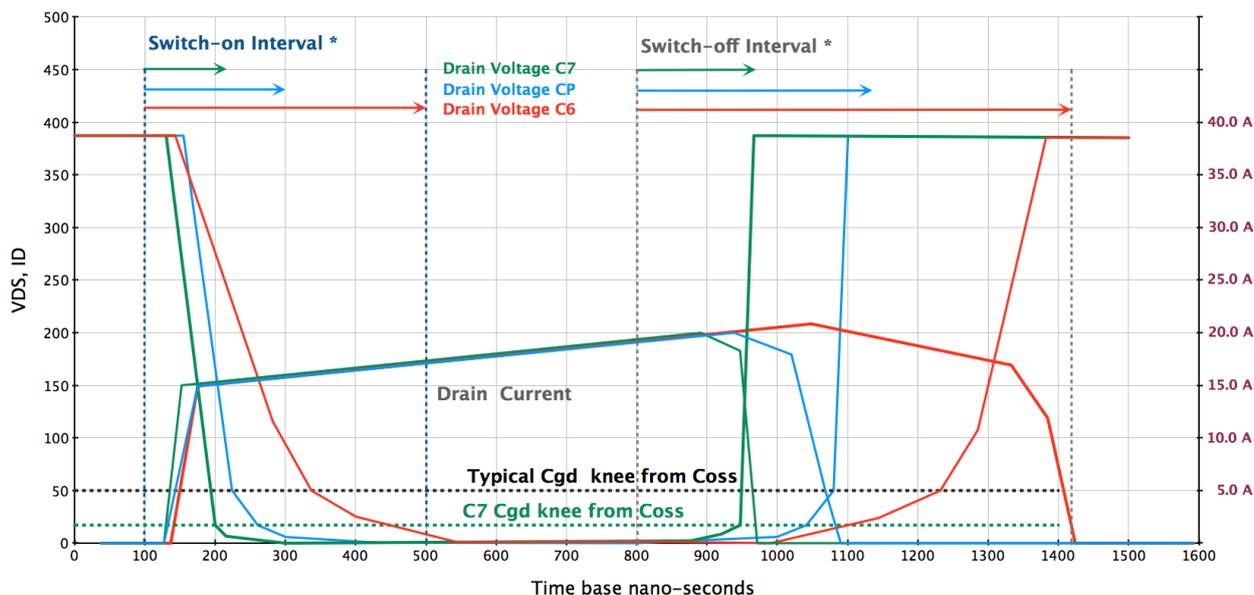
Figure 17: Switching simulation comparison for V_{DS} and I_D

The drain voltage and current waveforms in Figure 16 illustrate how the device characteristics result in different switching speed as well as different losses. Both CP and C7 have very low gate charge, and will show lower time delay and faster switching. To an extent, CP's behavior can be modified to look more like C6 by increasing the size of the gate resistor, and limiting the gate charging current. But the value of RG needed is high, in order to slow the main part of the drain to source transition occurring when C_{rss} is quite low.

That results in another effect, with higher losses then might be expected because of the non-linearity of C_{oss} and C_{rss}. This capacitance increases sharply as the P-wells are reforming in the region of 40-60V drain to source.

This effect can be labeled as a C_{GD} knee in the switching response. For CP, this will show up around 50V. For C7, due to the finer cell pitch, this effect occurs at about 20-25V, resulting in a faster drain voltage fall to a lower potential and lowering the turn-on loss.

However, as gate charge and C_{rss} at high voltage becomes lower in MOSFETs, and output capacitance non-linearity increases, using low values of gate drive resistance eventually shifts the switch-off behavior into a different mode, as we will see next.

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5.2 Quasi-ZVS turn-off switching (C$_{oss}$-limited)

Under conditions in which the gate drive turn-off is very fast, in combination with a relatively high C$_{oss}$ as can exist in superjunction MOSFETs when the drain to source voltage is below 50-60V, the switching behavior will be dominated by somewhat different mechanisms, and the drain switching voltage will not be controlled by the gate drive current, but by C$_{oss}$ and load current.

The behavior can still be roughly described by three main states, but externally measured gate drive or drain current can be misleading in identifying these states. The t1 state is governed similarly as for the gate controlled dv/dt mode; the difference arises in the t2 region, where the gate discharging current is at such a high level such that the load current cannot begin to charge a voltage across C$_{oss}$, and the channel current is turned off before the drain to source voltage rises. This is approximately described by:
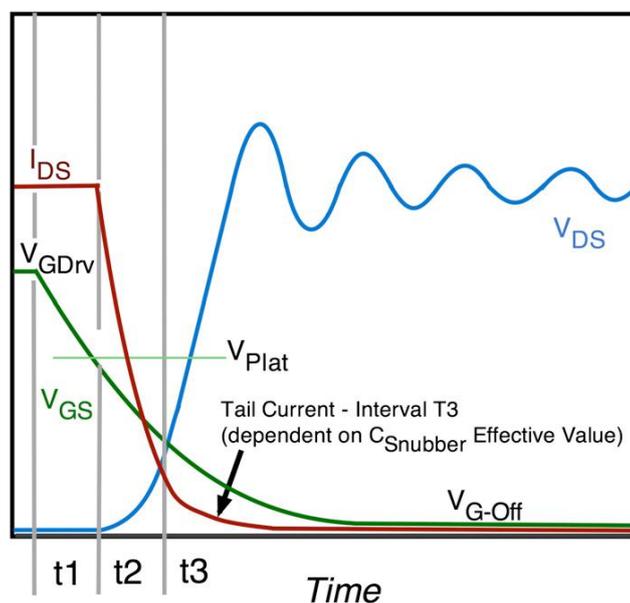
Figure 18: Quasi-ZVS C$_{oss}$ controlled turn-off

$$t2 = R_G * C_{iss} * \ln\left(\frac{V_{Plat} - V_{G\_off}}{V_{th} - V_{G\_off}}\right)$$

Equation 7

This mode does result in very low turn-off losses, as might be expected, but it has some characteristics to consider that can become problems in some applications, especially Power Factor Correction boost converters which can see a wide range of input current, and brief but high overloads.

This requires some extra care in the CoolMOS™ C7 series, due to the very low Q$_{GD}$, and different output capacitance characteristic (Figure 6). Why does it happen? Examining the capacitance curves of the three technologies, it is seen that CoolMOS™ C7 has a substantially higher output capacitance below 20V.

This is due to the smaller cell pitch required to achieve lower area specific R$_{ON}$ with high doping levels in the epi. As blocking voltage develops, around 20V there is a very abrupt transition from a P-column structure to a near planar formation of the space charge region, resulting in more than an order of magnitude drop in output capacitance over a small voltage range.

This is the "ideal" characteristic for a low loss non-linear ZVS snubber - it keeps the output voltage rate of rise, or dv/dt, initially low, while gate voltage is completing turn-off. Then, the output capacitance drops to a very low level, around 50 pF, permitting a very fast drain voltage rise. However, any possibility of drain control is lost because the low Q_{GD} gate design means that gate-drain overlap capacitance is absolutely minimized, and as a result C_{rss} drops to an astonishingly low value, as can be seen in the previous Figure 4.

How is the designer to make a safe and effective choice, given these issues?

The first recommendation is to "stay in gate control" - understand the possibilities of stress on the MOSFET in the application circuit, and initially keep the turn-off transition in or near the gate controlled region. In a forward converter, the operating current range is relatively limited, and operating current tends to be low. C_{oss} controlled turn-off will not result in potentially destructive dv/dt and other effects in the circuit. In boost converters for PFC, the peak current is not necessarily under direct gate control, considering issues like input voltage transients and response delays in an average current mode controller. In that case, more care must be exercised.

The key to reliability under all conditions is maintaining device control. This means using gate drive to limit ultimate di/dt and dv/dt by using the correct range for gate driver resistance. This is in principle the same for CoolMOS™ C7 than for CP or C6.

Drain current as a function of applied Gate voltage for the three generations is similar, as the comparison shows here in Figure 19 between IPW60R041C6, the IPW60R045CP, and the IPW65R045C7. Therefore each generation can carry the same approximate current for the same gate voltage.

The lower saturation level of C7 limits the current in short circuit condition and therefore protects the whole application from high short circuit stress.

Figure 19: Typical V_{GS} to I_D Transfer Characteristics for 41-45 mΩ C6, CP and C7

5.3   Turn off di/dt

What happens when gate driver resistors are chosen outside a reasonable operating range? Let's examine this within the context of the 45 mΩ class C6, CP and C7 CoolMOS™.

With very low values of gate driver resistance, di/dt is not under control of the MOSFET, but instead by the surrounding circuit elements. This is demonstrated in Figure 20 with the gate input resistor of 1.8ohms for an IPP65R045C7, and di/dt that rises quite rapidly with load current, until limited by external parasitic inductance. In this case di/dt quickly reaches thousands of amperes per microsecond.

With the gate resistor raised to the range of 5 to 10Ω, the situation moderates, and the rate of charging C_{GS} controls the di/dt somewhat independently of parasitics in drain circuit, keeping peak di/dt in this case to a fast 2,000 - 3,000A/μsec.
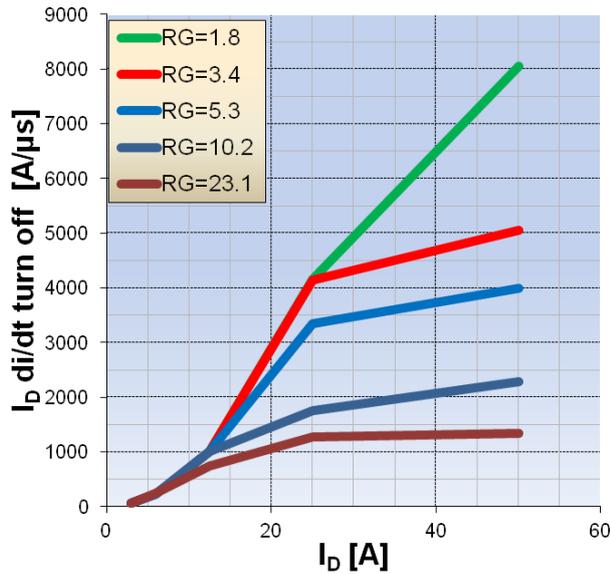
Figure 20: C7 turn-off di/dt for V_GS=12V as a function of drain current for R_G =1.8 - 23Ω
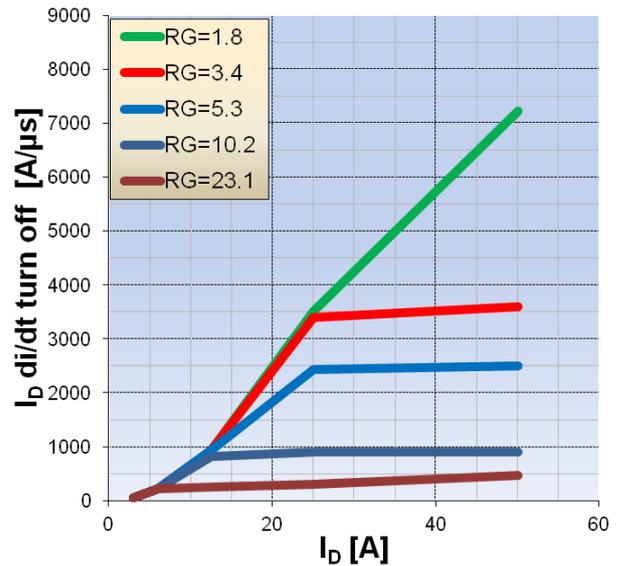
Figure 21: : CP turn-off di/dt for V_GS=12V as a function of drain current for R_G =1.8 - 23Ω
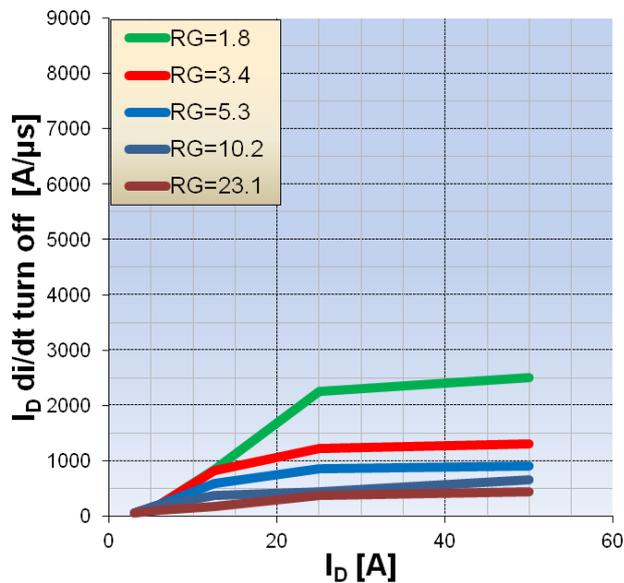
Figure 22: C6 turn-off di/dt as a function of drain current for R_G =1.8 - 23Ω

Contrast this performance with CP and C6 under the same driving and test conditions, in Figure 20 and Figure 21. CP has poorer control of di/dt regardless of the higher device capacitance, and makes an abrupt transition from relatively in control di/dt with an R_G=5.3Ω, to essentially no di/dt control with R_G=3.4Ω or 1.8Ω.

CP is clearly in C_{oss} limited mode even with 3.4Ω R_G, while C7 is in what can be called transition mode on the border between full gate control and ZVS switching, with some limitation of di/dt between 25 and 50A drain current.

Contrast this with C6, with its much higher gate to drain capacitance, as well as output capacitance. Even with 1.8Ω R_G, the di/dt is limited to a much lower range than for C7 or CP.

In some applications where high load current switching but very controlled di/dt is required, C6 may be a preferred alternative. However, this level of control can be reached with C7 using a 23Ω gate resistor, and switching losses will be in the same range as for C6 with an R_G of 5Ω. If light load efficiency and low gate drive power are considerations, or using a smaller package with lower inductance like the TO220 is a factor (IPP65R045C7), then consider the C7 technology.

5.4 Turn off dv/dt

Figure 23: C7 Turn-off dv/dt as a function of drain current for R$_G$ =1.8 - 23Ω

Figure 24: CP Turn-off dv/dt as a function of drain current for range of R$_G$ 1.8 - 23Ω

A similar situation exists for controlling dv/dt, as would be expected from Figure 23.

In the case of IPP65R045C7 with a gate resistor of 1.8Ω, the turn-off is very fast, due to low gate charge and low output capacitance above 25V. The dv/dt shows a linear rise with increasing load current, indicating true ZVS turn-off of the MOS channel, and rise of drain voltage which is only a function of how fast the output load current can charge the output capacitance C$_{oss}$.

This situation still exists with an R$_G$ of 3.4Ω and only begins to enter the transition region with an R$_G$ of 5.3Ω. For true gate controlled switching, an R$_G$ of 10Ω or higher is recommended. But, if the peak current is under 50A, even the lower R$_G$ values stay within the C7 dv/dt limit of 100V/ns. With higher peak currents, this dv/dt limit would likely be exceeded.

For the IPW60R045CP shown in Figure 24 the measured dv/dt is also high, but about 30% lower than for C7 under the same conditions. This cannot be considered equivalent, though, as the rated maximum dv/dt is 50V/ns for CP, but 100V/ns for C7. Overall, CP does not have the same level of control, as even the second highest value of gate resistance (10.2Ω) still shows steadily increasing dv/dt with higher load current. An R$_G$ of 5.3Ω puts the IPW60R045CP at the top of the transition region for dv/dt, and may be the lowest prudent value unless other circuit effects limit di/dt and dv/dt, such as operation in a half bridge with limiting series inductance.

To summarize, dv/dt during turn off is limited either by discharging the gate-drain capacitance (R$_G$ control) or by the charging rate of the output capacitance (C$_{oss}$ limited).

Working in the C$_{oss}$ limitation mode means:

✓ Little to no Joule losses at turn-off, and highest efficiency

✓ dv/dt strongly depending on load current

✓ No di/dt control anymore - controlled by external parasitic components or application circuit

Working under gate resistor control means:

✓ Additional switching losses

✓ dv/dt and di/dt relatively independent from load current

The lower the gate resistor tend the lower the load current, the closer you are to C$_{oss}$ guided turn off! At light load current, not a problem- at high load current, di/dt in stray inductance, including package source inductance may disrupt this switching behavior.

6 Circuit design and layout recommendations

There are a number of recommendations to make with regards to circuit design and layout practices that will assure a combination of high performance and reliability. They can be recommended as if "in order of importance", but realistically all are important, both in contribution toward circuit stability and reliability as well as overall efficiency and performance. They are not that dissimilar to recommendations made for the introduction of MOSFETs compared to bipolar transistors, or CoolMOS™ compared with standard MOSFETs; it is a matter of the degree of care. Particularly more care must be taken with very fast switching MOSFETs because of the inherent differences in internal capacitance, and how that can react in the application with external parasitic components inherent in the PCB layout.

6.1 Why MOSFETs can be susceptible to oscillations during switching

To understand the problems that can arise with fast power MOSFETs in SMPS applications, it is necessary to look both at device characteristics and external parasitic effects due to layout. Figure 25 shows the equivalent electrical circuit, including the effects of internal package and lead inductance, and the coupling capacitance dependent on PCB layout. The critical configuration is the loop formed by the effective "components" in the gate to drain circuit, including internal C_{GD}, gate and drain lead inductances, and the external parasitic coupling capacitance between gate and drain. Together these form a resonant circuit with a Q (quality factor) largely determined by the internal R_G ($R_{G\ int}$), at a frequency determined by the value of the reactive components. The phase shift through this network back to the gate can lead to oscillations if the MOSFET gain is greater than one at the tank circuit resonant frequency.

The main determinant of behavior is this external series resonant circuit, and the relationship of the effective resonant frequency to the internal corner frequency of the MOSFET, where the gain drops below 1. The gain corner frequency is controlled by internal R_G, device capacitances, and gain G_{fs}. The latter of course is dependent on the current operating level, so problems may not occur at nominal drain currents but can show up at peak operating current such as cycle skip recovery in boost PFC stages, or in current limit for isolated forward converters.

Figure 25: MOSFET equivalent circuit with surrounding elements forming a resonant circuit

The gain corner frequency is defined by:

$$f_G = \frac{C_{rss\_eff} * G_{fs}}{2 * C_{iss} * C_{DS}}$$

Equation 8

For the reason that the low C_{rss} enables fast switching in CoolMOS™ CP with low gate drive power, it also raises the corner frequency of the device, making comparable reductions in the layout parasitic capacitance necessary to avoid the situation where the series resonance of the drain gate circuit is within the higher gain area of operation of the MOSFET. As a result, external coupling capacitance as low as 10pF gate to drain

can lead to resonant effect causing oscillation (Figure 28). C_{rss} effective is voltage dependent, as also is C_{oss}, so the gain and likelihood of oscillation is voltage dependent in a complex manner. At higher V_{DS}, the output capacitance lowers, and the gain-bandwidth product increases. As transconductance is current dependent, then also is the likelihood of oscillation greatest at high current because of the increase in overall gain and pushing the unity gain crossover higher in frequency.

As a result, external C_{GD} should be kept below 5pF to stay in the safe area.

An additional important factor is the total effective source inductance, including the package wire bond inductance and the external trace inductance. This doesn't affect the resonant frequency in the gate to drain circuit, but is the triggering factor. When turning off with small values of R_G, the rapid collapse of drain current causes a di/dt spike that triggers the gate-drain circuit, and the trigger effect is dependent on the amplitude of dv/dt generated in the source. For a larger source inductance a greater the value of peak dv/dt results and a bigger kick occurs to start off oscillations.

The key then is to avoid a gate to drain series resonant circuit frequency that is lower than the gain corner of the MOSFET. This can be achieved in two ways - firstly, by using layout practices to raise the series resonant tank frequency through reducing parasitic capacitance and inductance and secondly by limiting the MOSFET gain and gate circuit "Q" through appropriate gate drive circuits.

6.2   Layout - Avoid stray coupling capacitance between drain and gate

As it was discussed above, stray gate to drain capacitance needs to be minimized. In the effort to pack more and more components in less space, this dictum is often overlooked, as the example of Figure 26 shows. While problems with voltage clearance do not increase as long as gap spacing is maintained, close gap spacing over a large area definitely creates problems with increased capacitance. Do not run gate traces parallel to drain foils, and when possible, use source foils or the ground-plane to shield the gate from the drain connection.
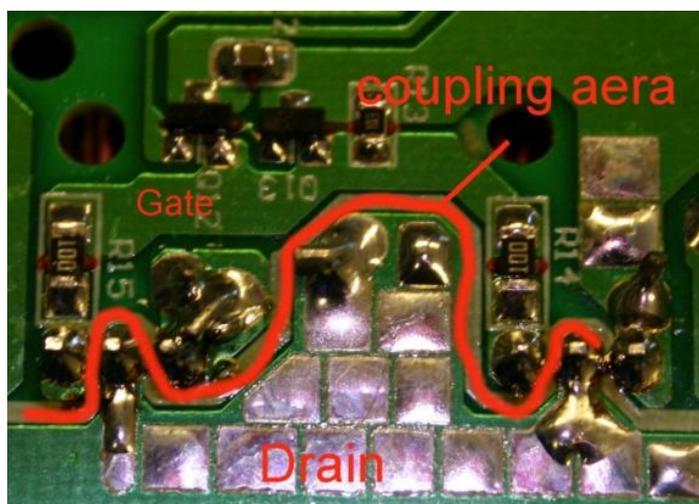
**Figure 26: Commercial layout leading to problems
due to close proximity of gate and drain**

6.3 Control gain and dv/dt and di/dt by proper selection of gate resistor

The question may arise, what does the switching look like if one does not carefully size the gate resistor and keep the layout compact and tight? Consider the oscillograph shown in Figure 28 at 20ns/div. MOSFET turn-off is forced very quickly via low gate driving resistance, but due to energy stored in the long gate trace connection, turn-off is not fully completed and results in oscillations and turn-on again of the MOSFET. This bad gate loop behavior is seen from the ringing measured differentially across the gate trace (blue trace), the ringing and secondary rise in drain current, and the secondary rise in gate voltage for nearly 40ns. This type of "dirty" turn-off, besides having the potential for developing oscillations that can reach voltage amplitudes sufficient to destroy the gate oxide, will also generate additional radiated EMI. This EMI may exceed permissible limits during compliance testing.

The first step in attacking this problem will be to limit dv/dt with the right value of gate resistor. This will reduce the affect of other design issues, and facilitate further testing and optimization. The second step would be reducing the inductance of the gate connection either by reducing the length or increasing the trace width. For the circuit tested in Figure 27, adding a fast PNP pull down located by the MOSFET, and lowering the ground circuit inductance solved most of the problems and lowered radiated EMI by over 20dB.
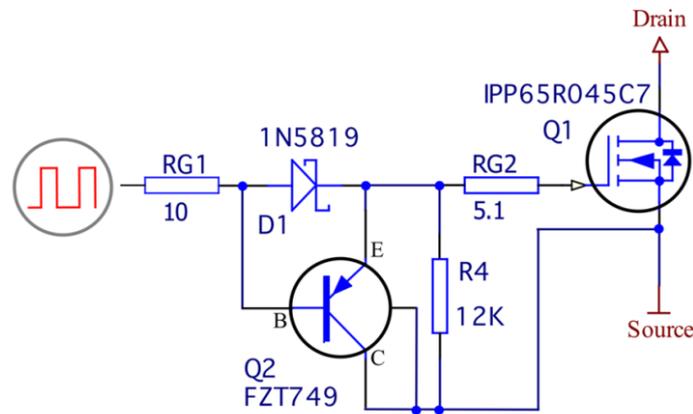
Figure 27: PNP pull down gate drive
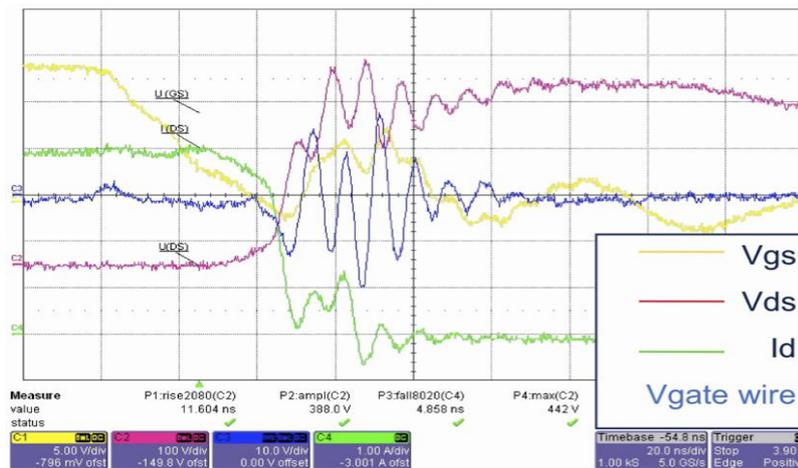
Figure 28: Turn-off waveforms with gate oscillations arising due to interaction in the gate to source circuit during turn-off
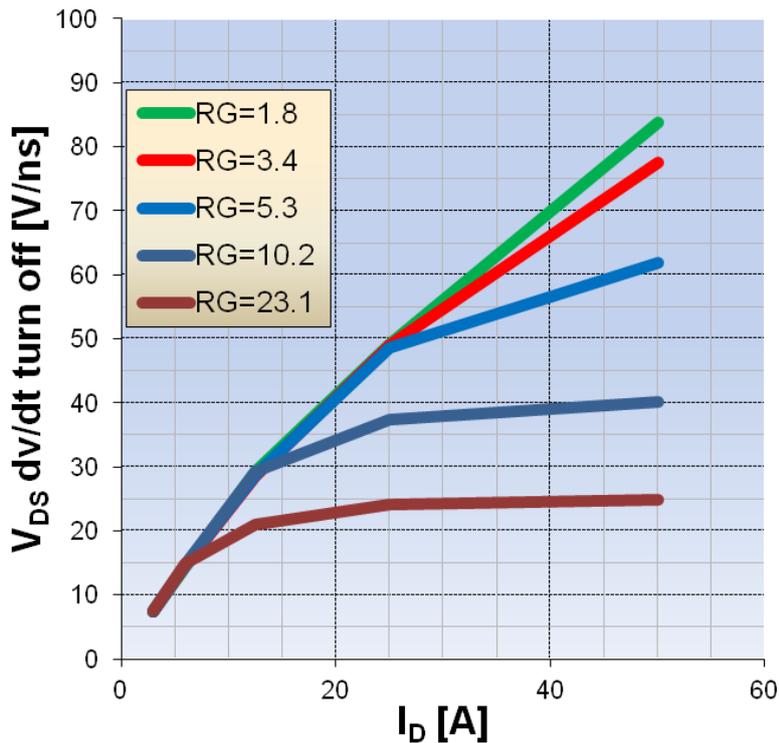
Figure 29: C7 Turn-off dv/dt as a function of drain current for R$_G$ =1.8 - 23Ω
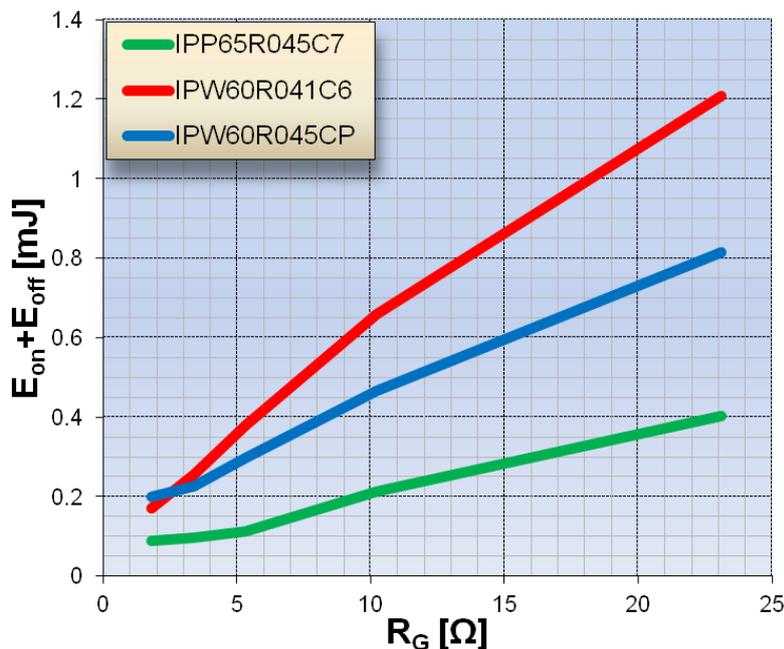
Figure 30: Switching losses comparison (E$_{on}$+E$_{off}$) @ 25A drain current for R$_G$=1.8 - 23Ω

Keep in mind that the gate resistor scales with device size and area related capacitance. Figure 29 below shows the behavior with several R$_G$ values from 1.8Ω to 23Ω for the IPP65R045C7 over a range of drain current. Depending on system performance targets, optimal performance may suggest an R$_G$ value of 10Ω, as it is at the edge of the transition region, but still shows effective dv/dt control at about 40-50V/ns from about 1/3 of rated drain current and higher.

Combined E$_{on/off}$ losses, from Figure 30 below, are about 200 µJ. This is by no means best case possible for C7, but it's actually in the same range to the values achievable with C6 and CP using R$_G$=3.3Ω. On the other hand, if using significantly lower R$_G$ values for C7, dv/dt control will be lost. Last, the characterization data suggests that going below an R$_G$ of 5Ω with C7 in this package is just generating more EMI, as lower losses won't be gained.

For other R$_{DS(on)}$ values than the 45mΩ, the gate resistor will scale ratio-metrically. For double the R$_{DS(on]}$, try doubling the R$_G$. Also keep in mind that package source inductance has an effect on switching time and losses, and is load current dependent - this topic is worth its own paper.

Note that when there are suspected layout issues, it is prudent to use a higher gate resistor value initially with C7, such as 23Ω, conducting testing with a lower di/dt and dv/dt, until other issues are fully resolved.

6.4   Improved gate damping of C7 compared with CP

The question naturally arises, with the lowered Q_{GD} and improved FOM, is there a drawback? How does C7 compare with CP as regards ringing in typical applications? To investigate this thoroughly, special application test boards based on boost topology have been developed with well-characterized parasitic PCB C_{GD} for the DUT, in order to study MOSFET ringing as a function of the layout and load current.

The testing is done in a boost topology and the sequence supplies a number of pulses to the gate of the DUT to increase the drain/inductor current during on-time of the MOSFET. During the time while the gate signal is low, the current in the inductor continues its flow through a diode into the output capacitor which is kept at 400V. Therefore the current at the following pulse is nearly the same as it was for turn off at the previous one. This testing sequence allows the analyses of switching behavior at different current levels for reference to real application.
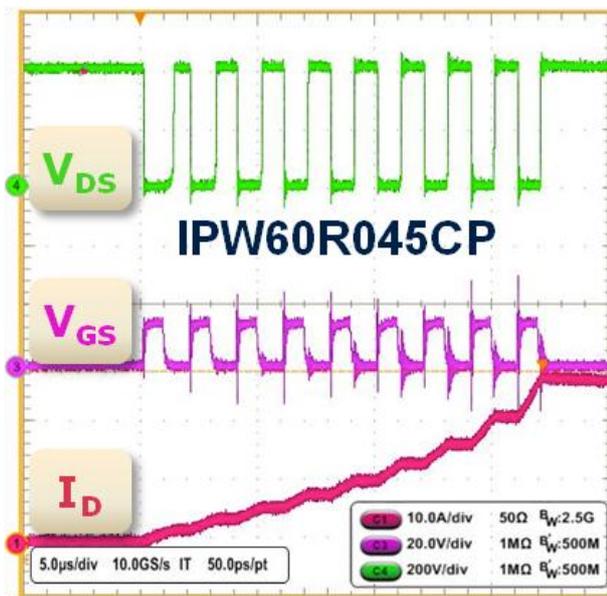
Figure 31: Gate ringing test with IPW60R045CP for current stepped up to 25A for R_G=3Ω.
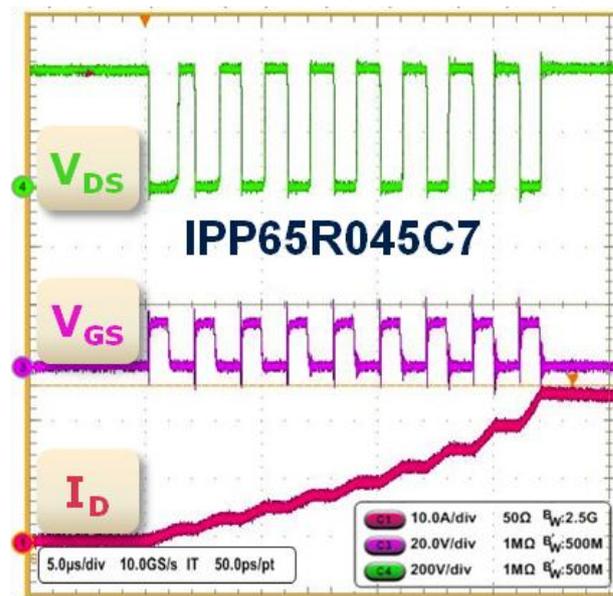
Figure 32: Gate ringing test with IPP65R045C7 for current stepped up to 25A for R_G=3Ω

The graphs above show the ringing behavior in a switched current test that steps up the inductor current to a level of 25A, in a standard test layout with parasitic capacitance not well optimized. Under the same conditions, CP exhibits both greater gate ringing (magenta trace) and some apparent drain to source ringing (green trace, seen as undershoot on the drain to source waveform).

Additionally, raising the test current to the current probe limit of 50A showed no further growth in ringing for C7, but may result in sudden destruction of the CP parts because of the impact of board inductance and capacitance.

This is a test board system engineered to provoke this kind of behavior by increasing the amount of PCB feedback capacitance between gate and drain. The results of this comparison show that efforts to increase the internal damping and produce a more robust MOSFET with C7 have been successful.

A detailed zoom of the behavior at the 25A level shows much lower levels for the ringing time and amplitude for C7 compared with CP:
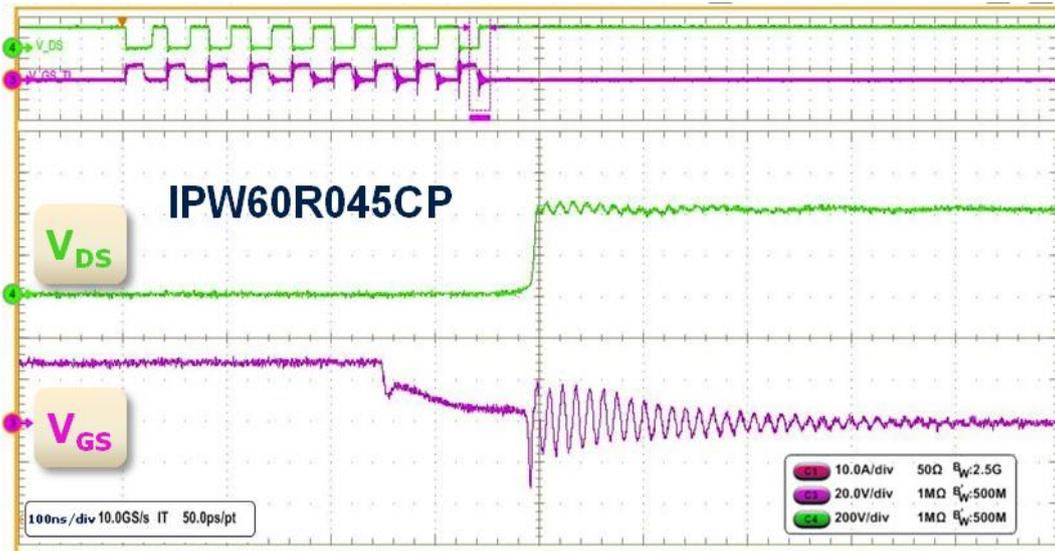
Figure 33: Zoom at 25A for IPW60R045CP gate ringing in test PCB

The oscillograph below in Figure 34 shows a much lower level of ringing for C7, which damps out much faster. In neither case were extra measures like a gate ferrite bead used.

Beside this much better ringing behavior of the C7, it is strongly recommended to use ferrite beads for the Gate in case of pronounced Voltage peaks on the Gate in certain application circuits as described on next page.
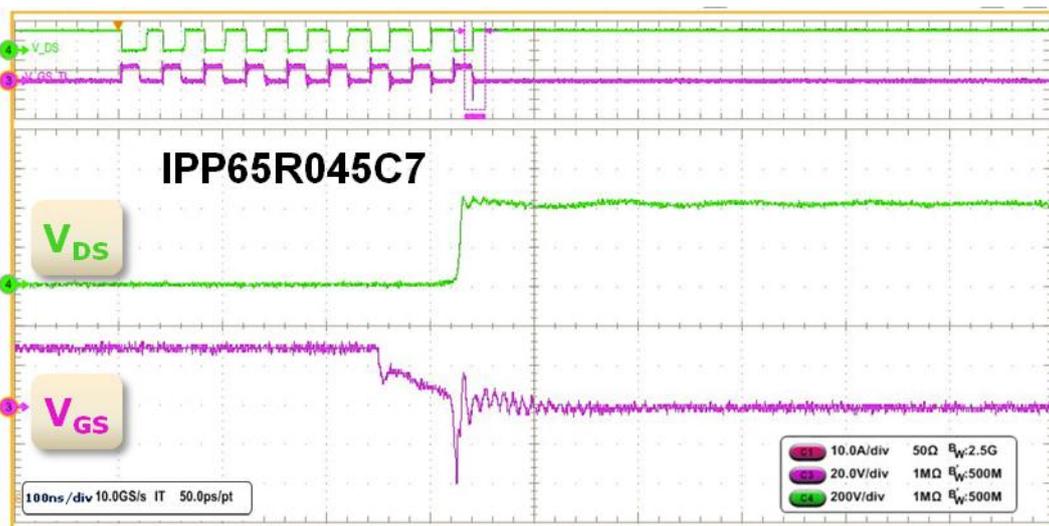
Figure 34: Zoom at 25A for IPP65045C7 gate ringing in test PCB

6.5   For fast switching circuits and problematic layouts, use a ferrite bead

A ferrite bead connected closely to the gate pin can reduce the MOSEFET corner frequency substantially while having only a small impact on the gate switching behavior. It must have a peak current capability matching the peak gate drive levels expected with some margin, and should introduce an effected loss impedance of 50-60ohms at 100MHz and above.

A suitable example is the Murata BLM41PG600SN1, in an 1806 SMD package. It is rated for 6A current and has a DC-resistance of 0.01Ω.

Figure 35: Impedance-frequency characteristics of BLM41PG600SN1 ferrite bead

It is particularly advisable to use this type of bead when going for the fastest reasonable switching speed in the converter, and particularly is helpful when paralleling devices like shown in Figure 36.

In an application circuit with a decent but not fully optimized layout, adding the bead may change the situation from having 8-12 cycles for gate ringing to damp out to just one or two cycles. If a single driver is used for paralleled MOSFETs, use of a ferrite bead at each gate is highly recommended and may be mandatory, depending on the layout. This prevents the possibility of the FETs literally talking to each other across the layout, due to influence from lack of symmetry of the current paths and the common gate connection.

Figure 36: Schematic of parallel MOS operation with ferrite bead on the gate

Mounting should be as close as possible to the gate pin. With this ferrite bead, it's possible to extend the region of stability at 400V to several times higher external gate to drain coupling capacitance. The main drawback of a ferrite bead is the small additional cost and the slight increase in board space from the 1806 SMD package.

7 Conclusions

Infineon's latest high-voltage superjunction MOSFET technology CoolMOS™ C7 has been able to achieve typical $R_{DS(on)}$*A values below 1 Ω*mm^2 for the first time. Additionally, the switching FOMs have been optimized to keep both good ease-of-use and the best efficiency for hard switching applications, when compared to previous generations. Furthermore, the relevance of the switching losses at high currents (i.e. power ratings) makes CoolMOS™ C7 an enabler for higher frequencies and/or higher power ratings.

8 List of abbreviations

C_{GD} ....internal gate drain capacitance $C_{GD}=C_{rss}$

C_{iss} .... input capacitance $C_{iss}=C_{GS}+C_{GD}$

$C_{o(er)}$ .... effective output capacitance

di/dt ....steepness of current comutation at turn off / turn on

DUT..device under test

dv/dt ....steepness of voltage comutation at turn off / turn on

E_{off}... power loss during switch off

E_{on}...power loss during switch on

E_{oss}.. stored energy in output capacitance (C_{oss}) at typ. V_{DS}=400V

FOM .... Figures of Merit

I_D .... drain current

MOSFET..metal oxide semiconductor field effect transistor

PFC..power factor correction

PNP.. bipolar transistor type (pnp vs. npn)

Q .... quality factor of resonant circuit

$R_{DS(on)}$...drain-source on-state resistance

SiC .... silicon carbide

SMD.. surface mounded device

SMPS.. switched mode power supply

VDS..drain to source voltage, drain to source voltage

ZVS..zero voltage switching

9 References

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