High voltage CoolMOS™ CE in SOT-223 package

SOT-223 as DPAK replacement

About this document

Scope and purpose

Nowadays, the package costs of high voltage, high ohmic MOSFETs (metal oxide semiconductor field effect transistors) is the dominant part of the overall end customer selling price, therefore it is necessary to find other package solutions which can meet the same requirements and provide the same benefits as currently used package concepts.

This application note will provide an explanation of how to use a high voltage CoolMOS™ in a SOT-223 package. This package is a direct pin to pin replacement for DPAK without suffering any thermal limitations when using the DPAK footprint for SOT-223. Infineon Technologies provides the first high voltage MOSFET portfolio in a SOT-223 package without middle pin. This features the smallest geometry per $R_{DS(on)}$ (drain source on-state resistance) and reduces the overall BOM (bill of material) of an application as much as possible.

The biggest challenge when using SMD packages is the thermal behavior. DPAK is already widely used, especially in lighting applications. This document is going to compare DPAK and SOT-223 with respect to package dimensions and, most importantly, the thermal behavior.

Intended audience

This application note is written to give an application engineer or SMPS (switched mode power supply) designer the ability to overcome thermal boundaries related to SOT-223 through simulations and real application measurements.

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1 SOT-223 versus DPAK package outlines

The SOT-223 package can be a direct pin to pin replacement for a DPAK package with the outer dimensions and lead spacing shown in Figure 1.

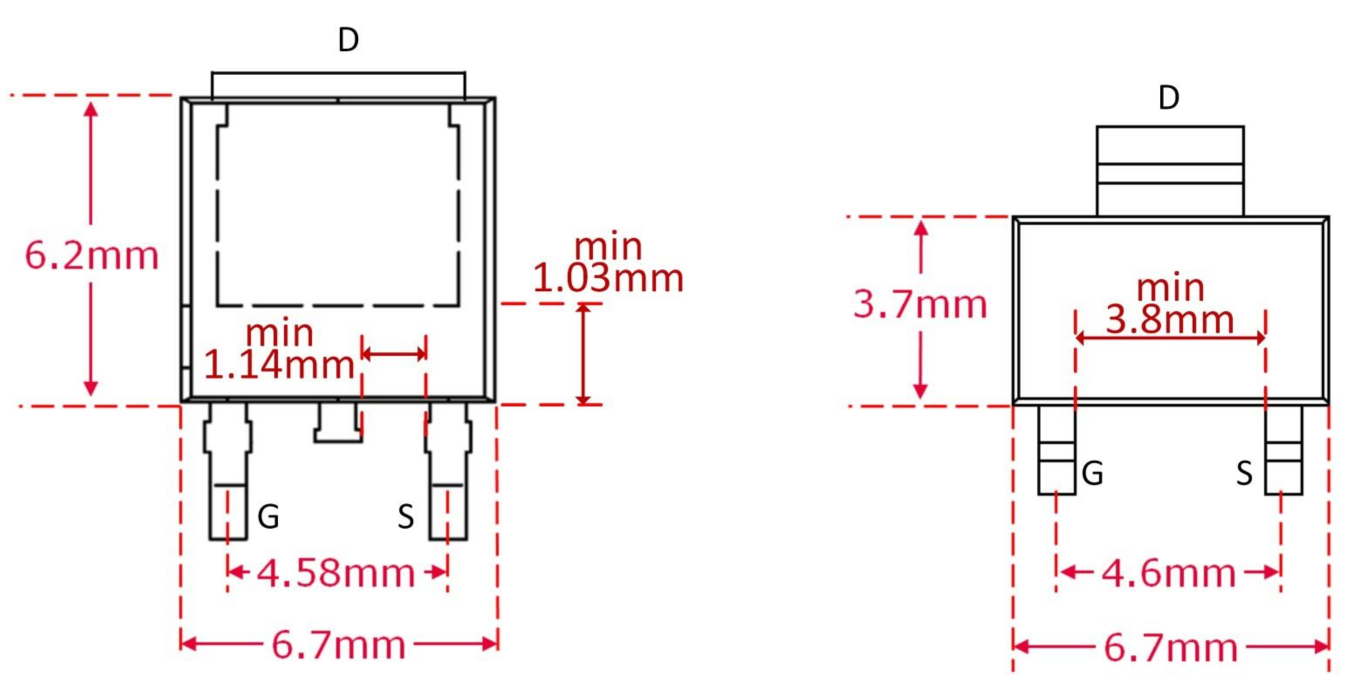


Figure 1 Package comparison SOT-223 and DPAK

It can be seen that the middle pin of a standard SOT-223 is removed which allows the inclusion of 700 V MOSFETs. This version of SOT-223 is even safer with respect to soldering processes (reflow or especially wave) as there is less possibility for solder residues between the leads. Additionally, the optical solder inspection after the soldering process allows greater visibility than with DPAK.

As already anticipated in the scope and purpose section of this document the biggest challenge with SOT-223 is the thermal behavior. This application note will discuss the general structure and thermal resistance (R_{th}) during steady state conditions in the next section.

2 Thermal behavior in steady state

The SOT-223 package does not offer an exposed leadframe like DPAK does. Therefore, the overall $R_{th,JC}$ (thermal resistance from junction to backside of the leadframe) is not a useful parameter and a SOT-223 package uses $R_{th,JS}$ (thermal resistance from junction to solder point) which is typically higher than the $R_{th,JC}$ from a DPAK (see Figure 2).

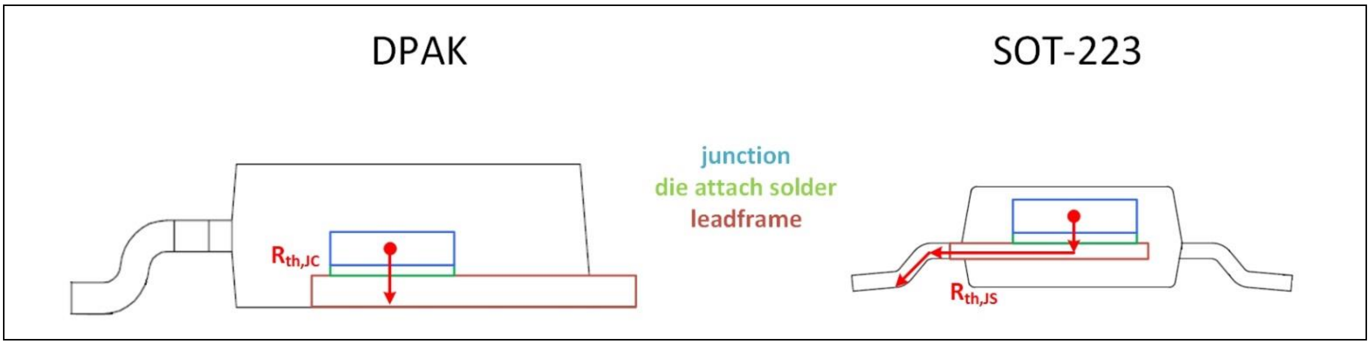


Figure 2 Simplified $R_{th,JC}$ (DPAK) versus $R_{th,JS}$ (SOT-223)

This leads to the conclusion that a SOT-223 package can only be used as a plug and play replacement if the overall power losses (switching losses and conduction losses) of the MOSFET do not exceed 300 mW and by accepting a slightly higher case temperature. If the power losses exceed this value, an additional copper area (connected to the drain pin (D)) needs to be included on the PCB (printed circuit board). Figure 3 below shows the thermal dependency of DPAK and SOT-223 packages on the copper area around the drain connection.

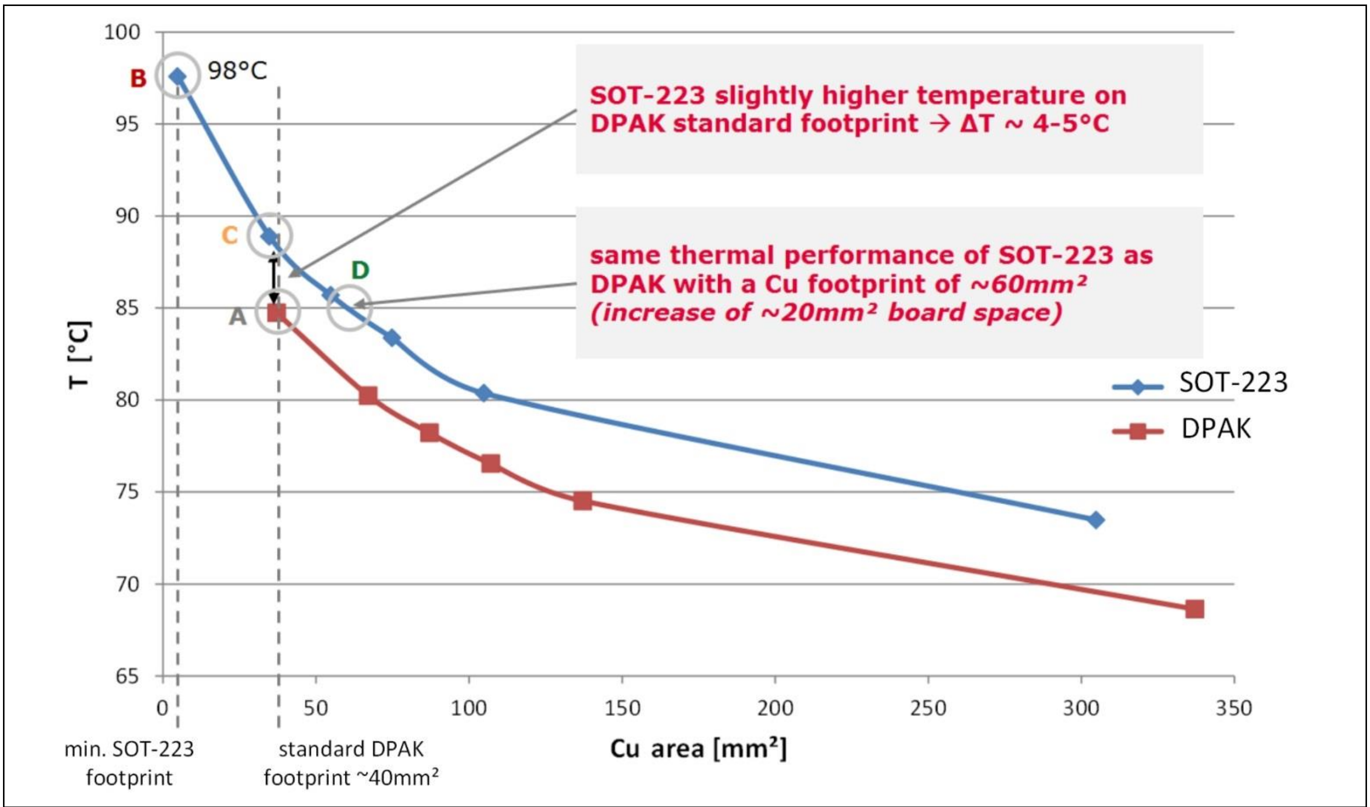


Figure 3 Thermal simulation of junction temperature @250 mW and ambient temperature of 55°C

This thermal behavior can be illustrated and explained by a constant current measurement setup which shows the temperature differences of the MOSFET mold compound. This comparison uses a DPAK mounted on minimum footprint (~40 mm²) and a SOT-223 placed on various PCB footprints (35 µm copper thickness / FR4 material), with up to 800 mW losses within the MOSFET.

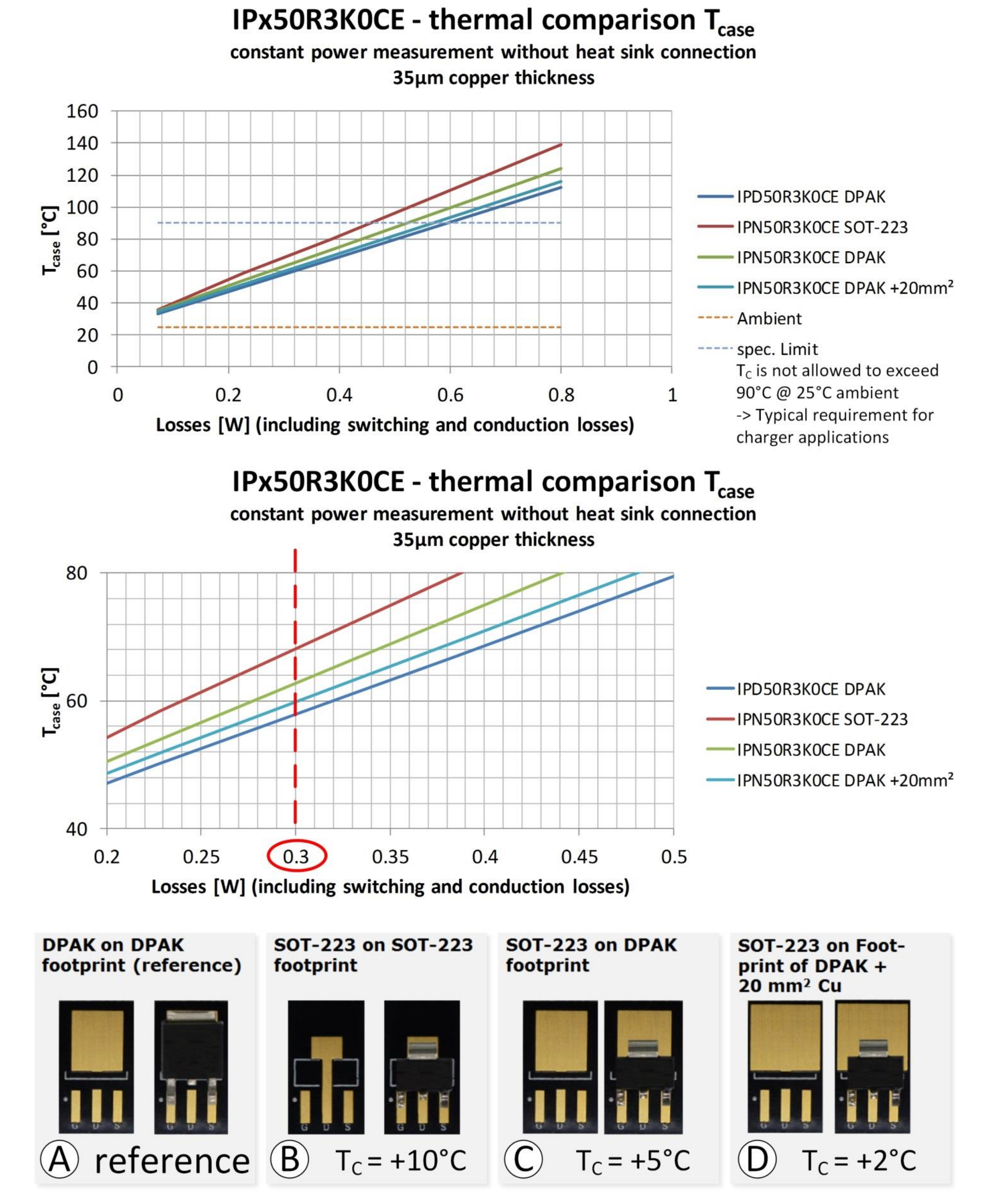


Figure 4 Thermal measurement with different adapter PCBs for SOT-223

Thermal behavior in steady state

A	DPAK on DPAK footprint:	This adapter board uses the minimum DPAK footprint with a DPAK package in order to have a reference measurement. The thermal image was acquired by a thermal camera after thermal saturation with a thermal gradient (ΔT_C) < 0.1°C/min.
B	SOT-223 on SOT-223 footprint: ~10 mm² copper area	The use of a SOT-223 package on the minimum SOT-223 footprint adds an additional 10°C to the mold compound temperature when compared to the DPAK which makes this setup suitable for very low power levels - giving the possibility to save board space. Nevertheless, as a direct DPAK replacement it can only be implemented if the design has enough thermal 'headroom'.
C	SOT-223 on DPAK footprint: ~40 mm² copper area	With this setup it is possible to use a SOT-223 package as a direct drop-in replacement for DPAK by accepting a ~5°C higher mold compound temperature. However, the DPAK design should have some thermal 'headroom' before reaching specification limits.
D	SOT-223 on DPAK + 20 mm² Cu: ~60 mm² copper area	The IFX recommended usage is represented by this configuration. With an additional copper area on the drain lead of around 20 mm² in comparison to the DPAK minimum footprint it is possible to achieve nearly the same thermal performance as with a DPAK.

It is clear that in case of using a SOT-223 package on minimum footprint as a replacement for DPAK would need very high thermal 'headroom' and this is typically not available in customer designs. The best opportunity to reach similar performace to the DPAK is to increase the copper area. This is especially true in lighting applications and is discussed in the next section of this application note where we will cover some thermal measurements in real customer designs with open and closed frames.

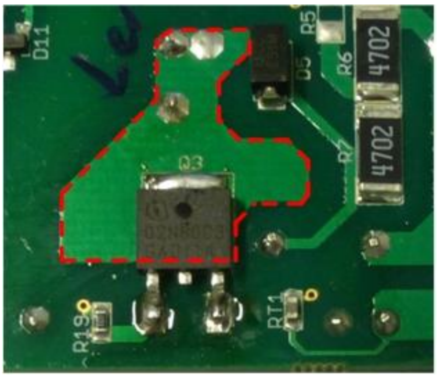
3 Thermal behavior in end customer designs

By reviewing end customer designs, especially in the lighting segment, there is a general availability of additional copper, in the range of >150 mm^2, as can be seen below. This would allow for a plug and play replacement by accepting a 2°C higher case temperature. Furthermore, all results which are shown are taken after 30 minutes burn-in time in order to heat up the whole application.

Attention: for a reliable and correct comparison between different packages even with the same technology inside it is necessary to have characterized and matched devices with respect to the chip inside the package itself.

3.1 18 W LED driver (open frame measurement)

3.1.1 Setup description



This LED driver is a single stage power factor corrected isolated flyback LED driver for lighting applications.

V_{IN} = 90 – 305 V_{AC}

I_{OUT} = 350 mA

V_{OUT} = 12 – 50 V_{DC}

Copper area = ~175 mm^2 (red marking)

Tested MOSFETs: IPD65R1K4C6 vs. IPN65R1K5CE

Thermal measurement: thermal camera; open frame; ambient = 25°C

3.1.2 Results

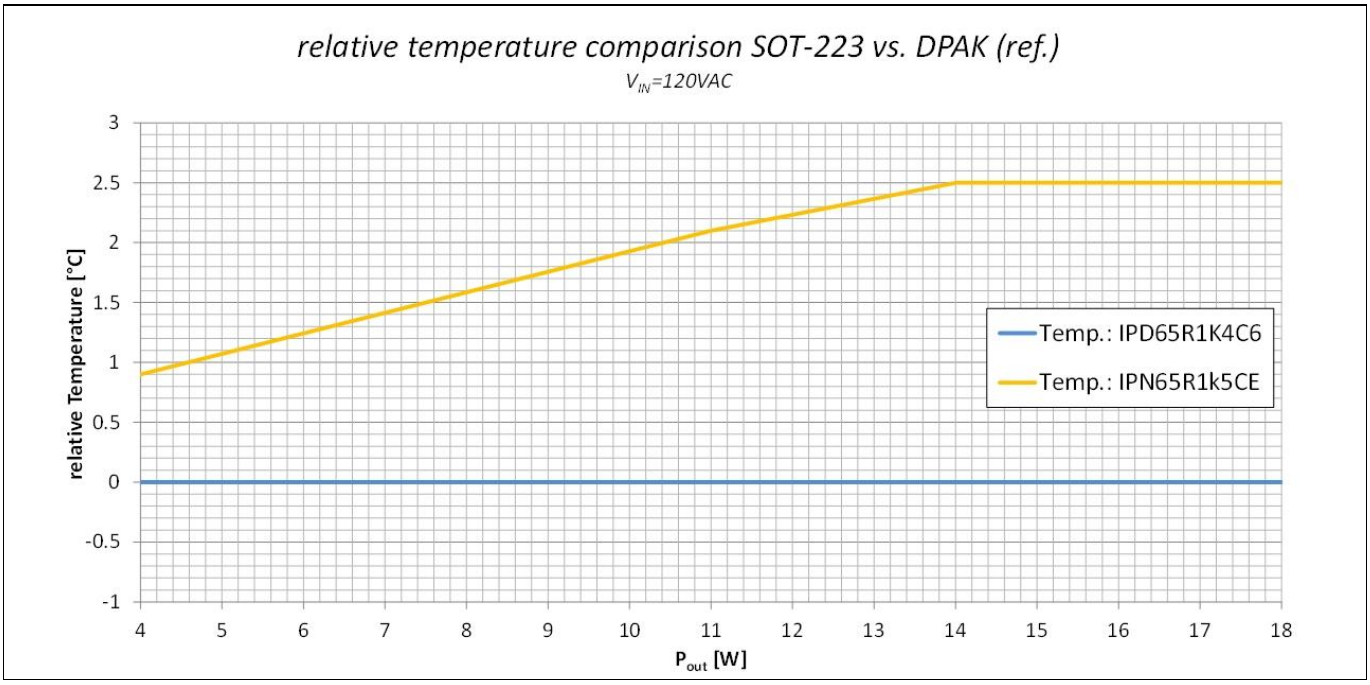
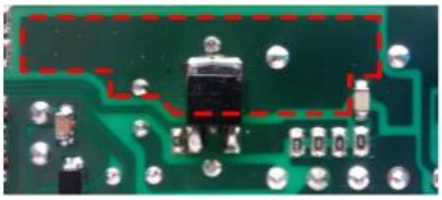


Figure 5 Thermal comparison of IPD65R1K4C6 vs. IPN65R1K5CE in an 18 W LED driver

Figure 5 above illustrates the maximum mold compound temperature on the y-axis and the output power on the x-axis. The IPD65R1K4C6 is represented as reference line in blue directly on the x-axis while the IPN65R1K5CE is represented as yellow line. It is clearly shown that the IPN65R1K5CE exhibits a higher mold compound temperature (2.5°C at full load and 120 V_{AC} input) than the IPD65R1K4C6. Now we will consider closed frame operation.

3.2 50 W LED driver (closed frame measurement)

3.2.1 Setup description



This LED driver is a single stage power factor corrected isolated flyback LED driver for lighting applications.

V_{IN} = 198 – 264 V_{AC}

I_{OUT} = 350 mA

V_{OUT} = 54 – 150 V_{DC}

Copper area = ~530 mm² (red marking)

Tested MOSFETs: IPD70R1K5CE vs. IPN70R1K5CE

Thermal measurement: thermocouples; closed frame; ambient inside enclosure = 52°C

3.2.2 Results

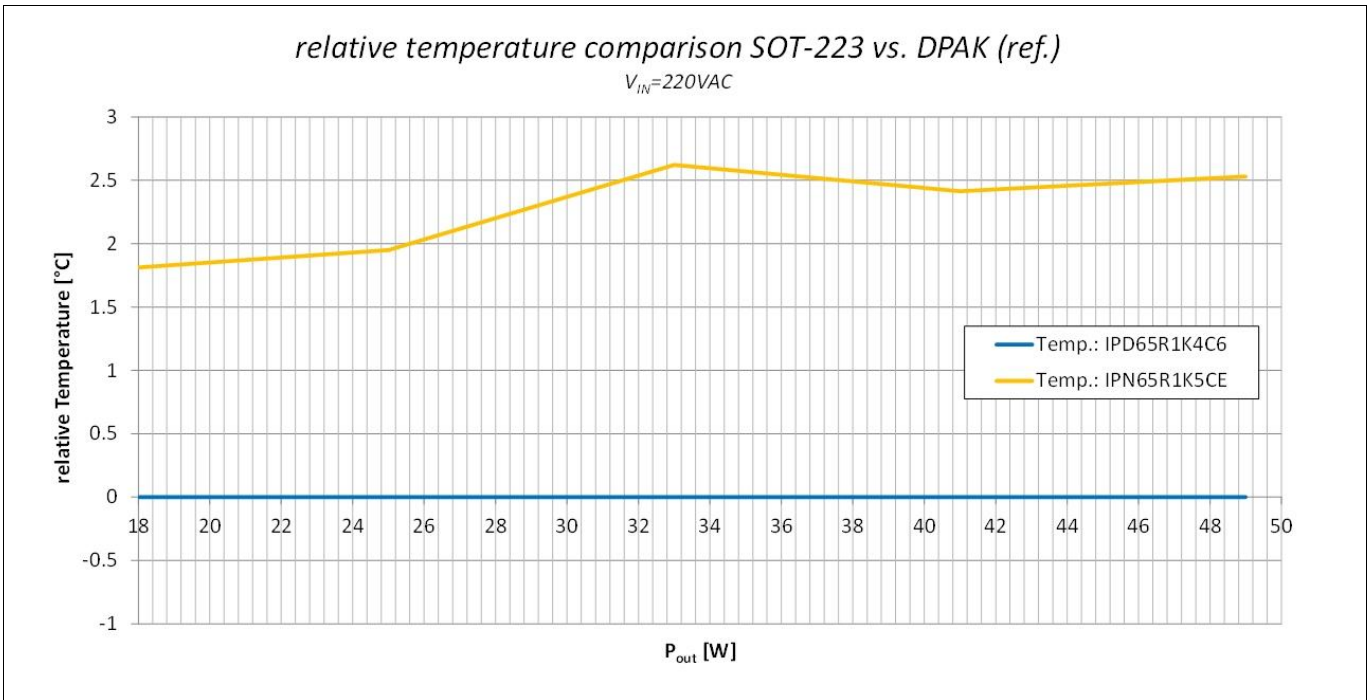
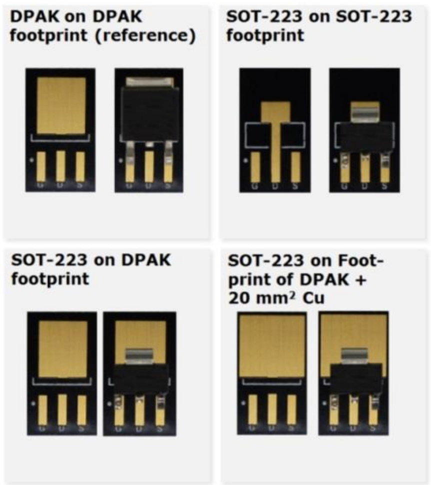


Figure 6 Thermal comparison of IPD65R1K4C6 vs. IPN65R1K5CE in a 50 W LED driver

3.3 10 W charger

3.3.1 Setup description



This charger is a QR flyback which typically uses an IPAK SL (short leads). In this case adapter boards were used to analyze the thermal performance – the same as the constant current measurement which was only tested at full load condition after 30min burn-in phase.

V_{IN} = 86 – 264 V_{AC}

I_{OUT} = 2 A

V_{OUT} = 5 V_{DC}

Copper area for SOT-223 = ~60 mm² (DPAK = ~40 mm²)

Tested MOSFETs: IPD60R2K0C6 vs. IPN60R2K1CE

Thermal measurement: thermal camera; open frame; ambient = 25°C

3.3.2 Results

Table 1 Thermal comparison of IPD60R2K0C6 vs. IPN60R2K1CE in a 10 W charger @ V_{IN}=90 V_{AC}

Adapter PCB	$T_{ambient}$ [°C]	T_{MOS} [°C]	ΔT (T_{MOS}-$T_{ambient}$) ΔT DPAK vs. SOT-223 [°C]
DPAK on DPAK footprint (reference)	24.6	95	**Reference**
SOT-223 on SOT-223 footprint	25.3	113.5	**+17.8°C**
SOT-223 on DPAK footprint	25.4	103.4	**+7.6°C**
SOT-223 ond DPAK footprint + 20 mm²	24.7	97.9	**+2.8°C**

It is clearly visible that this $R_{DS(on)}$ class would not fit the requirement of the charger itself. It clearly shows the thermal differences related to the package. In this case the SOT-223 would have a 2.8°C higher mold compound temperature on the DPAK footprint increased by 20 mm² (total of ~60 mm² copper area) than a DPAK on a DPAK footprint which leads to the following conclusion for all of the application tests performed.

3.4 Application test summary

All of the applications analyzed have shown that the mold compound temperature is heavily dependant on the additional cooling from the copper area connected to the drain pin. With an additional copper area of ~20 mm² and above, when compared to the DPAK minimum footprint, it is possible for a SOT-223 package to have nearly the same thermal performance as a DPAK by accepting a 2°C – 3°C (approx.) higher case temperature. This gives the SMPS designer the opportunity to reduce the overall BOM costs significantly as an additional copper area of 20 mm², if not already in place, does not increase the production costs of the application PCB.

Thermal behavior in end customer designs

The last section of this document will show the available portfolio of CoolMOS^{TM} high voltage MOSFETs in SOT-223.

4 Portfolio

The portfolio is currently based on CE technology in 4 voltage classes as shown in Figure 7 below.

$R_{DS(ON)}$[mΩ]	500V	600V	650V	700V
3400		IPN60R3K4CE		
3000	IPN50R3K0CE			
2000 / 2100	IPN50R2K0CE	IPN60R2K1CE		
1400 / 1500	IPN50R1K4CE	IPN60R1K5CE	IPN65R1K5CE	IPN70R1K5CE
950 / 1000	IPN50R950CE	IPN60R1K0CE		
800	IPN50R800CE			
650	IPN50R650CE			

Applications

Figure 7 Portfolio for SOT-223

In the future, the portfolio is planned to expand to include the latest technologies. Even lower $R_{DS(on)}$ values will be possible as better $R_{DS(on)}$ * A (area) technologies are in development. Updates to the portfolio will follow after the new P7 technologies are released by Infineon Technologies.

Revision history

Major changes since the last revision

Page or reference	Description of change

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