How to Compare the Figure Of Merit (FOM) of MOSFETs

by Jens Ejury

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Introduction

MOSFETs are produced for different applications. The basic understanding of a MOSFET is that the MOSFET works as a voltage controlled resistor. Ideally the resistance in on-state is zero, in off-state it should be infinite. Furthermore the control power should be zero since the control requires only a voltage – the current is zero.
For static applications – applications in which the MOSFET is controlled slowly, for example in protection circuits as a circuit breaker – the significant parameter is the on-state resistance $R_{(DS)ON}$. This value should be ideally zero but depending on the voltage range and the package it is in the range of some mΩ and some Ω.

In many cases MOSFETs are used to switch dynamically – for example in power converter applications (Switched Mode Power Supplies, SMPS). In these applications the performance of a MOSFET depends on several other parameters as well. SMPS switching frequencies are commonly in the range of below 100 kHz up to above 1 MHz. At these high frequencies the charge that has to be brought to the gate of the MOSFET to turn it on is not negligible. The charging and discharging of the gate has to be done very fast in order to diminish the switching losses. Basically it can be done faster if the charge to turn the MOSFET on is smaller. Because of that the gate charge Q_G is a very important parameter in a SMPS.

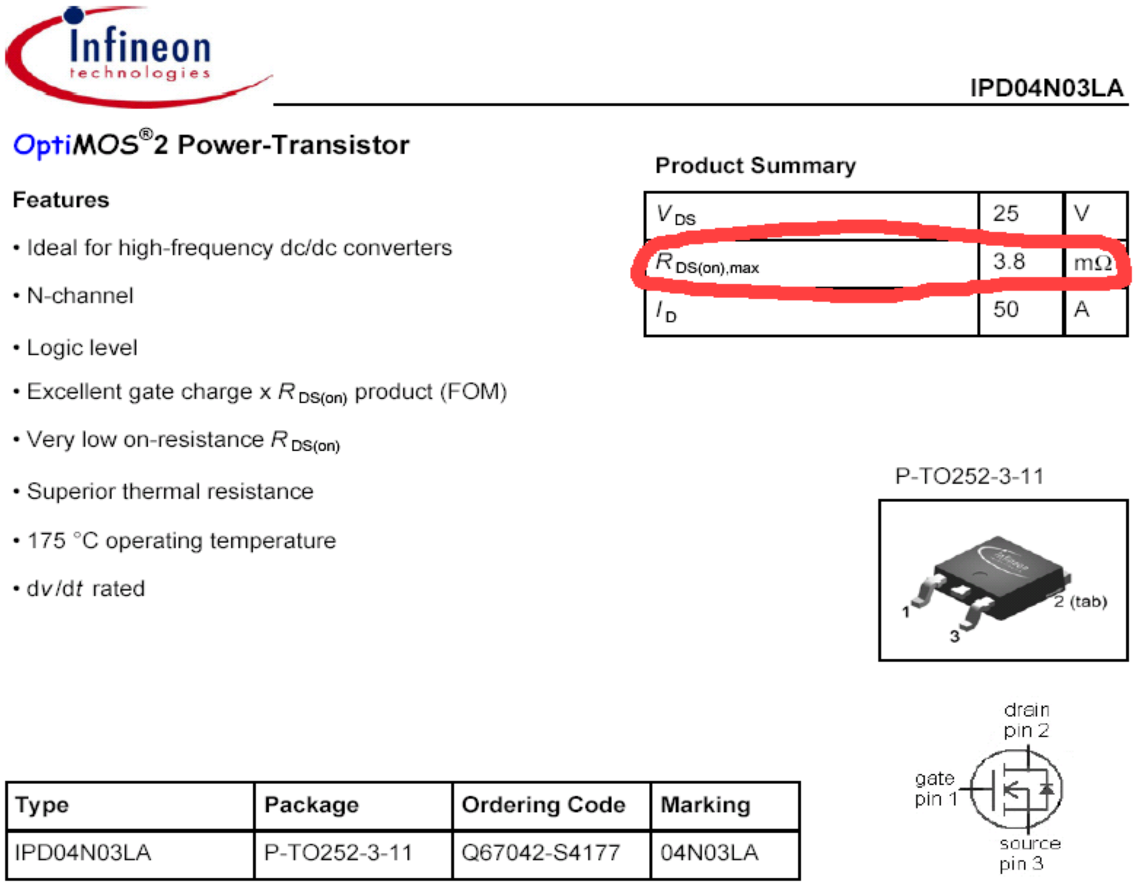
For a given MOSFET technology $R_{(DS)ON}$ and Q_G are opposite to each other. A MOSFET with a lower on-resistance has a higher gate charge and vise versa. The product of both parameters seems to be constant. It is called the Figure Of Merit (FOM) and defined as:

$$FOM = R_{(DS)ON} \cdot Q_G \tag{1}$$

The definition given above is not consistently used. This paper should help to compare MOSFETs and to calculate the FOM.

Calculation of the FOM

$R_{(DS)ON}$ and Q_G are parameters that depend on other conditions. Both are controlled by the gate-source-voltage. The $R_{(DS)ON}$ is also strongly influenced by the junction temperature. For the considerations here we will constitute a junction temperature of 25 ˚C. This is commonly used as the measurement condition for parameters in the datasheet.
In order to explain the calculation difficulties for the FOM we will have a look into a datasheet. As an example the Infineon OptiMOS®2 MOSFET IPD04N03LA will be used.



IPD04N03LA

OptiMOS®2 Power-Transistor

Features

- Ideal for high-frequency dc/dc converters
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- dv/dt rated

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	3.8	mΩ
I_D	50	A

P-TO252-3-11

Type	Package	Ordering Code	Marking
IPD04N03LA	P-TO252-3-11	Q67042-S4177	04N03LA

Figure 1

On the first page usually the $R_{(DS)ON}$ is given. The conditions are not specified here. This value has <u>only informal character</u> for the first choice of the MOSFET. It cannot be taken to compare the FOM since the conditions are not known.

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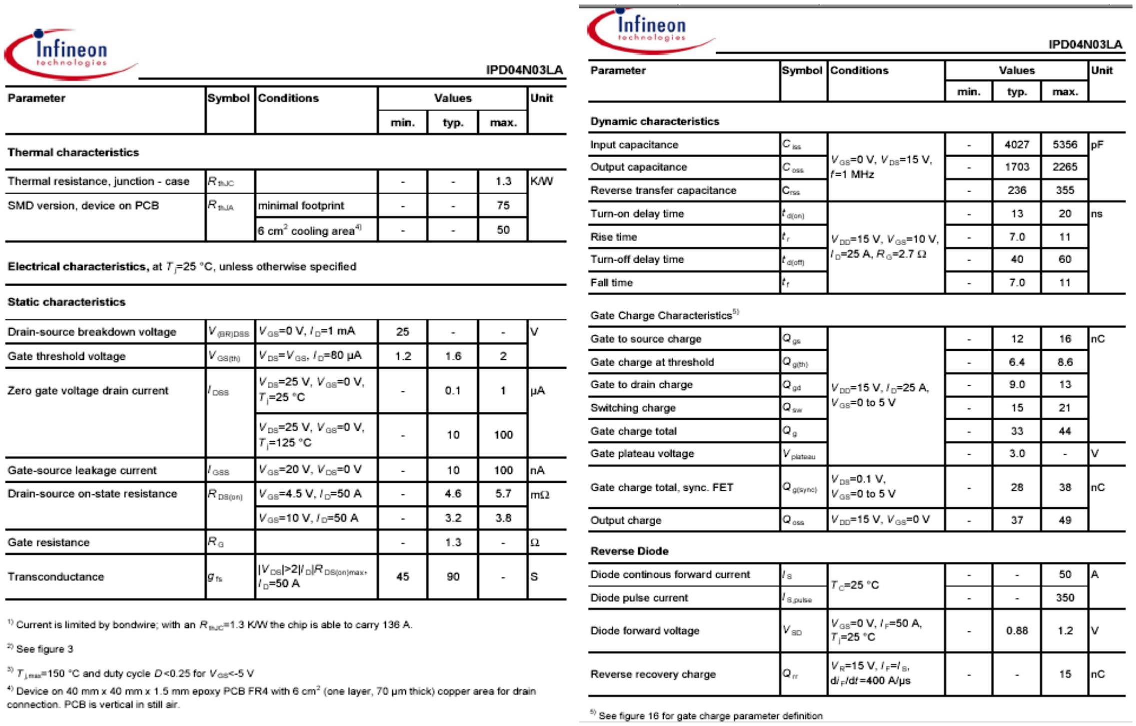
Figure 2 shows the second and the third page with the $R_{(DS)ON}$ and Q_G specifications and its conditions.



IPD04N03LA

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.3	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm^2 cooling area[4]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=80 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	4.6	5.7	mΩ
		V_{GS}=10 V, I_D=50 A	-	3.2	3.8	
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	45	90	-	S

[1] Current is limited by bondwire; with an R_{thJC}=1.3 K/W the chip is able to carry 136 A.

[2] See figure 3

[3] $T_{j,max}$=150 °C and duty cycle D<0.25 for V_{GS}<-5 V

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

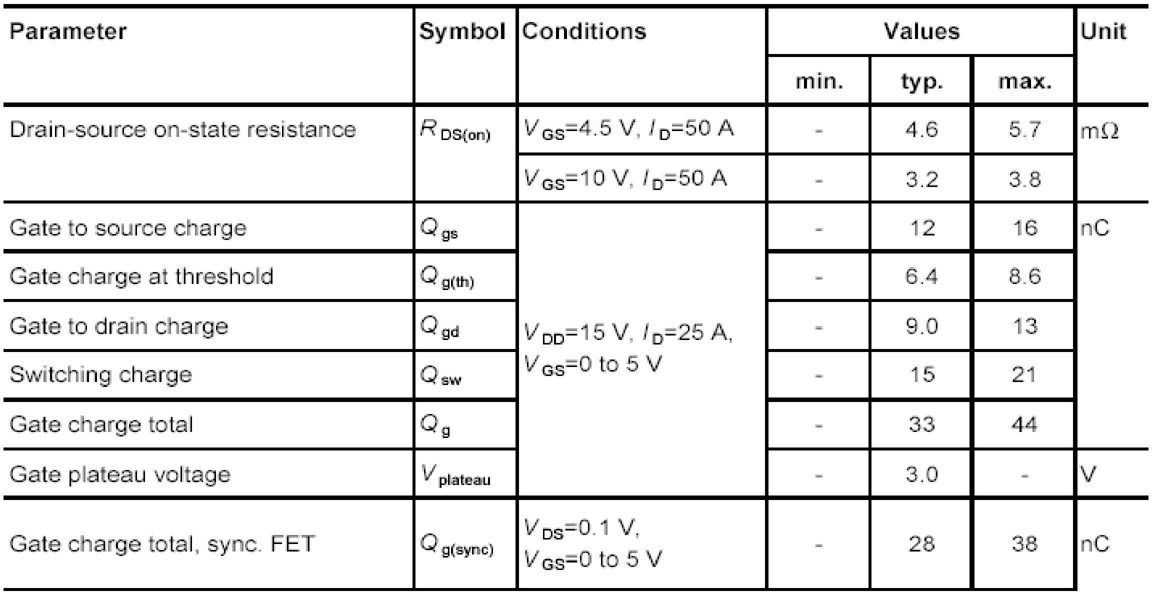
IPD04N03LA

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	4027	5356	pF
Output capacitance	C_{oss}		-	1703	2265	
Reverse transfer capacitance	C_{rss}		-	236	355	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=25 A, R_G=2.7 Ω	-	13	20	ns
Rise time	t_r		-	7.0	11	
Turn-off delay time	$t_{d(off)}$		-	40	60	
Fall time	t_f		-	7.0	11	
Gate Charge Characteristics[5]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=25 A, V_{GS}=0 to 5 V	-	12	16	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.4	8.6	
Gate to drain charge	Q_{gd}		-	9.0	13	
Switching charge	Q_{sw}		-	15	21	
Gate charge total	Q_g		-	33	44	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	28	38	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	37	49	
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	350	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	0.88	1.2	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	15	nC

[5] See figure 16 for gate charge parameter definition

Figure 2

The aggregation of the important parameters is shown in Figure 3.



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	4.6	5.7	mΩ
		V_{GS}=10 V, I_D=50 A	-	3.2	3.8	
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=25 A, V_{GS}=0 to 5 V	-	12	16	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.4	8.6	
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Gate charge total	Q_g		-	33	44	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	28	38	nC

Figure 3

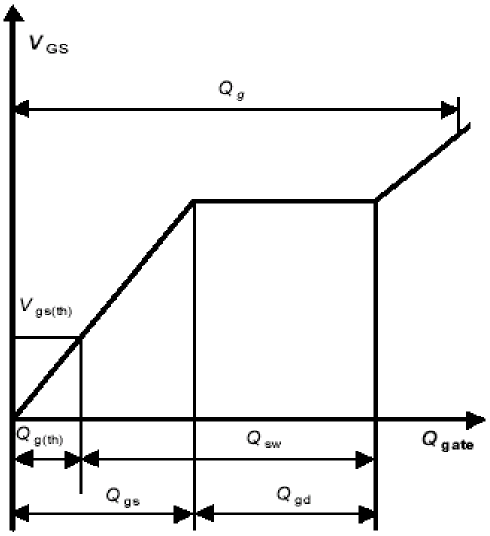

Figure 4

Figure 4 shows the differences in the gate charge parameters.

Q_{sw} is the so called switching charge. It applies for a V_{GS} between the threshold voltage and the first rise after the plateau voltage (the end of the plateau). During this phase the MOSFET changes from off-state to on-state. The shorter the time is when that happens the lower are the losses made during this transition. In other words – the lower the switching charge the lower the switching losses. The $R_{(DS)ON}$ depends on the gate-source-voltage and thus on the total gate charge at the applied V_{GS}. Total gate charge and switching charge are also a function of the drain-source-voltage.

Generally it is possible to take the lowest of the several $R_{(DS)ON}$ values and to multiply it with the lowest given gate charge value. The result would be a number which is nicely low but doesn't say anything about the MOSFET.

A sensible comparison of FOMs is only possible if made under the same conditions. First of all it has to be defined under what kind of voltage conditions (V_{GS}, V_{DS}) the FOM has to be calculated. That depends on the circuit requirements. Also it has to be determined what kind of FOM should be calculated, Q_{sw} x $R_{(DS)ON}$ or Q_G x $R_{(DS)ON}$. The voltage conditions have to be applied to both of the parameters identically (that means if V_{GS} is 5V, V_{DS}=12V then FOM(5V,12V)= Q_G(5V,12V) x $R_{(DS)ON}$(5V,12V)). Another important aspect is the choice of the right data columns – do you compare typical values or maximum values? Since the policies for the determination of maximum values are different in many companies the best choice is the comparison of typical values in order to evaluate the technology performance.

Let's assume the datasheet values have been taken under different conditions. Under these circumstances it is necessary to extract the typical values of the characteristic parameter diagrams. Figure 5 gives an example for getting the Q_G out of a characteristic diagram. V_{DS} is the parameter. Not every V_{DS} is given in the diagram. For missing values estimations have to be made. Figure 6 shows the dependency for the $R_{(DS)ON}$. Also here it is sometimes necessary to estimate not given values. Also it can be seen that the drain-current has a certain influence on the $R_{(DS)ON}$ and the comparison has be made with the same current.

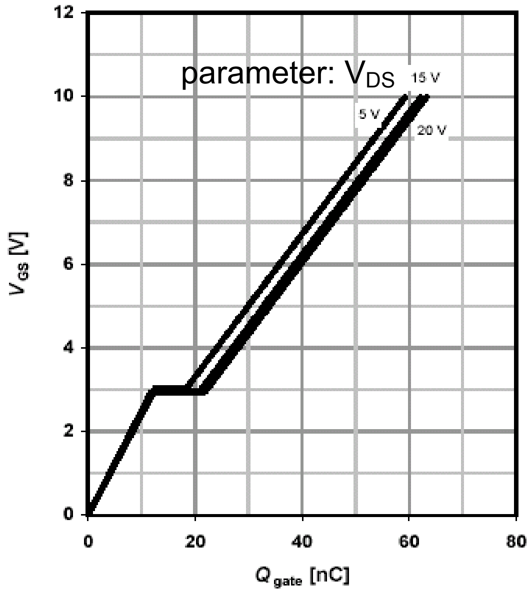

Figure 5

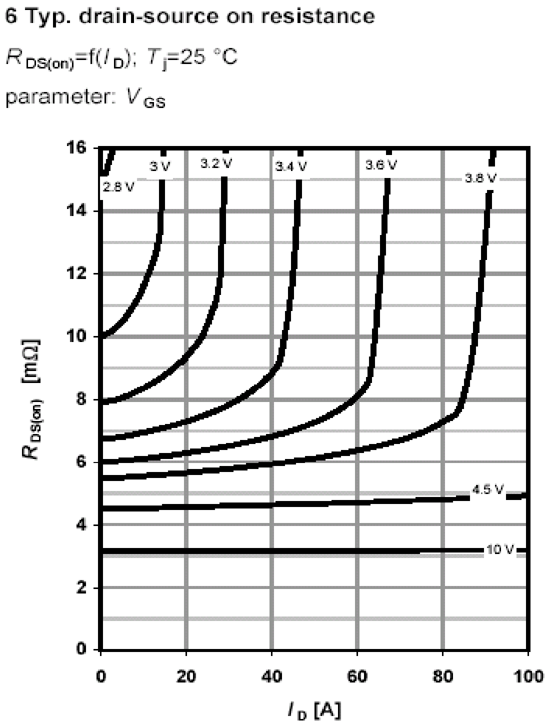

Figure 6

Conclusion

The comparison of MOSFETs of different vendors can be done by means of the Figure Of Merit under identical assumptions. Equations 2 and 3 describe how to calculate the FOM-values.

$$FOM(V_{GS}, V_{DS}, I_D) = R_{(DS)ON}(V_{GS}, I_D) \cdot Q_G(V_{GS}, V_{DS}) \qquad (2)$$

$$FOMsw(V_{GS}, V_{DS}, I_D) = R_{(DS)ON}(V_{GS}, I_D) \cdot Q_{sw}(V_{DS}) \qquad (3)$$

Important: For the calculation only the same kind of parameters can be taken, maximum or typical values for $R_{(DS)ON}$ and maximum or typical values for Q_G.