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Application Note

AN-CoolMOS-CP- 01

CoolMOS™ CP
- How to make most beneficial use of the latest generation of super junction technology devices

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Power Management & Supply

Never stop thinking

Revision History	
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1 Introduction

Today's trend in SMPS applications of system miniaturization and efficiency improvement put tough demands on power semiconductor performance. The new CoolMOS™ CP series meets these demands by offering a dramatic reduction of drain-source on-resistance (RDSon) in a given package, ultra-low total gate charge and a very low energy stored in the output capacitance. First 600V CoolMOS™ CP products were introduced during 2005 [1], with fill-up of product spectrum and introduction of a 500V class during 2006. This application note contains technical component details and a selection guide with design considerations.

Target applications for CoolMOS™ CP are server and telecom power supplies, notebook adapters, LCD TV, ATX and gaming power supplies and lighting ballasts, as outlined in Table 1. Table 2 gives a quick overview of available CoolMOS™ series today.

Application	PFC	PWM hard switching	PWM resonant switching
Topology	Conventional, Interleaved	TTF, ITTF, Flyback, Half-bridge	ZVS phase shift, res. HB, SRC, LLC
Adapter **ATX power supplies** **Server / Telecom** **LCD / PDP TV** **Lighting ballasts**	CoolMOS™ C3* CoolMOS™ CP**		CoolMOS™ CFD
	* Easy to design in ** Takes additional care for design-in		Highest reliability

Table 1 CoolMOS™ recommendation table for major applications.

	Market entry	*Voltage class [V]*	*Special characteristic*	*Vgs,th [V]*	*Gfs [S]*	*Internal Rg [Ohm]*
CoolMOS™ S5	1998	600	Low RDSon, Switching speed close to standard MOSFETs	4.5	Low	High
CoolMOS™ C3	2001	500/600/ 650/800	Fast switching speed, symmetrical rise/fall time at Vgs=10V	3	High	Low
CoolMOS™ CFD	2004	600	Fast body diode, Qrr 1/10th of C3 series	4	High	Low
CoolMOS™ CP	2005	500/600	Ultra-low RDSon, ultra-low Qg, very fast switching speed	3	High	Low

Table 2 CoolMOS™ series at a glance.

[1] The CoolMOS CS series is being absorbed into CoolMOS CP, employing same technology. CoolMOS CP series will be the umbrella series for all part numbers formerly shown as CoolMOS CS, with the only modification being the suffix change to CP from CS.

1.1 The Superjunction principle

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs and designed according to the superjunction (SJ) principle [1], which in turn is based on the RESURF [2] ideas being successfully used for decades in lateral power MOSFETs. Conventional power MOSFETs suffer from the limitation of the so-called silicon limit [3], which means that doubling the voltage blocking capability typically leads to an increase in the on-state resistance by a factor of five. The silicon limit is shown in Figure 2 where the area specific on state resistance of state-of-the-art standard MOSFETs as well are indicated. SJ technology may lower the on-state resistance of a power MOSFET virtually towards zero. The basic idea is to allow the current to flow from top to bottom of the MOSFET in very high doped vertically arranged regions. In other words, a lot more charge is available for current conduction compared to what is the case in a standard MOSFET structure. In the blocking state of the SJ MOSFET, the charge is counterbalanced by exactly the same amount of charge of the opposite type. The two charges are separated locally in the device by a very refined technology, and the resulting structure shows a laterally stacked fine-pitched pattern of alternating arranged p- and n-areas, see Figure 1. The finer the pitch can be made, the lower the on-state resistance of the device will be. With every CoolMOS™ generation the pitch is reduced, moving ever closer to the zero resistance point without losing voltage blocking capability.

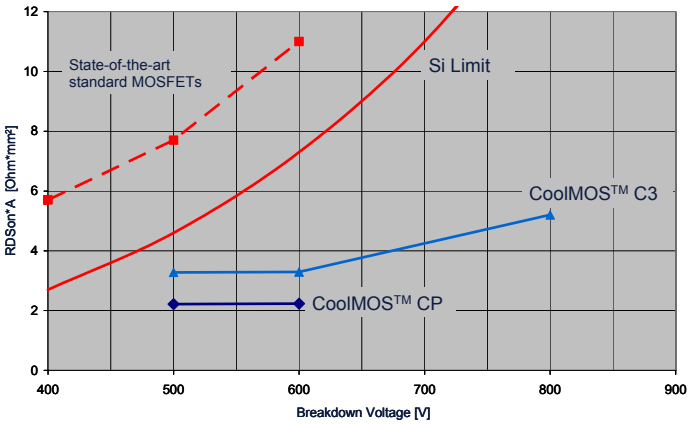

Figure 2 Area-specific RDSon versus breakdown voltage for standard MOSFET and CoolMOS™ technology.

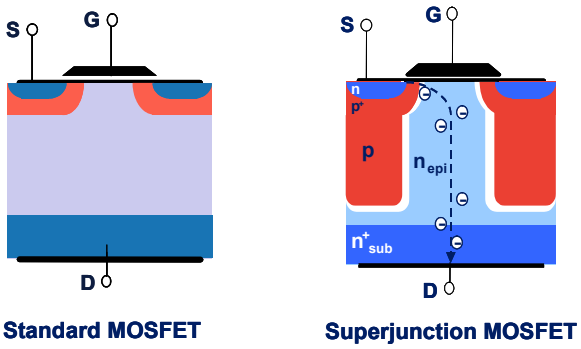

Figure 1 Schematic cross-section of a standard power MOSFET versus a superjunction MOSFET

Another signature of SJ technology is the extremely fast switching speed. The turn off behavior of a SJ MOSFET is not characterized by the relatively slow voltage driven vertical expansion of the space charge layer but by a sudden nearly intrinsic depletion of the laterally stacked p-n structure. This unique behavior makes the device very fast. The neutralization of these depletion layers is done via the MOS controlled turn-on of the load current for the n-areas and via a voltage driven drift current for the p-areas. SJ devices reach therefore theoretical switching speeds in the range of few nanoseconds.

Figure 3 shows a comparison of the figure-of-merit RDSon*Qg between the most advanced MOSFET technologies available in the market today.

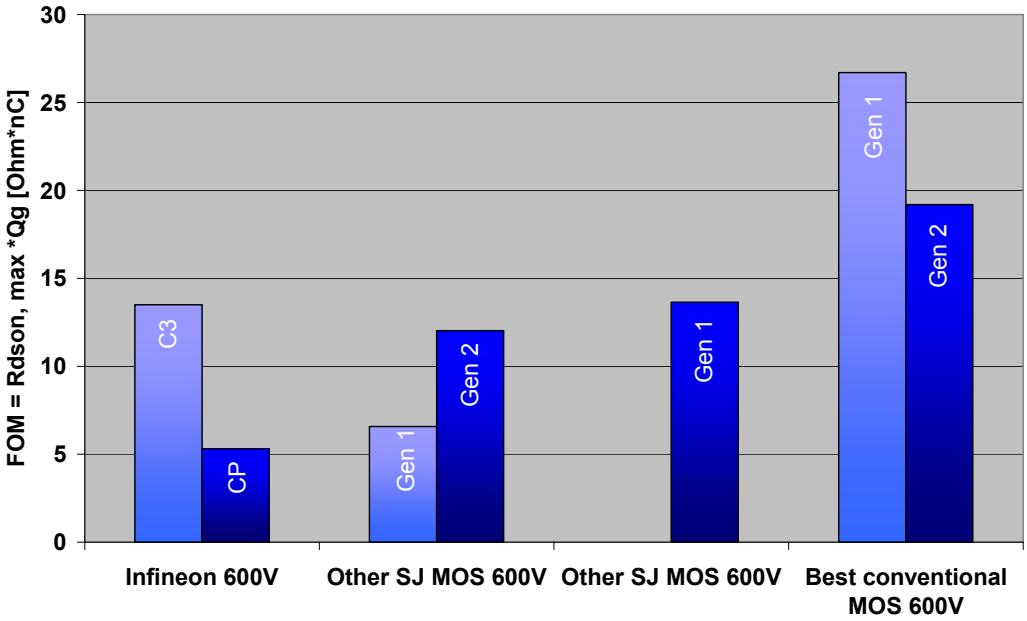

Figure 3 Comparison of figure-of-merit Rdson,max*Qg for most advanced 600V MOSFETs available in the market.

2 Technology Comparison of CoolMOS™ CP to C3

CoolMOS™ CP is the next step towards THE IDEAL HIGH VOLTAGE SWITCH with key features:

- ✓ Further reduced conduction and switching losses
- ✓ Lowest on-state-resistance per package @600V blocking capability
- ✓ Ultra-low gate charge and Lowest figure-of-merit R_{DSon} x Q_g

… which gives the application benefits:

- ✓ Extremely reduced heat generation
- ✓ Reduced system size and weight
- ✓ Very low gate drive power facilitating the use of low cost ICs and gate drivers
- ✓ Reduced overall system cost

To make an optimum MOSFET selection and apply it successfully, it's useful to first have a clear understanding of parameter differences with its predecessors. We present the key features of CoolMOS™ CP to C3 series in Table 3.

Specification	***Symbol***	***SPW20N60C3***	***IPW60R199CP***
On-state resistance, maximum rating, 25 °C	R_{DSon}	190 mΩ	199 mΩ
Drain current rating	I_D	20A	16A
FOM R_{DSon} x $Q_{g,total}$		16.5 ΩnC	6.4 ΩnC
Typical Gate to Source, Drain charge	Q_{gs}, Q_{gd}	11 nC, 33 nC	8 nC, 11nC
Typical C_{RSS} @ 50 V	C_{RSS}	9 pF	20 pF
Typical C_{RSS} @ 100 V	C_{RSS}	7.5 pF	1.8 pF
Energy stored in output capacitance @400V	E_{OSS}	10 µJ	7.5 µJ
Thermal resistance, junction-case	$R_{thJC,max}$	0.6 K/W	0.9 K/W
Gate threshold voltage, min…max	$V_{GS(th)}$	2.1… 3.9 V	2.5… 3.5 V

Table 3 Key features comparison of CoolMOS™ CP versus C3 series.

CoolMOS™ CP series has the world's lowest area-specific RDSon for 500V and 600V MOSFETs, which results in lowest RDSon per package type. Figure 4 shows technology advances in RDSon and current rating for 600V class MOSFETs in TO-220 package, from a 450 mOhm conventional MOSFET to superjunction MOSFETs. A TO-220 package in CP technology can handle an outstanding high continuous drain current of more than 30 A.

As the chip size for a given RDSon rating is smaller in CP technology compared to C3, the thermal impedance is higher and thus the current rating is slightly lower when comparing same RDSon. However, MOSFET selection should be made based on system thermal requirements, which means RDSon selection, and not on current rating. The slightly lower rating for CP compared to C3 has no affect in the majority of applications as nominal peak and rms currents are far below the rated currents in the datasheet. For peak current capability, there is no compromise between CP and C3 series.

The improvements in dynamic characteristics are substantial in CoolMOS™ CP. As shown in Figure 5, the gate to drain charge, Qgd, is greatly reduced and contributes to lower turn-on time and turn-off time. Furthermore, the output capacitance is as well reduced resulting in lower energy stored in the output capacitance, Eoss, for VDS=400V which is a key value for PFC and ZVS full-bridge topologies. As a consequence turn-on and turn-off switching power losses drop considerably for CP compared with C3 as seen in Figure 6. Eon is reduced by a factor of two, while Eoff is reduced by a factor of 3.3.

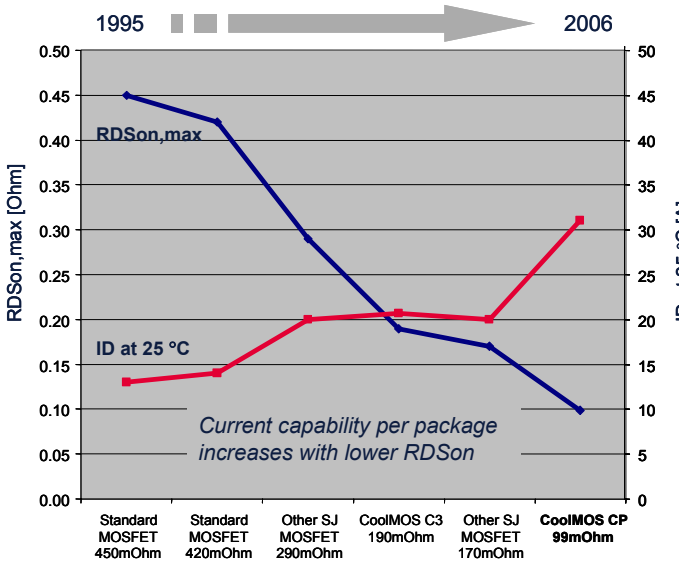

Figure 4 RDSon,max and nominal current rating for TO220 packages, showing technology advances over time for 600 V rated MOSFETs.

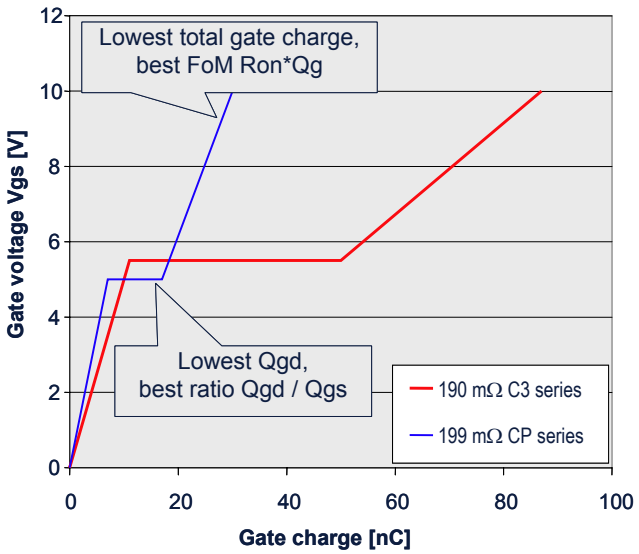

Figure 5 Gate charge characteristics comparison C3, CP.

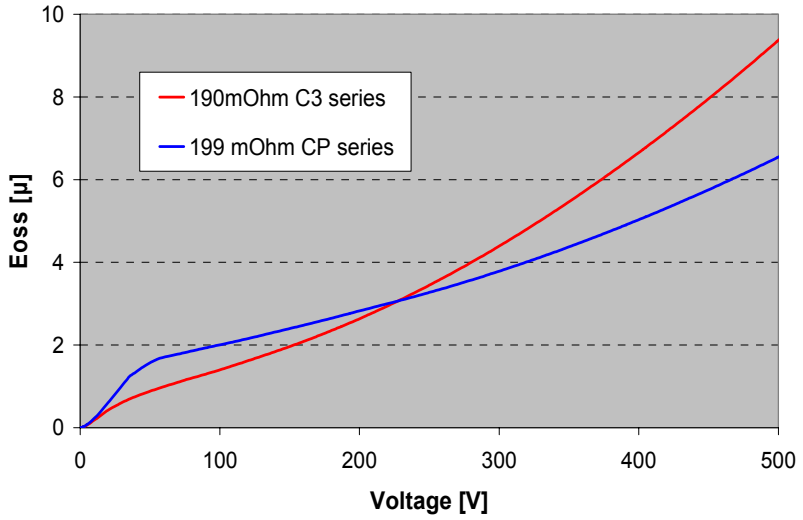

Figure 6 Comparison of energy stored in output capacitance CP to C3.

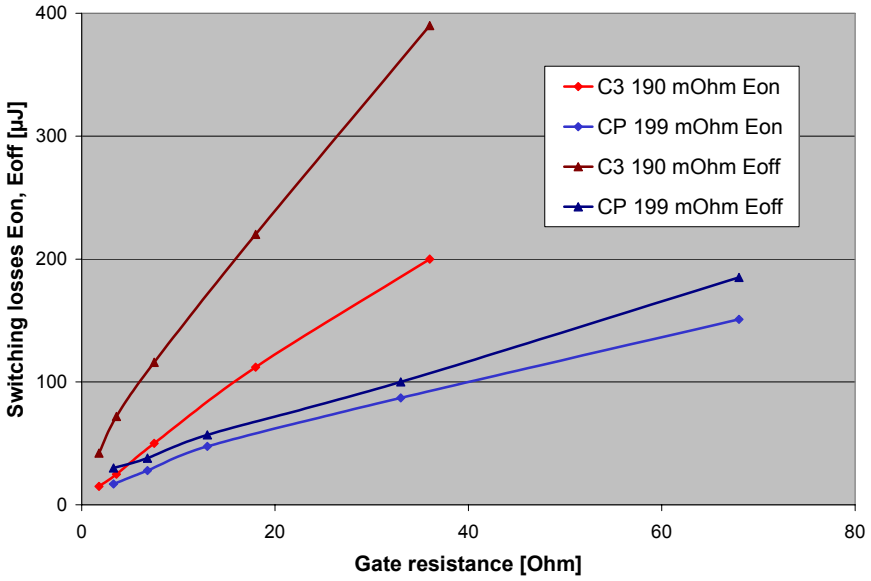

Figure 7 Comparison of switching power losses, CP vs. C3.

3 Dynamic Switching Behavior of CoolMOS™ CP

MOSFET switching is governed first and foremost about resistances (gate input) and capacitances (gate to source Cgs, gate to drain Cgd, and source to drain Cds), see Figure 8. With the very fast switching speed of CoolMOS™ CP, secondary effects become as well important, such as the influence of source circuit inductance and drain to source output capacitance. Behaviors may be seen, which are not usually encountered with conventional MOSFETs. Understanding these behaviors and using them to advantage within safe limits in the application requires a deeper look into the MOSFET switching behavior. Turn-on behavior is usually strongly influenced by the application circuit and associated components, but turn-off behavior is usually controlled just by the MOSFET, so this is the mode which will be examined closely in this section.
Note that for correlation with standard data sheet terms, Ciss = Cgs + Cgd, Crss = Cgd, and Coss = Cds + Cgd.

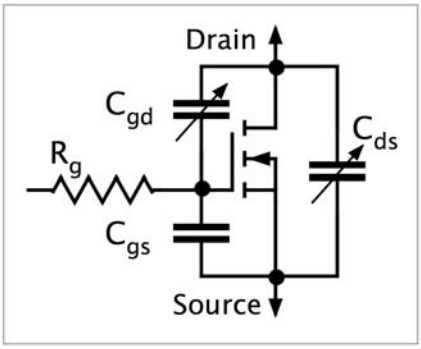

Figure 8 Elements controlling MOS switching.

3.1 Gate Controlled MOSFET Switching

Considering the diagram of Figure 9, the gate controlled MOSFET turn-off occurs in three fairly discrete intervals, and the behavior and losses for each interval is described separately below:
In the interval t1, the gate voltage is discharged to the current plateau level by the driver, with a time determined largely by Ciss, the gate input resistance RG, and the operating voltage levels for the gate drive and the plateau voltage determined by the MOSFET gfs and load current:

$$t1 = R_G \cdot C_{iss} \cdot \ln\left(\frac{V_{GDrv} - V_{G-Off}}{V_{Plat} - V_{G-Off}}\right) \quad (1)$$

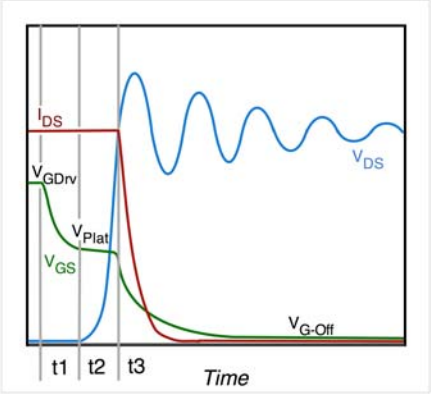

Figure 9 Example of gate controlled turn-off switching.

In the interval t2, the MOSFET is acting like an integrating amplifier, and the gate current supplied through Rg is that needed to charge Cgd as VDS rises, even while full ID current flows:

$$t2 = \frac{R_G \cdot C_{rss} \cdot V_{DS}}{V_{Plat} - V_{G-Off}} \quad (2)$$

During this gate controlled interval, where dVDS/dt is controlled by gate drive, the actual rate of change can be described by:

$$\frac{dV_{DS}}{dt} = \frac{V_{Plat} - V_{G-Off}}{R_G \cdot C_{Rss}} \quad (3)$$

In the final portion of turn-off, the gate drops below the plateau region, as RG discharges Ciss further, and ID falls following the MOSFET transfer function for ID as a function of VGS.

$$t3 = R_G \cdot C_{iss} \cdot \ln\left(\frac{V_{Plat} - V_{G-Off}}{V_{th} - V_{G-Off}}\right) \quad (4)$$

This turn-off behavior is shown in the simulation results of Figure 10, displaying the gate input waveform, drain to source voltage, and drain current. In this mode, the gate drive retains complete control over the dv/dt of the MOSFET, and is directly sizable by adjusting the size of the gate input resistor. However, as gate charge becomes lower in MOSFETs, and output capacitance non-linearity increases, using small values of gate drive resistance eventually shifts the switch-off behavior into a different mode.

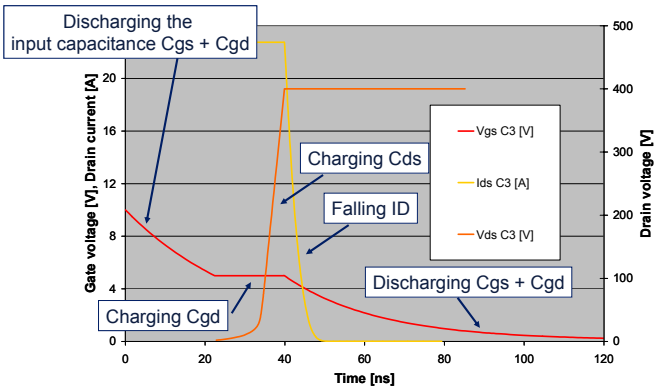

Figure 10 Turn-off simulation of CoolMOS™.

3.2 Quasi-ZVS Switching

Under conditions in which the gate drive turn-off is very fast, in combination with a relatively high Coss (as can exist in superjunction MOSFETs when the drain to source voltage is below 50V), the switching behavior will be dominated by somewhat different mechanisms, and the drain switching voltage will not be controlled by the gate drive current, but by Coss and load current. The behavior can still be roughly described by three main states Figure 11 but externally measured gate drive or drain current can be misleading in identifying these states. The t1 state is governed similarly as for the gate controlled dv/dt mode; the difference arises in the t2 region, where the gate discharging current is at such a high level such that the load current cannot begin to charge a voltage across COSS, and the channel current is turned off before the drain to source voltage rises. This is approximately described by:

$$t2 = R_G \cdot C_{iss} \cdot \ln\left(\frac{V_{Plat} - V_{G-Off}}{V_{th} - V_{G-Off}}\right) \quad (5)$$

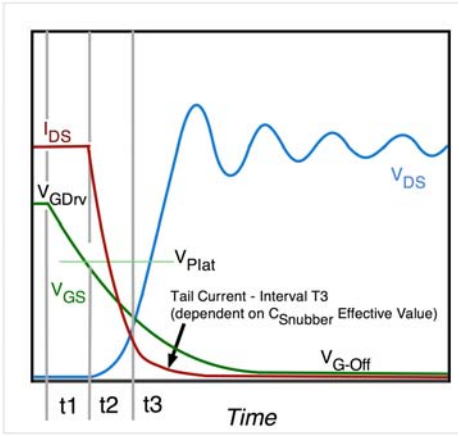

Figure 11 Quasi-ZVS Coss controlled turn-off.

This mode does result in very low turn-off losses, but it has some characteristics to consider that can become an issue in some applications, especially PFC converters with wide range of input current, and brief but high overloads.

Examining the capacitance curves of the two technologies, it is clear that CoolMOS™ CP has a substantially higher output capacitance below 50V. This is due to the smaller cell pitch compared to C3. As blocking voltage develops, around 50V there is a much more abrupt transition from a P-column structure to a planar depletion region, resulting in an order of magnitude drop in output capacitance over a small voltage range. This is the “ideal” characteristic for a low loss non-linear ZVS snubber - it keeps the output voltage rate of rise low initially while gate voltage is completing turn-off. Then, the output capacitance drops to a very low level, around 50 pF, permitting a very fast drain voltage rise. However, any possibility of drain control is lost because the low Qgd gate design means that gate-drain overlap capacitance is absolutely minimized, and as a result Crss drops to an astonishingly low value, less than 2 pF above 60V.

The impact of this can be seen even in simulation, where the dv/dt is controlled by Coss and load current in examples at 5A, 10A,

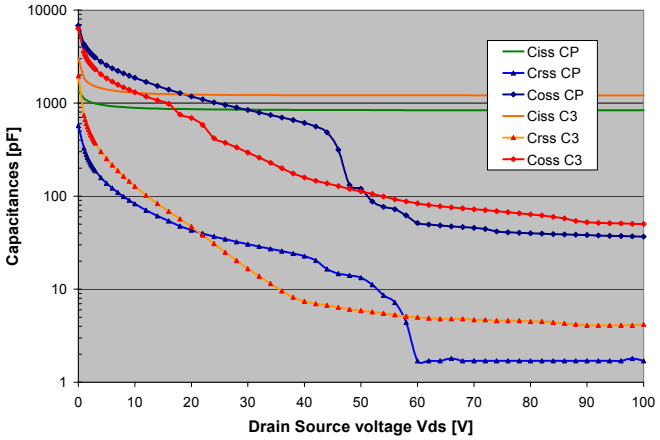

Figure 12 Device capacitances IPP60R385CP vs. SPP11N60C3.

and 30 (Figure 14). The Coss-controlled dv/dt is nearly doubled for CP compared to C3. In order to avoid excessively high dv/dt values, the first recommendation is to keep the turn-off transition in the gate controlled region under the highest load current condition occurring in the application. For example, in a forward converter the operating current range is relatively limited, and operating current tends to be low- Coss controlled turn-off will not result in potentially destructive dv/dt. However, in boost converters for PFC, the peak current is not necessarily under direct gate control, considering issues like input voltage transients and response delays in an average current mode controller. In that case, more care must be exercised.

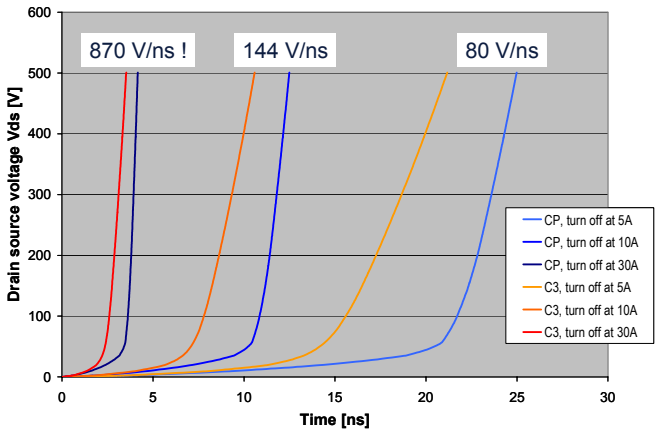

Figure 14 dv/dt simulation of CP, C3

The key to reliability under all conditions is maintaining device control. This means using gate drive to limit excessive di/dt and dv/dt by using the correct range for gate driver resistance. This is in principle no difference for CoolMOS™ CP than for C3. Transconductance for the two generations are actually quite similar, as the comparison in Figure 13 shows (190 mΩ C3, 199 mΩ CP). What happens when gate driver resistors are chosen outside a reasonable operating range? This is examined in the context of the 199/190 mΩ CP/C3 MOSFETs in next paragraph.

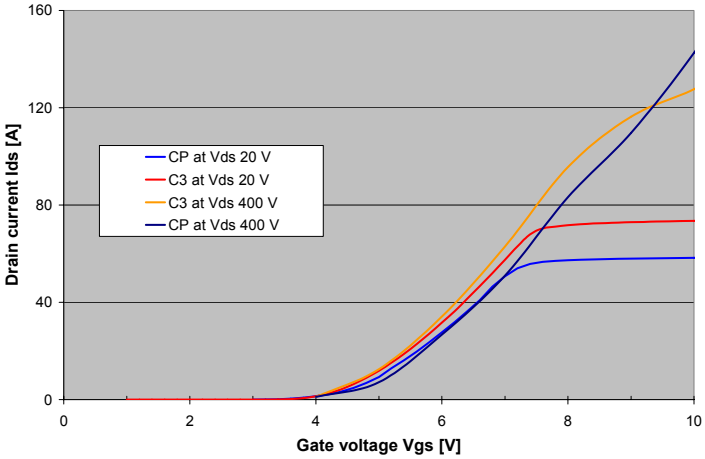

Figure 13 Transconductance characteristics of CP, C3

With very low values of gate driver resistance, di/dt is not under control of the MOSFET, but instead by the surrounding circuit elements. This is demonstrated in Figure 15 with the gate input resistor of 6.8 Ohm for an IPW60R199CP, and di/dt that rises quite rapidly with load current, until limited by external parasitic inductance. In this case di/dt can reach thousands of amperes per microsecond. With the gate resistor raised to 68 ohms, the picture is very different, and the rate of charging Cgs controls the di/dt independent of drain circuit loading, keeping peak di/dt in this case to a reasonable but fast 700A/µsec. A similar situation exists for controlling dv/dt, as would be expected.

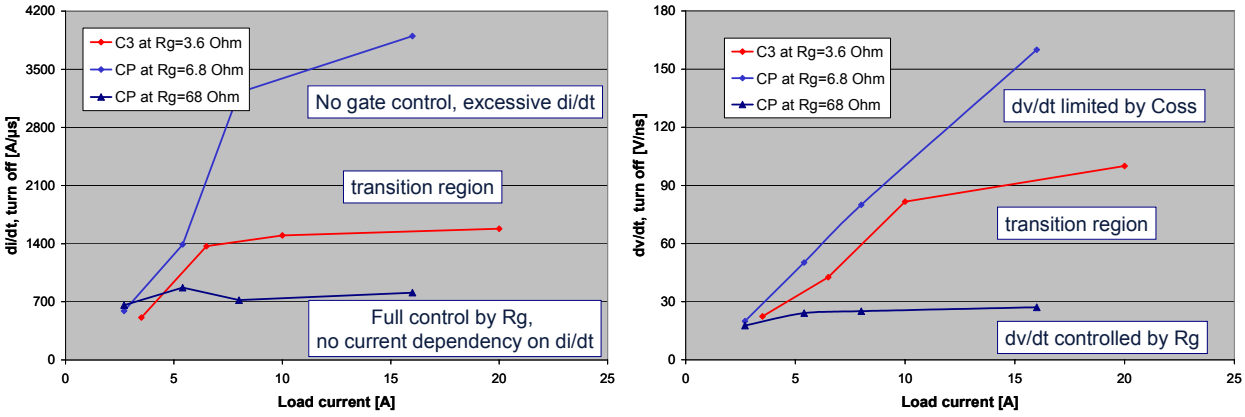

Figure 15 Left: di/dt for different load currents and gate drive resistance. Right: dv/dt for different load currents and gate drive resistance

In the case of IPW60R199CP with a gate resistor of 6.8 ohms, the turn-off is very fast, due to low gate charge and low output capacitance above 50V. The dv/dt shows a linear rise with increasing load current, indicating true ZVS turn-off of the MOS channel, and rise of drain voltage which is only a function of how fast the output load current can charge the output capacitance C_{OSS}.

The red curves shows what is called “transition region” behavior for C3 CoolMOS™, as the dv/dt is not completely controlled by output load current, and some gate control is still evident. With a gate resistance of 68 ohms, CoolMOS™ CP shows complete control of switching behavior by the gate, and drain to source dv/dt which is nearly invariant of load current. In this mode, the MOSFET is operating as an inverting/integrating amplifier, with the gate as a virtual AC ground. This is why the plateau region is fixed in voltage during switching. There is no feedback resistor, only the “integration” capacitance from the MOSFET C_{RSS} (gate to drain capacitance). At about 25 V/ns, drain switching speed is still fairly high compared with conventional MOSFETs, while remaining completely in control.

To summarize, dv/dt during turn off is limited either by discharging the gate-drain capacitance (Rg control) or by the charging rate of the output capacitance (Coss limited).

4 Circuit Design and Layout Recommendations

There are a number of recommendations to make with regards to circuit design and layout practices which will assure a combination of high performance and reliability. They can be recommended as if "in order of importance", but realistically all are important, both in contribution toward circuit stability and reliability as well as overall efficiency and performance. They are not that dissimilar to recommendations made for the introduction of MOSFETs compared to bipolar transistors, or CoolMOS compared with standard MOSFETs; it is a matter of the degree of care.

4.1 Control dv/dt and di/dt by proper selection of gate resistor

In order to exert full Rg control on the device maximum turn-off dv/dt we recommend the following procedure:

1. **Check for highest peak current in the application.**
2. **Choose Rg accordingly not to exceed 50V/ns.**
3. **At normal operation condition quasi ZVS condition can be expected, which gives best efficiency results.**

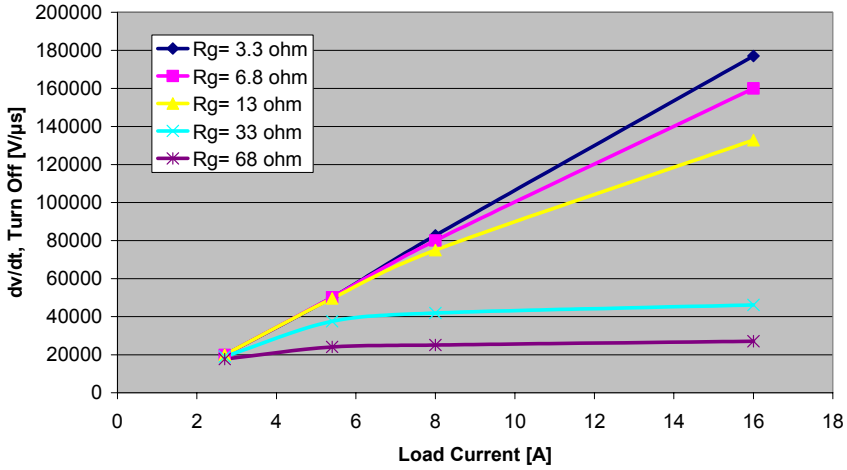

Figure 16 dv/dt for different load currents and gate drive resistances for IPW60R199CP (switching to 400V, Tj=125 °C).

Table 4 gives the Rg values for 50 V/ns and 30 V/ns at rated nominal current for each part as a quick guideline. Figure 16 also shows the turn-off dv/dt behavior for IPW60R199CP with several Rg values from 3.3 Ohms to 68 Ohms. An Rg value of 30 Ohm looks fairly optimal in order to exert full Rg for high currents and still keep quasi ZVS condition at lower currents. Keep in mind that the gate resistor scales with device size and area related capacitance. The value for Rg inversely scales with different MOSFETs. Further detailed switching characteristics can be found in Appendix.

CoolMOS™ Type	*RDSon,max*	*ID*	*Rg for dv/dt < 50V/ns*	*Rg for dv/dt < 30V/ns*
IPP60R385CP	**385 mΩ**	**9 A**	**30 Ω**	**64 Ω**
IPP60R299CP	**299 mΩ**	**11 A**	**30 Ω**	**62 Ω**
IPP60R199CP	**199 mΩ**	**16 A**	**30 Ω**	**60 Ω**
IPP60R165CP	**165 mΩ**	**21 A**	**26 Ω**	**50 Ω**
IPP60R125CP	**125 mΩ**	**25 A**	**19 Ω**	**37 Ω**
IPP60R099CP	**99 mΩ**	**31 A**	**15 Ω**	**28 Ω**
IPW60R045CP	**45 mΩ**	**60 A**	**10.5 Ω**	**17.5 Ω**

Table 4 Design guideline showing necessary gate resistance values for reaching dv/dt turn off values below 50 V/ns and 30 V/ns, respectively.

4.2 Minimize parasitic gate-drain board capacitance

Particularly care must be spent on the coupling capacitances between gate and drain traces on the PCB. As fast switching MOSFETs are capable to reach extremely high dv/dt values any coupling of the voltage rise at the drain into the gate circuit may disturb proper device control via the gate electrode. As the CoolMOSTM CP series reaches extremely low values of the internal Cgd capacitance (Crss in datasheet), we recommend keeping layout coupling capacitances below the internal capacitance of the device to exert full device control via the gate circuit. Figure 17 shows a good example, where the gate and drain traces are either perpendicular to each other or go into different directions with virtually no overlap or paralleling to each other. A “bad “ layout example is shown as reference to the good layout in Figure 19.

If possible, use source foils or ground-plane to shield the gate from the drain connection.

4.3 Use gate ferrite beads

We strongly recommend the use of ferrite beads in the gate as close as possible to the gate electrode to suppress any spikes, which may enter from drain dv/dt into the gate circuit. As the ferrite bead sees a peak pulse current determined by external Rg and gate drive, it should be chosen for this pulse current. Choose the ferrite bead small enough in order not to slow down normal gate waveforms but attenuation enough to suppress potential spikes at peak load current conditions. A suitable example is Murata BLM41PG600SN1, in an 1806 SMD package. It is rated for 6A current and a DCR of 10 mOhms, with about 50-60 Ohms effective attenuation above 100 Mhz.

4.4 Locate gate drivers and gate turn-off components as close as possible to the gate.

Always locate the gate drive as close as possible to the driven MOSFET and the gate resistor in close proximity of the gate pin (as an example, see R1 in Figure 17). This prevents it acting as an antenna for capacitively coupled signals. The controller/IC driver should be capable of providing a strong “low” level drive with voltage as near to ground as possible- MOS or bipolar/MOS composite output stages work well in that regard, due to low output saturation voltages. While some drivers may be deemed to have sufficient margin under static or “DC” conditions, with ground bounce, source inductance drop, etc, the operating margin to assure “off” mode can quickly disappear.

4.5 Use symmetrical layout for paralleling MOSFETs, and good isolation of Gate drive between FETs

We recommend the use of multi-channel gate drivers in order to have separate channels for each MOSFET. Physical layout should be as symmetrical as possible, with the low impedance driver located as close as possible to the MOSFETs and on a symmetric axis.

4.6 How to best make of use of the high performance of CoolMOS™ CP

To summarize, below recommendations are important when designing in CoolMOS™ CP to reach highest efficiency with clean waveforms and low EMI stress.

- ✓ **Control dv/dt and di/dt by proper selection of gate resistor**
- ✓ **Minimize parasitic gate-drain capacitance on board**
- ✓ **Use gate ferrite beads**
- ✓ **Locate gate drivers and gate turn-off components as close as possible to the gate**
- ✓ **Use symmetrical layout for paralleling**

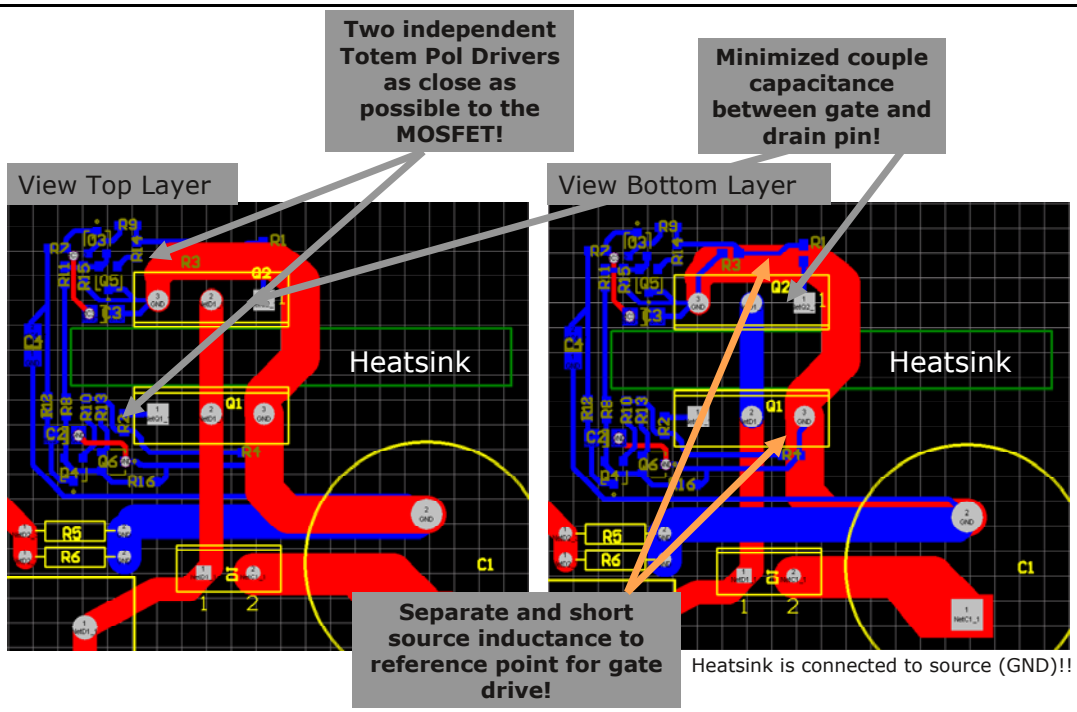

Figure 17 Good layout example ensuring clean waveforms when designing in CoolMOS™ CP.

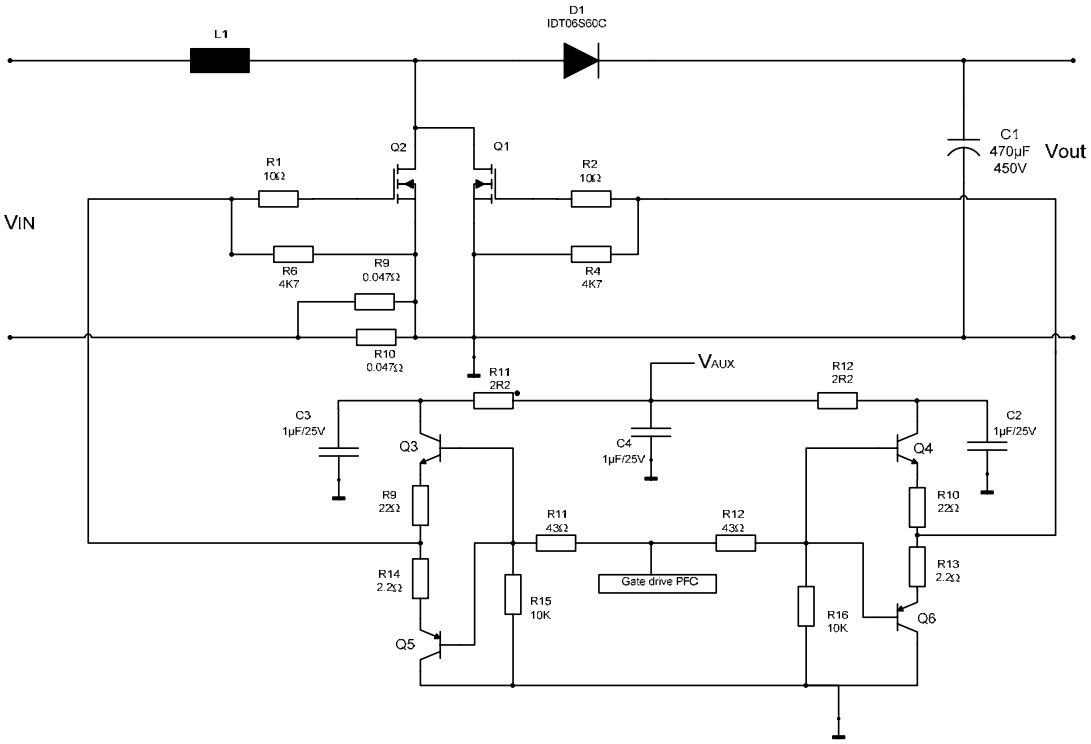

Figure 18 Good layout example showing schematic for PCB layout in Figure 17.

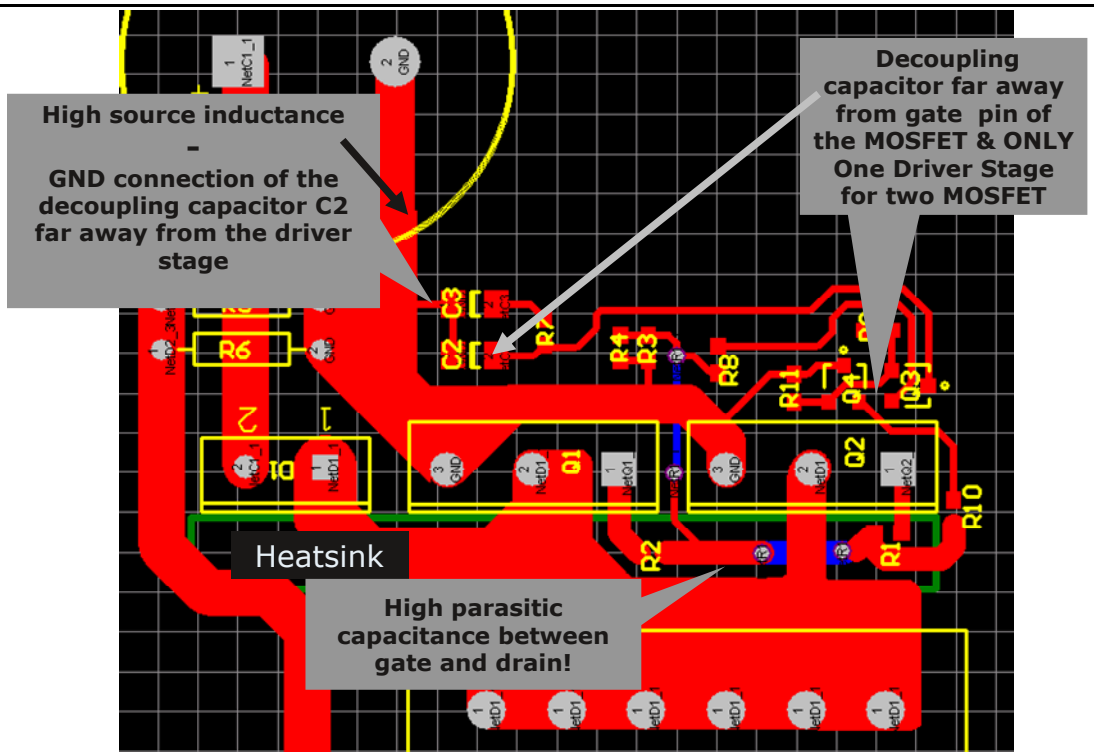

Figure 19 Bad layout example.

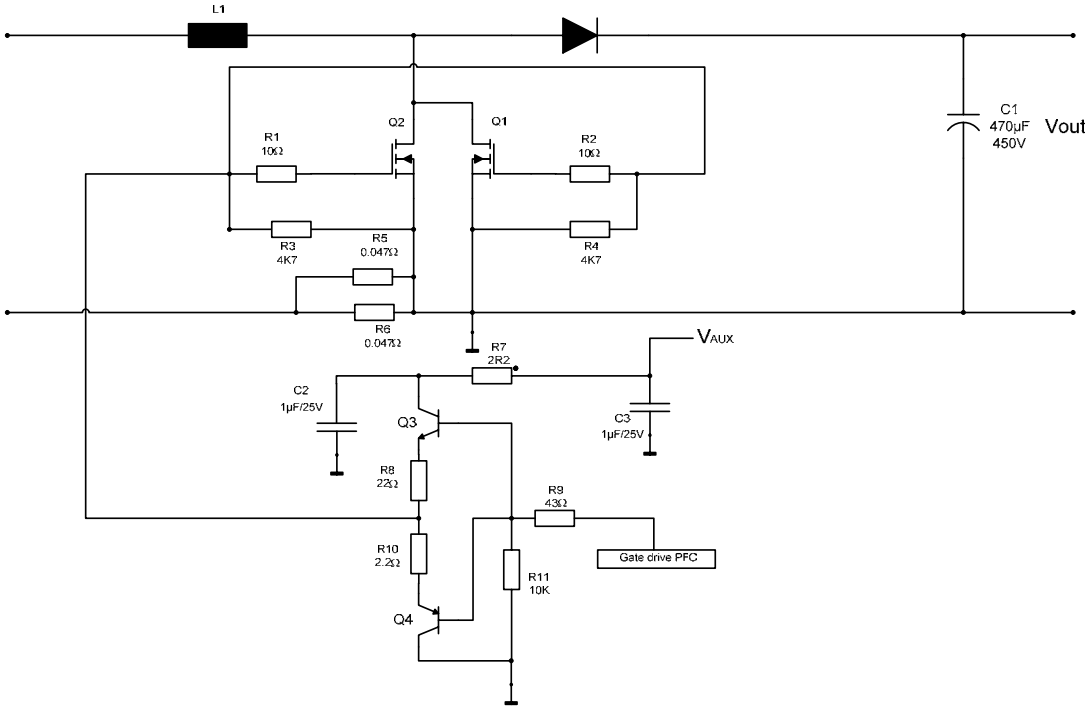

Figure 20 Schematic for bad layout example in Figure 19.

5 MOSFET Selection for the Application Based on Loss Balance

Final thoughts will be offered on optimizing the SMPS performance and cost through analysis of loss balance. For any given MOSFET technology there is a figure of merit based upon the balance of resistive losses and dynamic losses.
Improved MOSFET technologies will offer lower Coss related losses in proportion to Ron. If a specific application is examined with regards to the RMS conduction loss based on the variable RDS[on] and the switching loss based on dynamic factors (usually a combination of Coss pumping loss and crossover transition loss) a chip size with even balance of losses will provide the minimum total loss at the full load operating point. However, the slopes of the loss factors are not equivalent, and so considering the widest range of operating loads, the best efficiency and economics may occur working in a mode with higher conduction than switching losses at full load, especially in the case of redundant configured power supplies that normally operate at less than 1/2 of rated maximum output.
The analysis problem can be approached from a few different angles. Let's take as a starting example an interleaved two transistor forward converter (ITTF) designed for 1 kW output power, with the assumption of about 90% efficiency, which will require an input power of about 1100W. The maximum output current in the switches at minimum bus voltage has been calculated using:

$$I_{PEAK\_Sw} = \left(\frac{P_{Out\_Max}}{2 \times V_{In\_min} \times D_{max}} \right) = 3.67A \quad (6)$$

where VIn_min is the minimum operating bulk bus voltage, POut_Max is the output power, and Dmax is the calculated maximum duty cycle (based on transformer turns ratio primary to secondary). Let's say that as a first pass the best in class TO220 600V CP CoolMOS™ is chosen for consideration due to its very low RDS[on] for this package type. Then, the conduction loss can be calculated for an elevated junction temperature RDS[on] of 150 mΩ from

$$Pd_{Conduction} = \left(I_{Peak\_Sw}\right)^2 \times R_{DS[on]}(T_J) = 0.252 \text{ Watt} \quad (7)$$

This looks good, but perhaps too good? What about dynamic losses? As a first cut, the Coss pumping losses can be estimated from the energy equivalent output capacitance (CO(ER)) (integrated over 0 to 480V) in the datasheet:

$$Pd_{Coss} = \frac{1}{2} \times C_{O(ER)} \times V_{In\_Max}{}^2 \times f_S = 1.526 \text{ Watt} \quad (8)$$

Notice the imbalance in losses in this preliminary calculation. Switching losses can be further investigated using Eon and Eoff curves. These curves can be found in Appendix. The principle is the same, multiplying Eon and Eoff times the switching frequency, and summing the results.

Another more conventional, perhaps simplistic, approach is to estimate the dynamic losses just from the crossover times (Eqn 9), which may be reasonably valid in the gate control switching region discussed earlier.

$$Pd_{Switching} = \left(\frac{V_{In\_max}}{2} \right) \times I_{Peak\_Sw} \times \left(t_{on} + t_{off}\right) \times f_S = 2.028 \text{ Watt} \quad (9)$$

The picture which is clearly emerging, though, is that for a 1 kW, 130 kHz ITTF converter the 60R099 is more silicon than optimum. A detailed investigation will show that the 60R199 will offer about 15-20% lower losses, and much better economics.
In Figure 21 the total conduction and capacitive losses are analyzed with RDSon being the variable function. Switching losses are not taken into account as they do not depend on RDSon. This example is built around an 500W TTF (two transistor forward) stage, 130 kHz and the junction temperature for calculation purposes is 105 °C.

Compared even with other superjunction MOSFETs, the very low dynamic losses of CoolMOS™ CP can match the overall losses of competitors while having a 60% or higher RDS[on]. This conveys some significant advantages in chip size, package options, and cost, as well as opportunities to improve performance and thermal density.

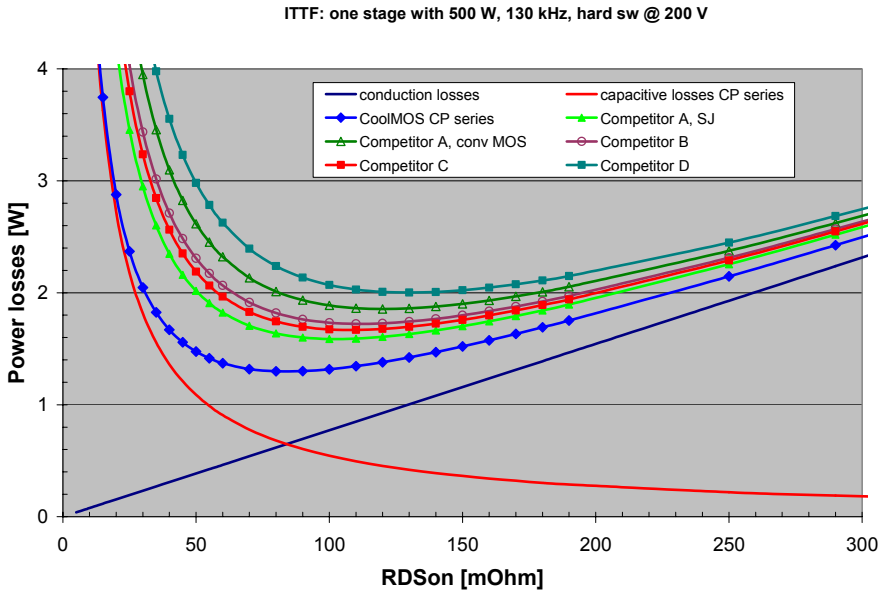

Figure 21 Calculated total power losses as a function of RDSon for one 500W TTF, as an example of 1000W ITTF, with switching frequency= 130 kHz, Tj=105°C.

How does this workout in more demanding applications, such as wide input range power factor correction with a high clock frequency to reduce the boost inductor size? In this case, the performance of the boost rectifier diode in continuous conduction mode PFC is the gating factor- having a direct influence on the turn-on losses observed in the MOSFET. By using a **thinQ! 2G™** silicon carbide Schottky diode, a nearly ideal diode is possible, and the switching losses are governed mostly by the MOSFET capabilities. The results are seen in the graph of Figure 22, which shows the possibility of matching power losses at full load with a MOSFET of much higher RDSon. Besides the economic reasons for doing this, the reduction in output capacitance related dynamic losses with the smaller chip MOSFET will pay back good dividends with improved moderate and low load efficiency, especially at high line operation.

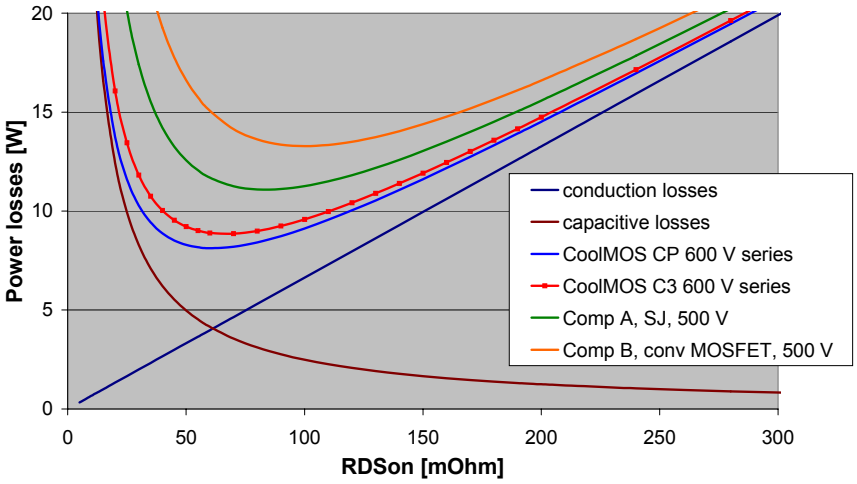

Figure 22 Calculated total Losses as a function of RDSon for an 800W PFC converter, with switching frequency=250 kHz, 110 V input voltage.

6 Examples of Application Benefits with CoolMOS™ CP

With today's trend of universal input voltage range for world-wide use, a low RDSon becomes a key requirement in active PFC converters as under low line conditions power losses are at its peak due to maximum current requirement.

Replacement of several paralleled MOSFETs by fewer components of new CooMOS™ CP series

Reduction of part count will save space on the PCB board and largely facilitate gate driving. Especially versatile replacements are 2x 190mOhm or 2x 170mOhm by 1x 99mOhm, or 3x 190/170mOhm by 2x 125mOhm. The design will benefit from a lower energy stored in the output capacitance, lower gate drive power and the higher switching speed. With the highest thermal resistance being heat sink to ambient the effective increase of thermal resistance junction to ambient is relatively small. The reduction of number of parts is therefore highly applicable.

Example 1: 600 W CCM PFC stage, 130 kHz

Different power MOSFETs, all TO220 packages, were measured under low-line condition 90VAC. Highest PFC efficiency was obtained with one 99 mOhm CoolMOS™ CP (Figure 23). The reference parts were rated at 500V in order to use lowest available RDSon in the comparison.

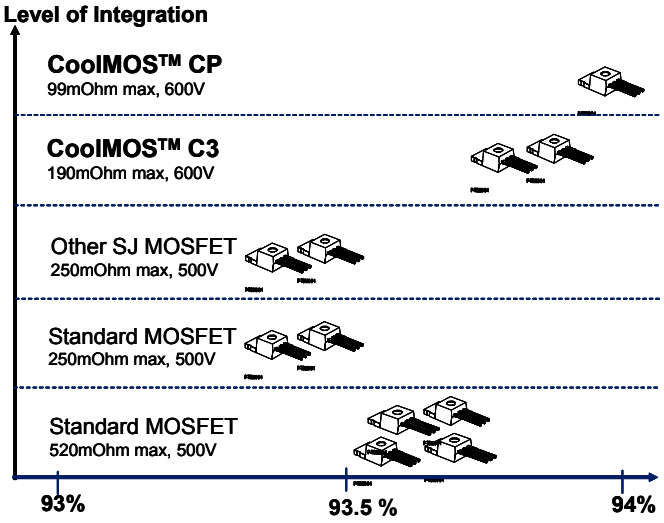

Figure 23 Level of integration for TO220 MOSFET devices in a 600 W CCM PFC stage, 130 kHz, 90VAC input voltage. *Source: ISLE Institute, Germany.*

Example 2: 800 W Evaluation server board

An 800W Evaluation server board was designed with 85…265VAC input and 1U form factor. **The PFC stage uses one TO247 600V CoolMOS™ CP with 45 mOhm**, as shown in Figure 24. Further information about the evaluation board can be found in an application note [5].

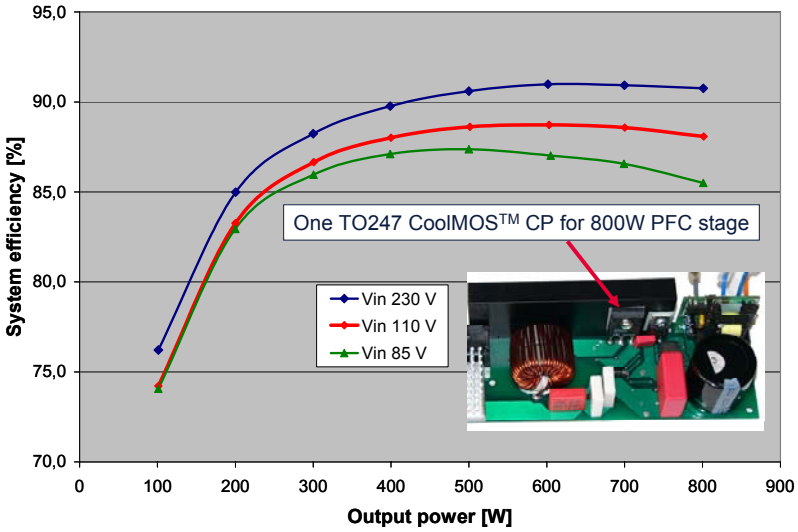

Figure 24 System efficiency versus load for different input voltages of an 800W Evaluation server board.

For hard-switching applications such as CCM PFC, two-transistor forward (TTF), interleaved TTF, and half-bridge, CoolMOS™ CP is the ideal switch

Example 3: 500W Silverbox using TTF topology

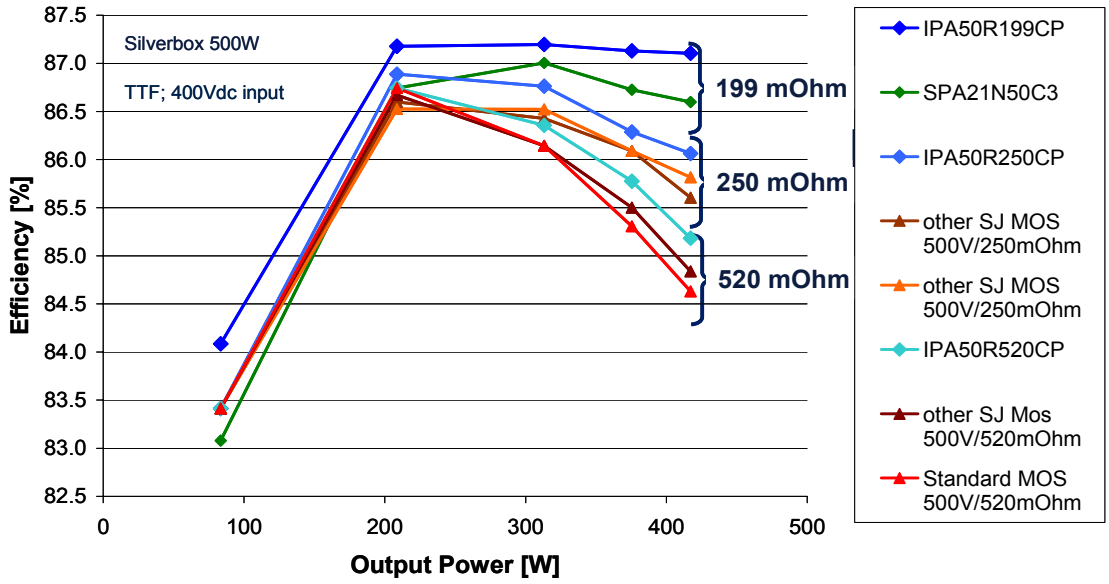

Figure 25 DC-DC stage efficiency for a 500W Silverbox (commerciably available), comparing 500V CoolMOS™ CP with other 500V MOSFETs.

As seen in Figure 25 500V CoolMOSTM CP gives lowest efficiency per RDSon class in a TTF stage in a 500W commerciably available silverbox power supply.

CoolMOS™ CP enables higher operating frequencies

Changing from less advanced SJ technologies or conventional MOSFETs to new CoolMOS™ series with identical RDS,on enables a higher system frequency. The much faster switching speed, lower energy stored in the output capacitance and lower required gate drive power will enable a higher operation frequency, for example up to 130 kHz or 250 kHz. This will result in smaller passive components and hence a reduction in form factor.

7 Product Portfolios

With CoolMOS™ CP series a new naming system for CoolMOS™ products is taken into place, explained in Figure 26.

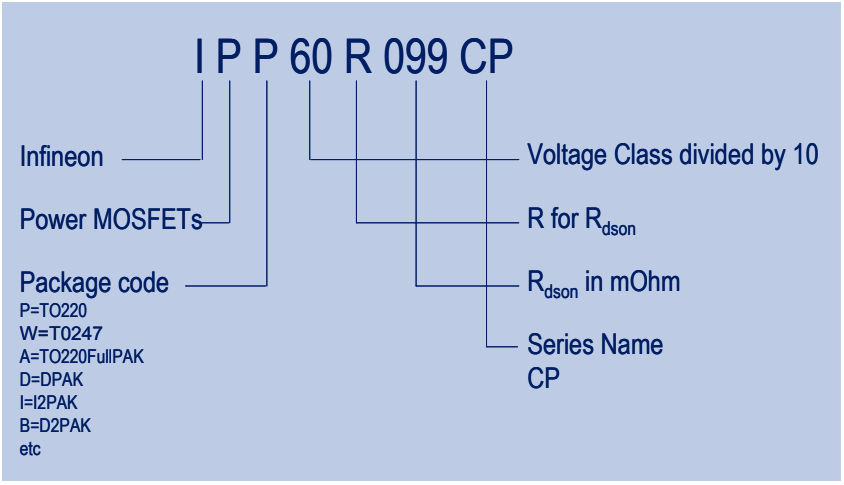

Figure 26 Naming system for CoolMOS™ CP products.

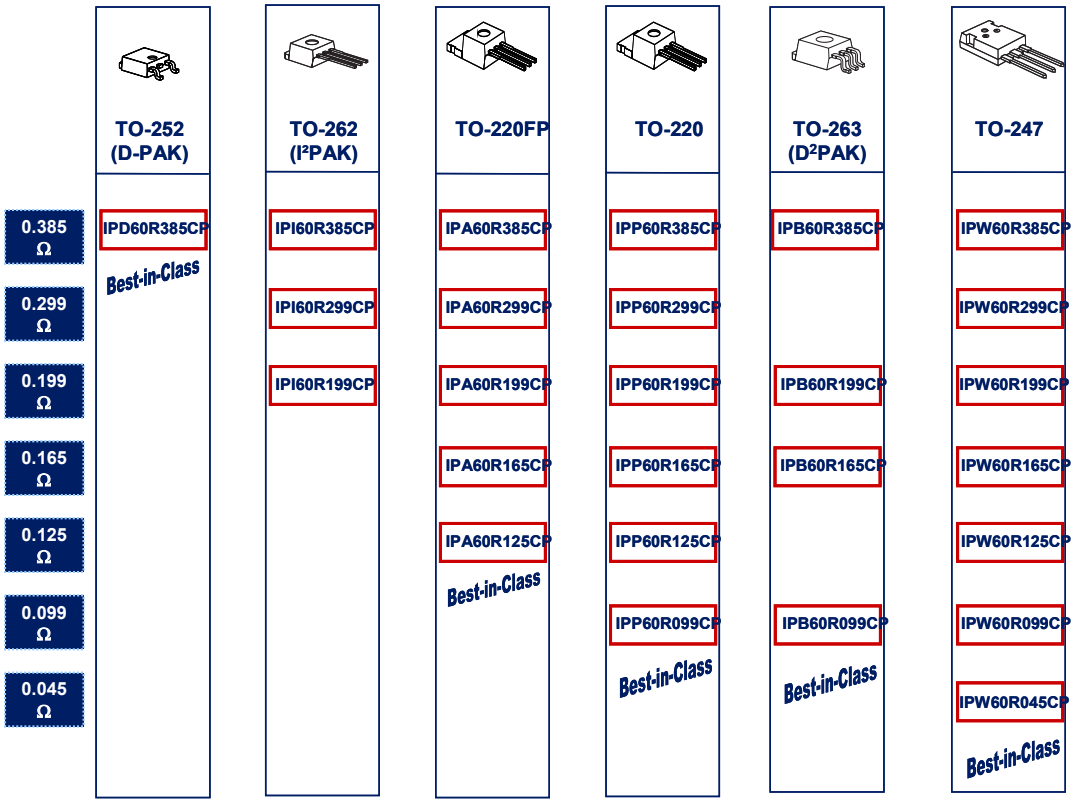

Figure 27 CoolMOS™ CP 600V products

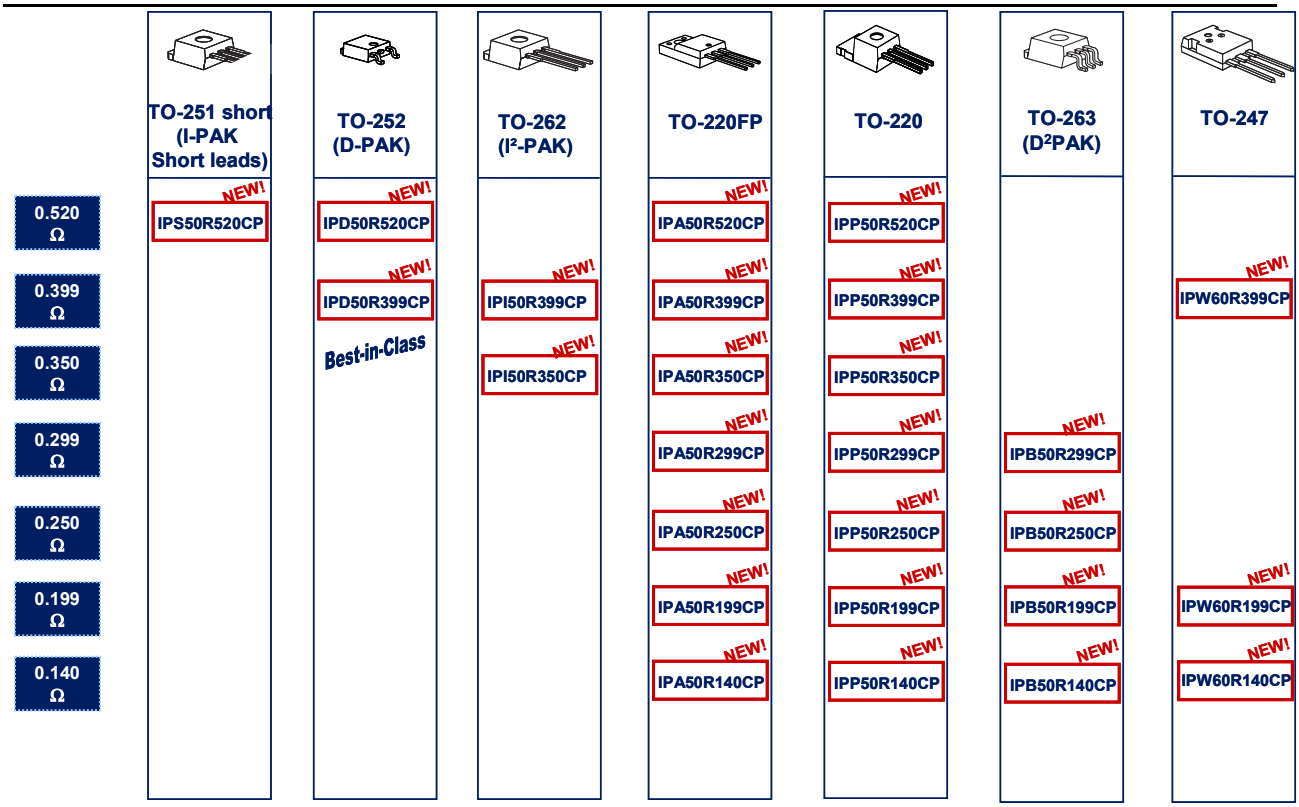

Figure 28 CoolMOS™ CP 500V products

8 References

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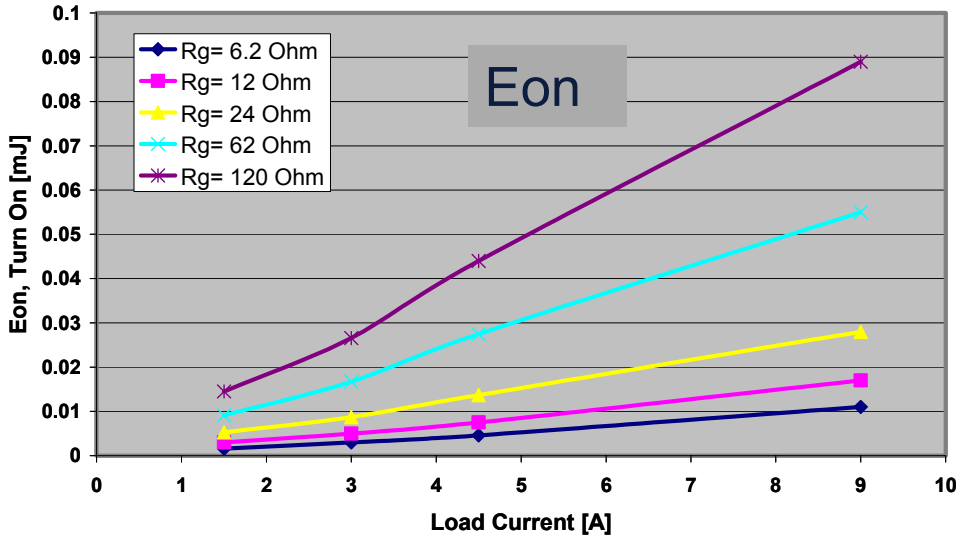
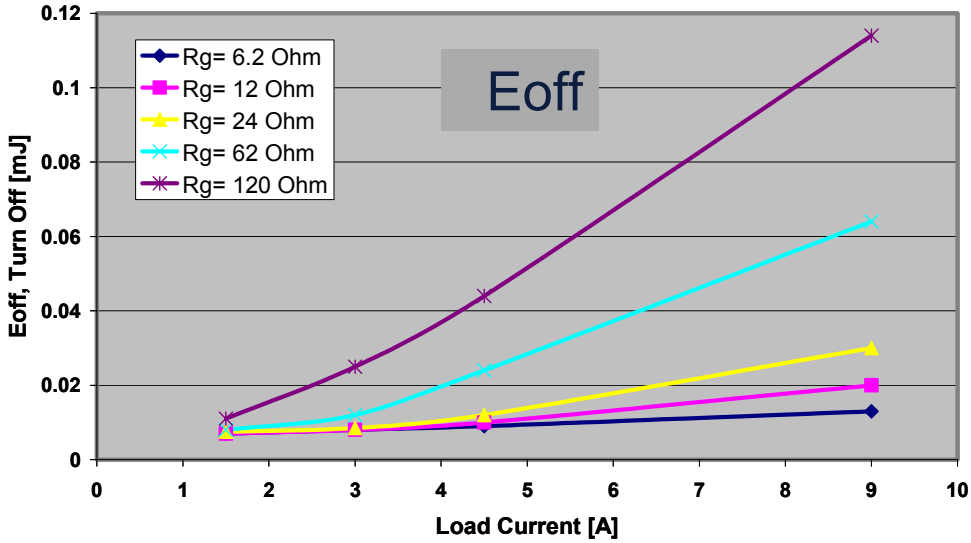
Appendix – Typical Dynamic Switching Characteristics of CoolMOS™ CP 600V

IPP60R385CP, Tj = 125 °C, VGS=+13 V / 0 V





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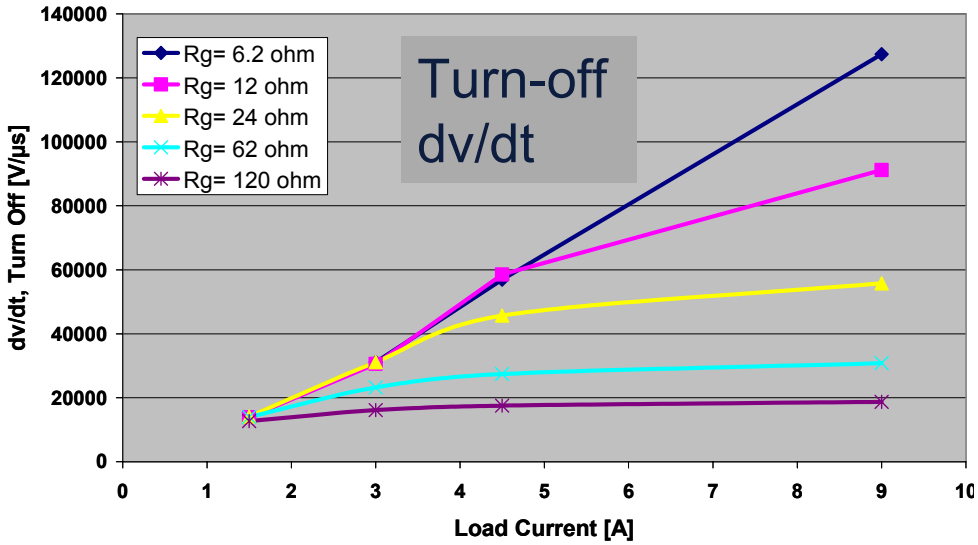

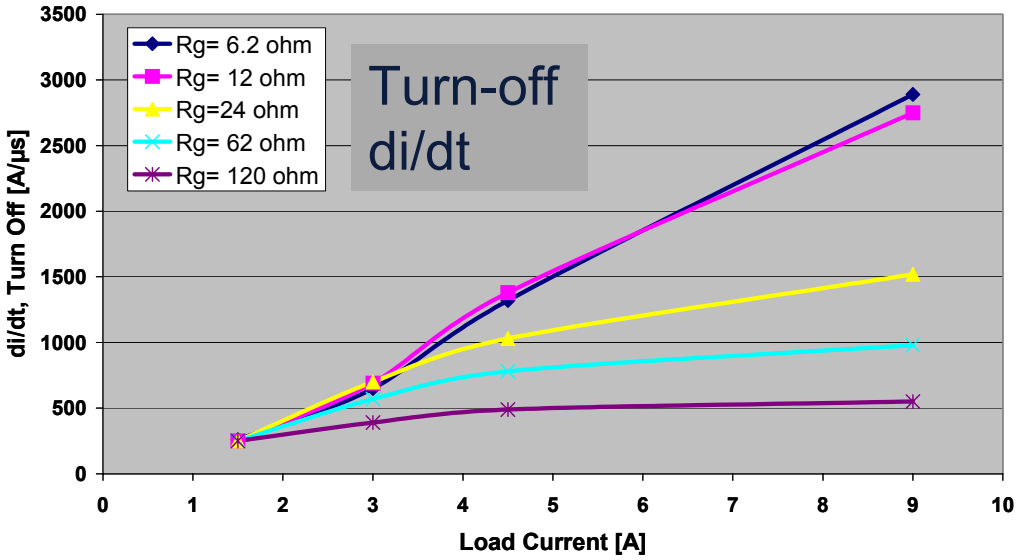

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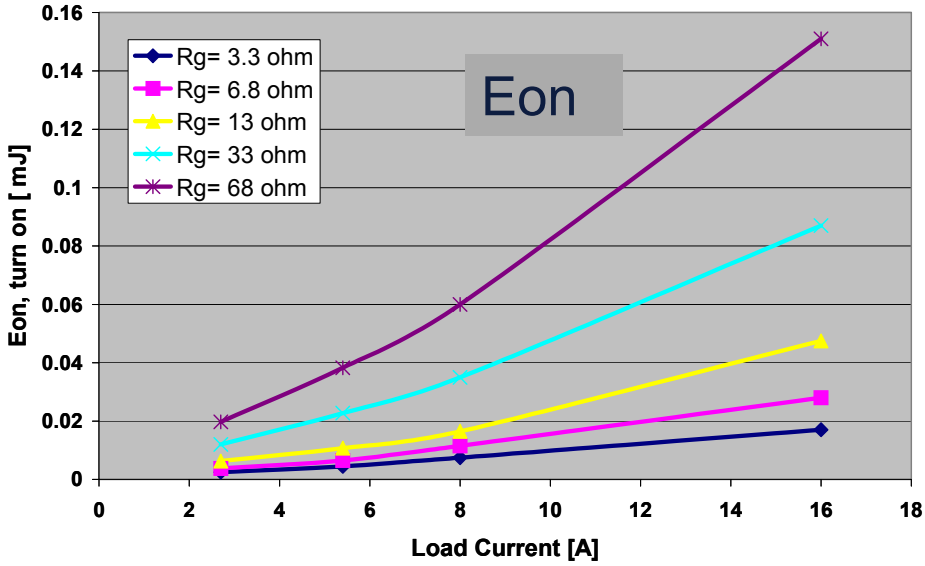

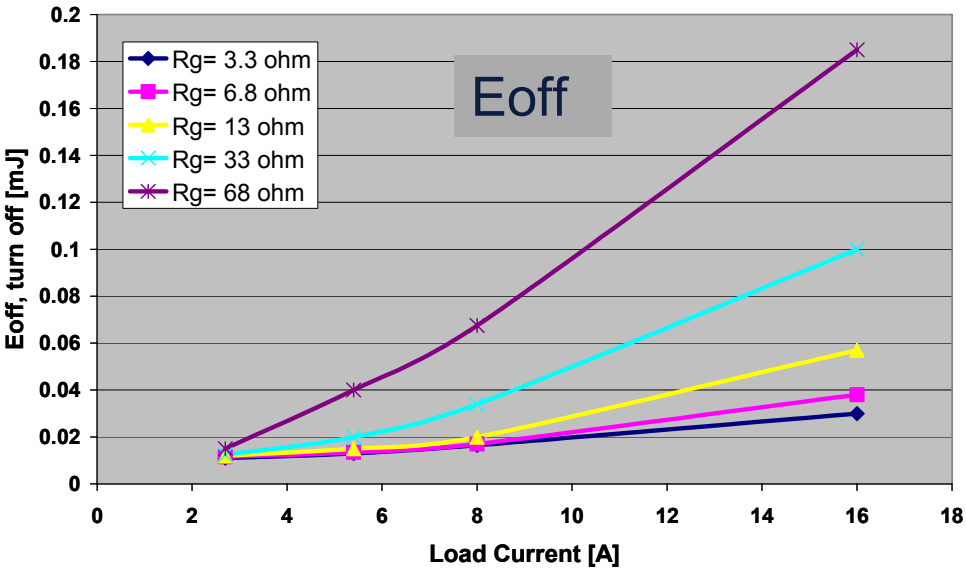

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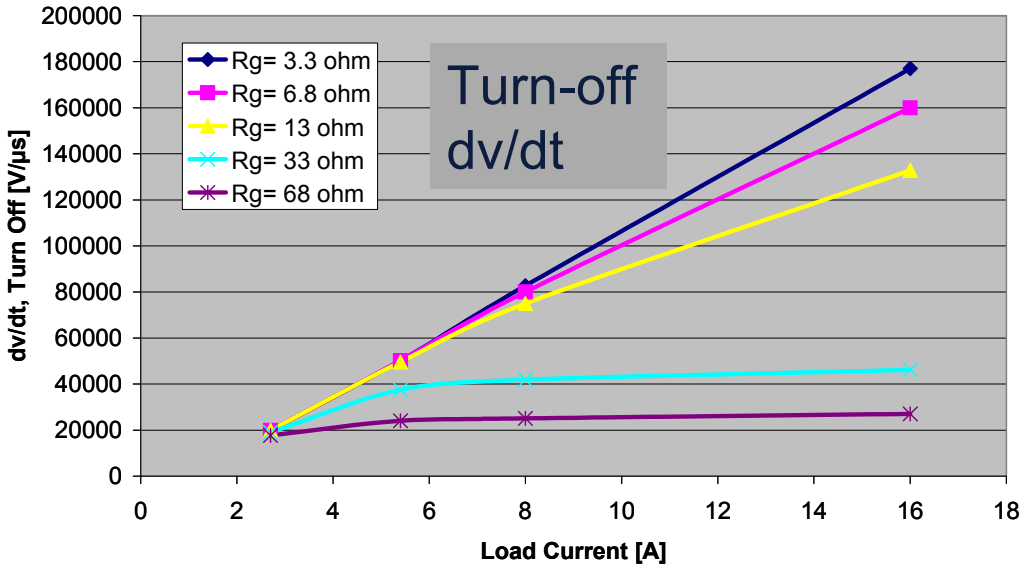

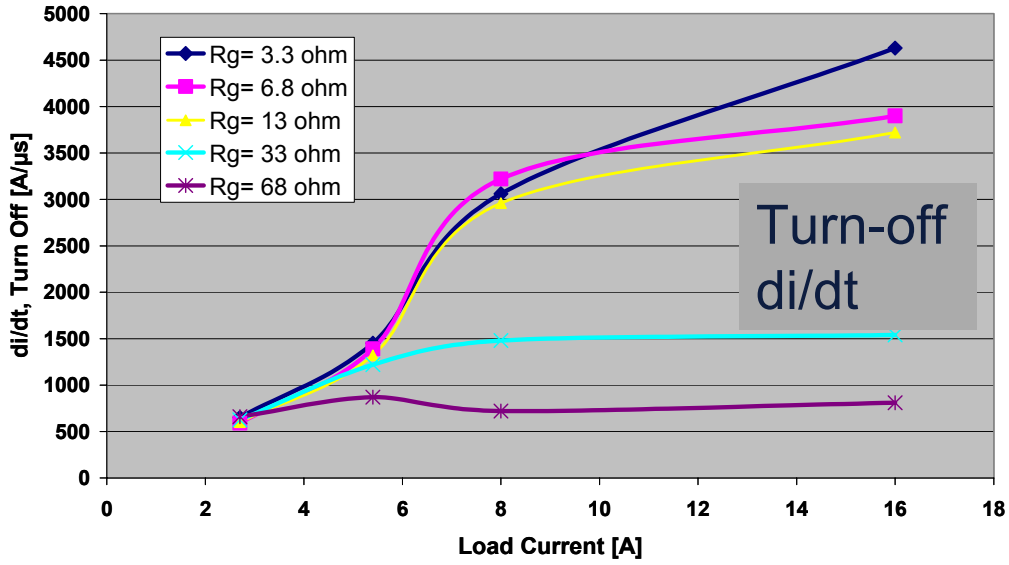

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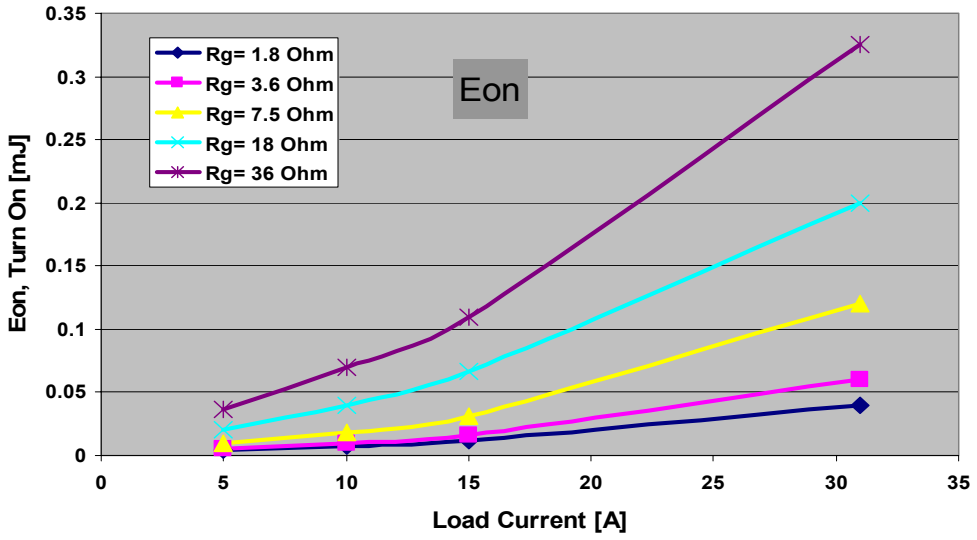

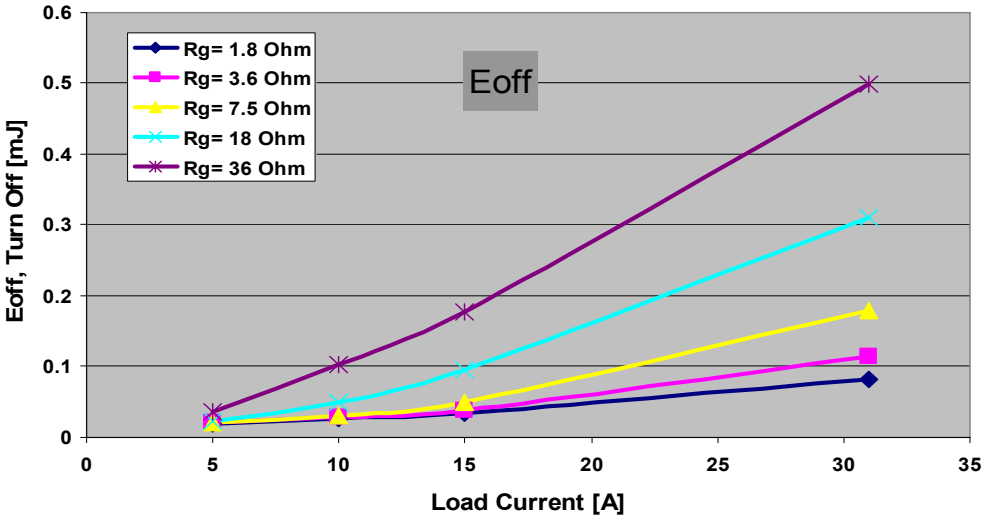

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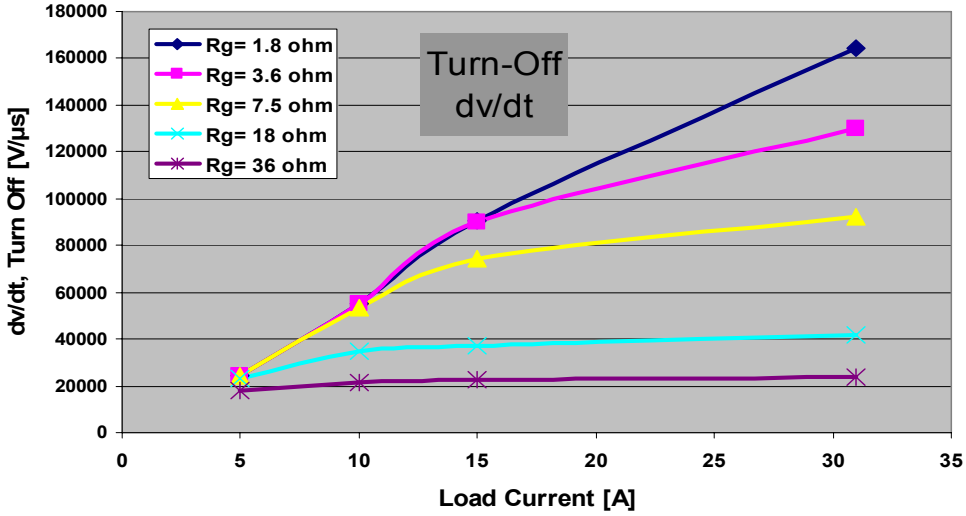

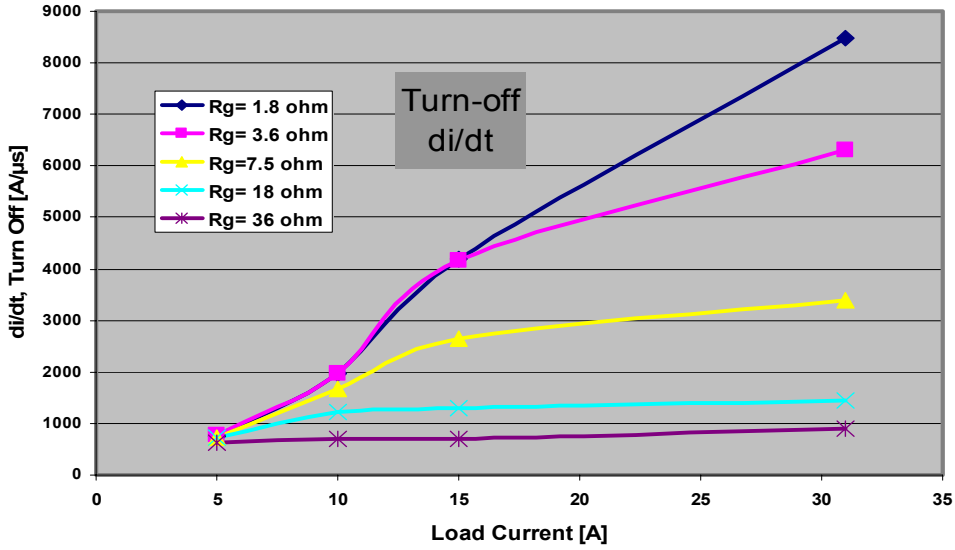

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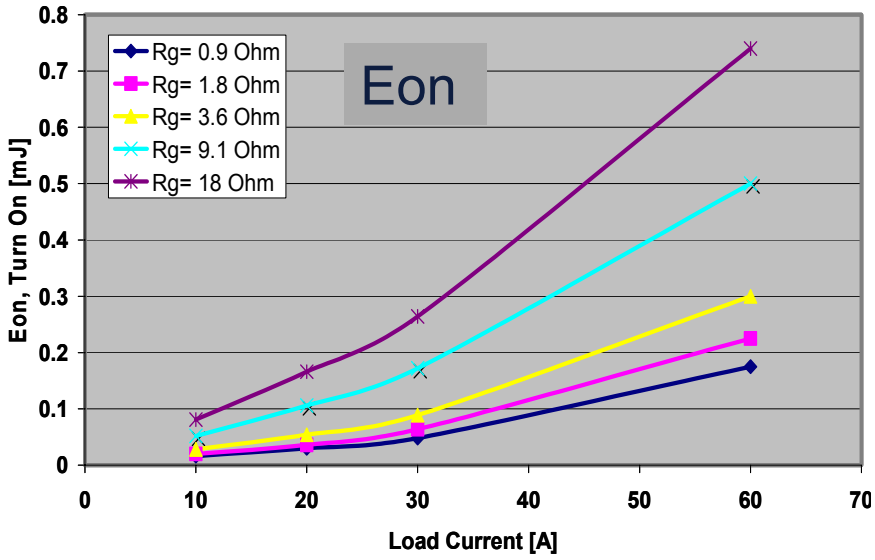

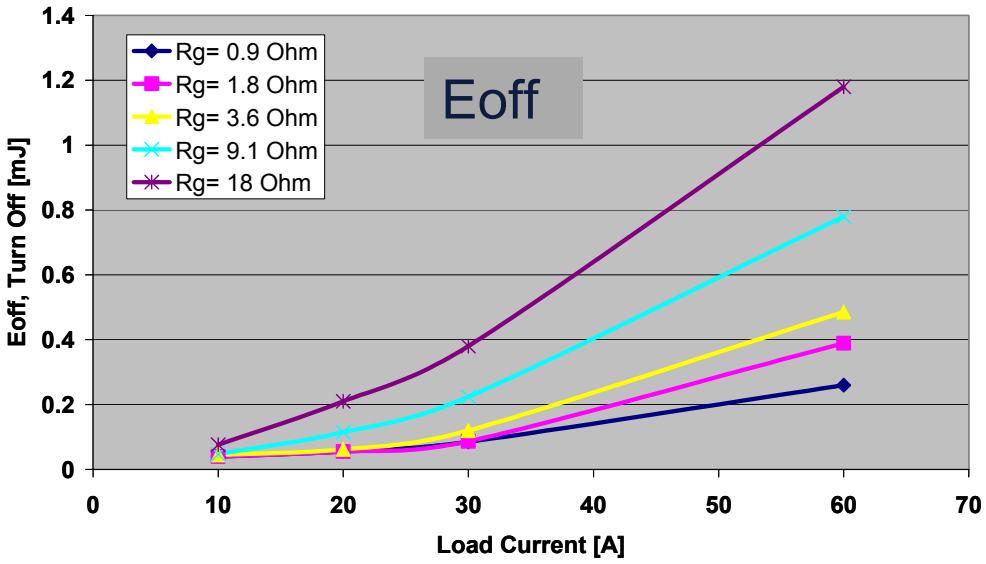

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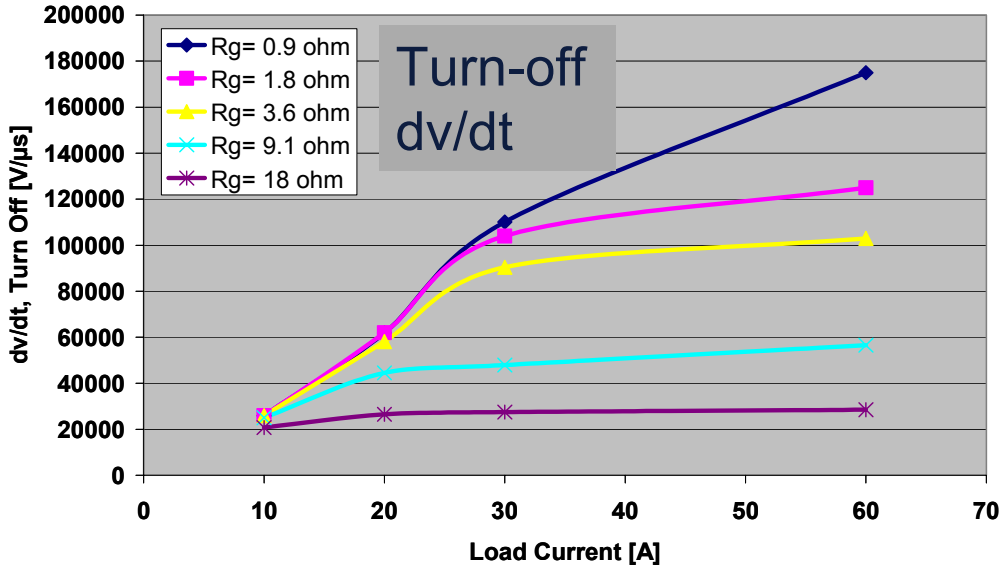

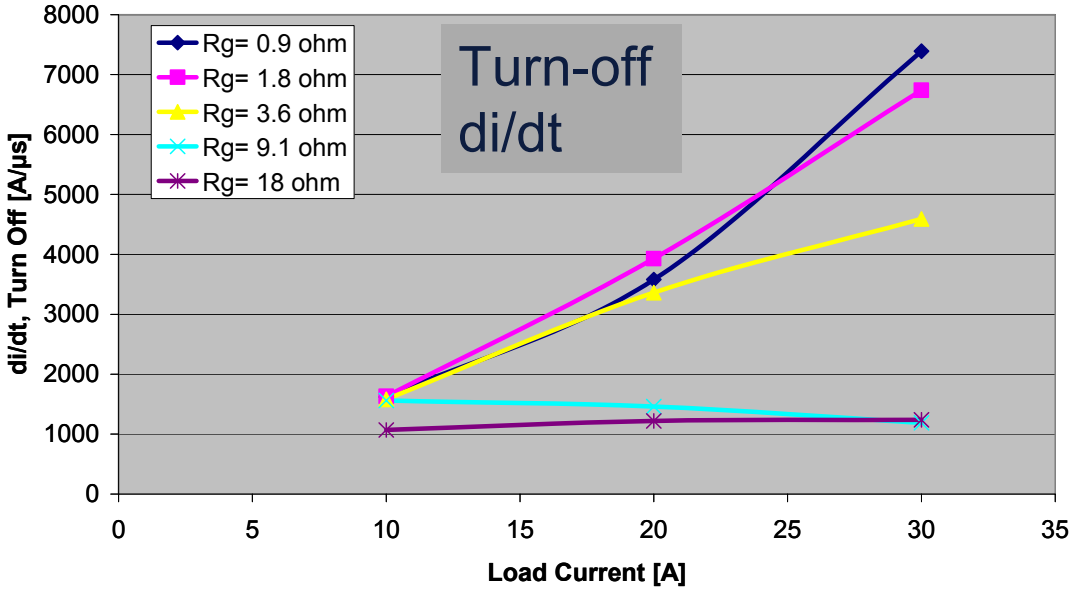

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