AP24001

OCDS Level 1 JTAG Connector
16-Bit & 32-Bit Microcontrollers
OCDS Level 1 JTAG Connector

Revision History: 2003-07 V2.2.1

Previous Version: V2.2.0

Page Subjects (major changes since last revision)

- Changes and corrections to the technical content and document layout and design.
- Adapted to reflect current signal naming conventions.
- Table footnotes added.
- V2.1 was an intermediate version.
- pg3/5 Added Connector manufacturer example (section 2.2) and confirmed which signals are Pull-up (section 3.1)

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ipdoc@infineon.com
1 Introduction

This document describes the Infineon Technologies JTAG Connector for the C166CBC, C166S V1, C166S V2 and TriCore cores. Since there is no standard connector defined in the JTAG standard (IEEE1149.1) specification, nor an established industry standard, we are defining, for debug purposes, our own standard.

2 The Connector Layout

2.1 Slow and Fast Signals, Shielding

Since the connector will be used together with a flat ribbon cable, the pins on the left and right side of the connector will alter within the flat ribbon cable. Slow signals and GND are on the right side and fast signals are on the left side. This gives some shielding. The key pin should be forced down by the debugger side to GND.

2.2 Mechanical

The connector (Pin Header) is a standard 2.54 mm (0.1 inch) centres and 10mm pins. An example manufacturer is Molex (www.molex.com) C-Grid III, 8w Dual Row (Molex part number 90131-0764. These can also be ordered from RS).

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Figure 1 Connector Layout
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![Connector Layout Diagram]

Application Note

V2.2.1, 2003-07
2.3 Signal Description

The following are the Infineon JTAG connector signals.

Note that directions are indicated as follows:

- O = output from the CPU processor board to the debugger.
- I = input to the CPU processor board from the debugger.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Pin</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDO</td>
<td>O</td>
<td>3</td>
<td>IEEE 1149.1</td>
</tr>
<tr>
<td>TDI</td>
<td>I</td>
<td>7</td>
<td>IEEE 1149.1</td>
</tr>
<tr>
<td>TMS</td>
<td>I</td>
<td>1</td>
<td>IEEE 1149.1</td>
</tr>
<tr>
<td>TCK</td>
<td>I</td>
<td>11</td>
<td>IEEE 1149.1</td>
</tr>
<tr>
<td>TRST</td>
<td>I</td>
<td>9</td>
<td>IEEE 1149.1</td>
</tr>
<tr>
<td>BRKIN</td>
<td>I</td>
<td>13</td>
<td>Break Input &amp; OCDS configuration</td>
</tr>
<tr>
<td>BRKOUT</td>
<td>O</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>RESET</td>
<td>I</td>
<td>8</td>
<td>Open drain, TriCore: PORST (Power On Reset)</td>
</tr>
<tr>
<td>CPU_CLOCK</td>
<td>O</td>
<td>5</td>
<td>Optional</td>
</tr>
<tr>
<td>RCAP1</td>
<td>15</td>
<td>Reserved for customer application purposes</td>
<td></td>
</tr>
<tr>
<td>OCDSE&lt;sup&gt;1&lt;/sup&gt;</td>
<td>I</td>
<td>14</td>
<td>TriCore, OCDS configuration</td>
</tr>
<tr>
<td>GND</td>
<td>4,6,12</td>
<td>I/O ring voltage of CPU</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>2</td>
<td>I/O ring voltage of CPU</td>
<td></td>
</tr>
<tr>
<td>RCAP2</td>
<td>16</td>
<td>Reserved for customer application purposes</td>
<td></td>
</tr>
</tbody>
</table>

<sup>1</sup> This signal is not available on each Microcontroller implementation. This signal must be forced to a low level from the Trace Hardware (Emulator). If the Microcontroller derivative has no corresponding signal, it should be left unconnected in the target hardware.

2.4 Voltage

All signals have the voltage of the I/O ring. Current Microcontroller implementations have 5 V, 3.3 V or 2.5 V V<sub>DD</sub> on I/O ring.

The V<sub>DD</sub> I/O ring should be provided from the target based board to the active buffers at the cable level (if present).
3 Implementation Considerations

3.1 Pull-Ups
On the CPU board the following signals should each be connected to pull-ups of 10 kΩ respectively.
- OCDS
- TMS
- TCK
- TDI
- TRST
- RESET
- BRKIN

3.2 Clock Pin
The clock is optional since not every CPU has a Clock-out pin available. Since the clock pin could be a very good antenna it should be connected via any sort of Jumper. If not implemented it should be GND so that it can be sensed if there is clock or not.

3.3 RCAP1 and RCAP2 Pins
These pins are reserved for customer application purposes.

3.4 OCDS and BRKIN Pins
These pins are used during power on reset (POR reset pin) to setup the OCDS system (TriCore only)
4 Low Cost EVA Board Connector

The Infineon StarterKit boards are equipped with a low cost DB25 printer port connector. The JTAG Signals are mapped to the following Printer-Port signals. It is not recommended to use a DB25 connector in customer applications since the onboard-wiggler would eat up additional board space & power.

<table>
<thead>
<tr>
<th>LPT Pin</th>
<th>LPT Signal</th>
<th>Type</th>
<th>JTAG/Board Signals</th>
<th>16-pin JTAG Connector</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Strobe</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Auto feed</td>
<td>O</td>
<td>VPP User</td>
<td></td>
<td>Optional: 12 V for external User. FLASH programming</td>
</tr>
<tr>
<td>2</td>
<td>D0</td>
<td>O</td>
<td>TDI</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Error</td>
<td>I</td>
<td>10 kΩ pull-up to 5 Volt</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D1</td>
<td>O</td>
<td>TMS</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Init</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D2</td>
<td>O</td>
<td>TCK</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Select</td>
<td>O</td>
<td>VPP Mon</td>
<td></td>
<td>Optional: 12 V for external Mon. FLASH programming.</td>
</tr>
<tr>
<td>5</td>
<td>D3</td>
<td>O</td>
<td>TRST</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>D4</td>
<td>O</td>
<td>BRKIN</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>D5</td>
<td>O</td>
<td>RESET</td>
<td>8</td>
<td>TriCore: PORST (Power On Reset)</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>D6</td>
<td>O</td>
<td>OCDSE(^T)</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>D7</td>
<td>O</td>
<td>NMI</td>
<td>9</td>
<td>Optional</td>
</tr>
<tr>
<td>22</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Ack</td>
<td>I</td>
<td>BRKOUT</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
</tbody>
</table>
### Table 2 Connector Signals

<table>
<thead>
<tr>
<th>LPT Pin</th>
<th>LPT Signal</th>
<th>Type</th>
<th>JTAG/Board Signals</th>
<th>16-pin JTAG Connector</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Busy</td>
<td>I</td>
<td>10 kΩ pull-down to GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Paper empty</td>
<td>I</td>
<td>TDO</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>GND</td>
<td>SH</td>
<td>GND</td>
<td>4,6,12</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Select</td>
<td>O</td>
<td>IRQ pending</td>
<td>Optional</td>
<td></td>
</tr>
</tbody>
</table>

1) This signal is not available on each Microcontroller implementation. This signal must be forced to a low level from the Trace Hardware (Emulator). If the Microcontroller derivative has no corresponding signal, it should be left unconnected in the target hardware.
5 Onboard Wiggler

The Infineon Technologies StarterKit boards are equipped with Onboard Wigglers. The Onboard Wiggler protects the microcontroller from voltage peaks and operates as a level shifter if needed.

Please note that the above Wiggler describes a stand-alone version. On the StarterKit board the right side of the Wiggler would be connected with the chip.

![Wiggler Circuit Diagram](image)

Figure 2 Wiggler Circuit Diagram
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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results. Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher