

SmartLEWIS™ RX+

TDA5225

Enhanced Sensitivity Multi-Configuration Receiver

Handling of Sensitivity

Application Note

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Wireless Control

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TDA5225 Enhanced Sensitivity Multi-Configuration Receiver

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Page	Subjects (major changes since last revision)

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1 Overview and General Information

This document gives a simple overview on how to use the TDA5225 for best achievable sensitivity results.

For the TDA5225, the output signals DATA or DATA_MATCHFIL can be used (transparent mode).

BER sensitivity measurements, as noted in the data sheet, use the transparent receive mode TMMF (DATA_MATCHFIL output signal), where the received data is sampled with ideal data clock.

The DATA_MATCHFIL output signal will provide higher systematic jitter than the DATA output signal.

Please keep in mind, that the achievable sensitivity in both transparent modes is significantly depending on the implemented clock and data recovery algorithm of the user software in the application controller.

For the sensitivity values given in the data sheet, also the filter settings in the signal chain (on-chip BPF and FSK PDF filter) are noted. In case these filter setting need to be adapted for the application, the achievable sensitivity will change accordingly.

2 TDA5225 Output Signals

There are two output sources of the matched filter shown in [Figure 1](#):

- DATA: DC cancellation (Raw DATA Slicer) is applied to the 1-chip MF output
- DATA_MATCHFIL: The signum is taken from the 2-chip MF output, no DC cancellation necessary

DATA_MATCHFIL has about 3 dB better performance than DATA output, but DATA_MATCHFIL output signal will provide higher systematic jitter than the DATA output signal (see different slopes of MF signal in [Figure 2](#)).

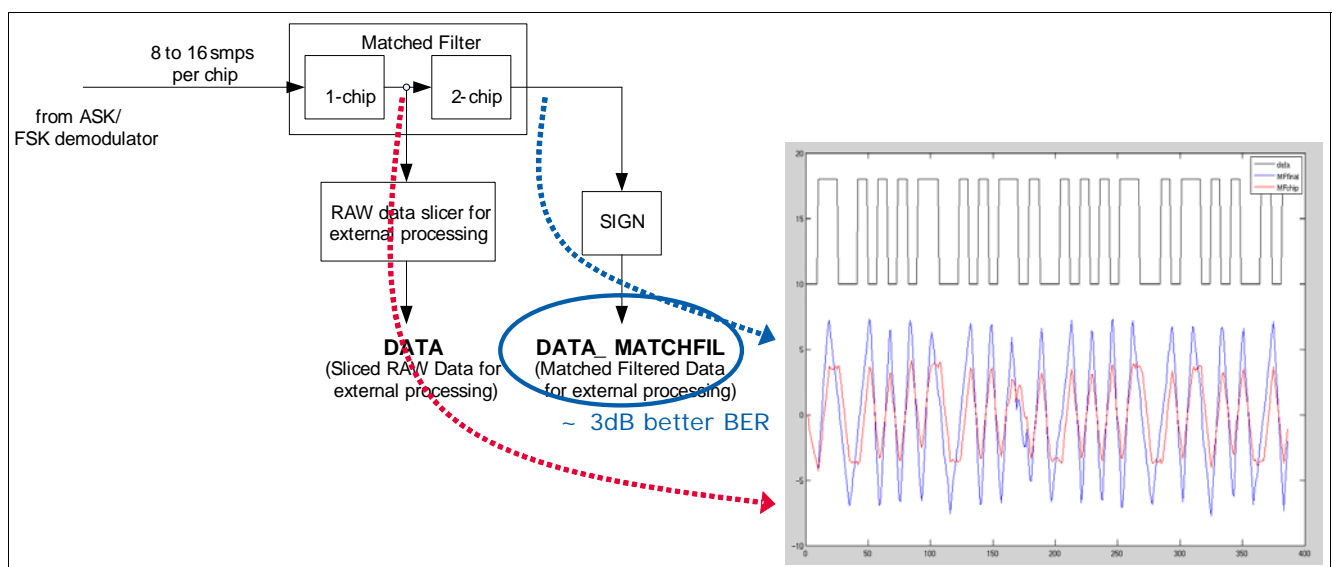


Figure 1 Matched Filter Output Sources

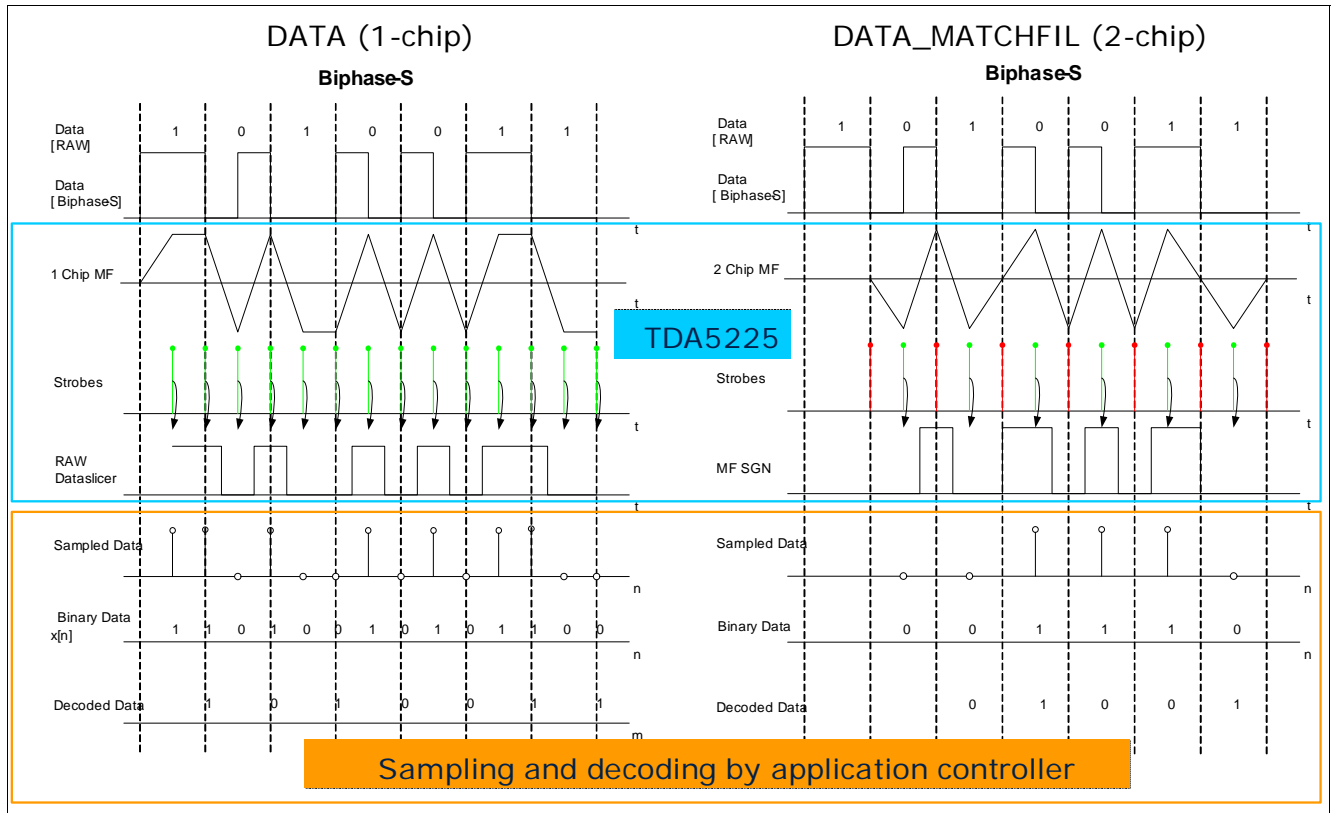


Figure 2 Matched Filter Output Signals

2.1 Output Signal DATA

A DC offset of the 1-chip MF signal must be compensated to be able to slice the data correctly.

This DC cancellation is based on a BW-adjustable digital lowpass filter. The bandwidth of the DC removal filter used for the Raw Data slicer (external slicer, register x_EXTSLC) can be increased to achieve a faster settling time. Faster settling time comes at the cost of higher ripple which causes more jitter at the output.

NOTE: The ripple introduced by fast DC cancellation will also cause a decrease of performance.

The settling time does not only depend on the selected DC removal filter bandwidth but also on the frequency offset.

- In FSK a frequency offset introduces a DC offset at the output of the Matched Filter
- In ASK there is also a DC offset introduced due to the antilog function needed for linearization of the input signal

The preamble of the transmitted signal must be long enough for the filter to settle.

2.2 Output Signal DATA_MATCHFIL

On usage of the 2-chip Matched Filter output, the DC cancellation is achieved within one symbol.

There is no ripple because of the DC cancellation, therefore the sensitivity is increased, but DATA_MATCHFIL output signal will provide higher systematic jitter, due to different slopes of MF signal shown in [Figure 2](#).

The „systematic jitter“ is data-dependent and can therefore be compensated by the application controller.

3 Final Conclusion - Data Jitter

Three types of jitter are superimposed at the output and contribute differently at different input power levels:

- Systematic Jitter can be reduced by oversampling (TDA5225 Explorer software tool is generating the optimal chip-internal oversampling). This jitter can also be observed at good RF input power levels.
- Smaller DC canceller bandwidth (RAW Data Slicer) can be used to reduce ripple and therefore reduce the jitter slightly, but this increases the slicer settling time. For the final application a trade-off between settling time and ripple must be made.
- Jitter due to Noise can not be reduced (except for a BPF BW reduction) and limits therefore the achievable performance.

IMPORTANT NOTE: When the software clock-data recovery in the application controller requires an additional criterion of a certain allowed jitter at the output signal of the radio, the noted high sensitivity can NOT (not even under best case conditions) be achieved at the Raw Data Slicer output (DATA).

Usage of the 2-chip matched filter output (DATA_MATCHFIL) and compensation for systematic pulse width “modulation” needs to be done in the external “high performance” software clock recovery, which may require a strong application controller.

Note: The TDA5235/40 can deliver high sensitivity due to internal available multi-bit signals (TDA5225 only delivers a 1-bit output signal) and a real hardware clock-recovery unit.

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