BGA728L7

Broadband Low Noise Amplifier for FM Radio Applications using BGA728L7

Including a configuration for minimum NF and one for best input matching in a 50 Ohm system

Application Note AN231

Revision: Rev. 1.0
2010-08-02

RF and Protection Devices

Edition 2010-08-02

Published by
Infineon Technologies AG
81726 Munich, Germany

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Application Note AN231	
Revision History: 2010-08-02	
Previous Revision: prev. Rev. x.x	
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1 Introduction

FM Radio has a long history to its credit starting from its development in 1933. Today, FM radio is an integral part of almost all mobile phones, including the ultra low cost phones. FM Radio broadcast today is not just used to listento songs and news, but also used for RDS (Radio Data System) to receive various services including TMC (Traffic Message Channel) which gives traffic information for navigation purposes. In addition, some handsets are being equipped with FM Radio transimission capability to send voice signals to car audio systems or Hi-Fi systems.

Therefore, FM system design in a phone is getting more and more complex. Till recently, the headset served as the antenna for FM Radio reception, wherein the antenna size is a bit relaxed and the antenna performance is satisfactory. A new trend has emerged to be able to use FM radio also without the headset, wherein the antenna embedded into the phone. But in this case, the space constraint poses a challenge on the antenna design. Shrinking the size of the antenna reduces antenna gain and bandwidth, which introduces a high loss into the system which deteriorates the receiver performance, namely the receiver sensitivity. This application note presents Infineon solution to the aforementioned challenges leading to the design of a high performance RF front end with the lowest power consumption.

A general topology for the RF front-end of FM Radio is as shown in Figure 1. Variations of the given application schematic are possible based on the complete system design and concept. These may include systems with only external headset antenna, only internal embedded antenna or both antennas co-existing. Infineon offers the complete chain of RF front-end parts between the antenna and the receiver IC for FM Radio, which include ESD protection devices, RF switches and LNAs. The focus of this application note is Low Noise Amplifier for FMR.

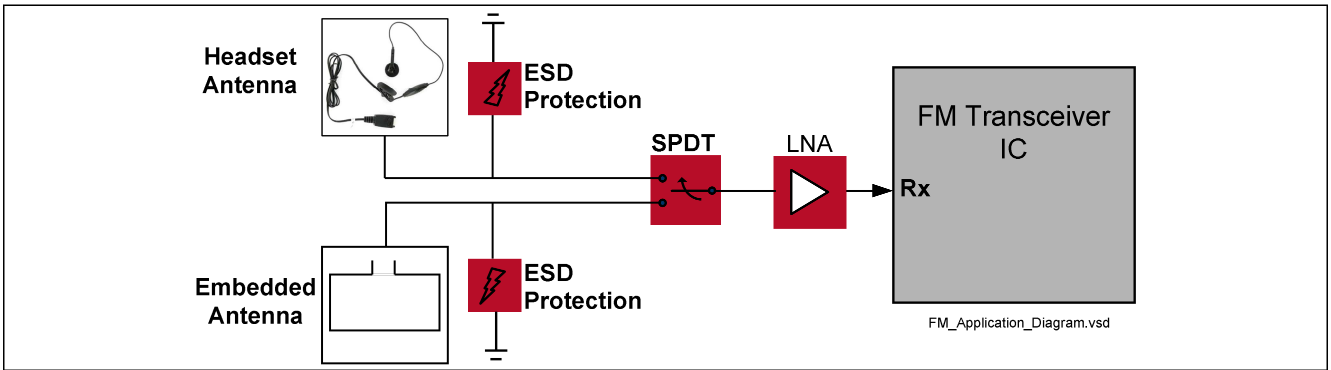


Figure 1 FM Radio RF front-end block diagram

An ESD protection circuit is needed at the antenna to protect the front-end system from ESD strikes, as the antenna is susceptible to ESD events. For more information please see Appendix 1.

A Single Pole Double Throw or SPDT RF switch is used to toggle between the headset and embedded antenna. The switch being in front of the LNA and in the vicinity of strong cellular signals should introduce minimal loss to the system and offer high linearity. To know more about Infineon solutions for RF Switches, please refer to application note AN175.

A Low Noise Amplifier or LNA follows the switch, which significantly reduces the noise figure of the whole receiver chain, thereby improving the receiver sensitivity. However, there are a few challenges in the design of the LNA for this purpose. Using it in a hand held device demands low current consumption and high linearity due to the coexistence of cellular bands. In a system with internal antenna, due to the very small size, the antenna impedance is very high and thus the LNA has to be matched to this high impedance and in addition offer a low noise figure.

2 Overview

This application note shows the performance of Infineon's BGA728L7 as an LNA for FM radio.

BGA728L7 is a broadband MMIC originally targeted at mobile TV applications but may also being used for FM radio applications. It offers high integration including biasing, on/off switch and a low gain mode.

The application note is divided in two parts. The first part shows the MMIC in a configuration that is optimized for low noise figure, in the other part the LNA is optimized for a good matching to 50 Ohms.

Comparison of the two circuits.Table 1 gives a quick overview of the performance difference of the two circuits. Test conditions are the same for both configurations

Table 1 Comparison of the two circuits.

	Optimized for	
Parameter	**Noise Figure**	**Input matching**
Noise figure / dB	1.3	1.65
Gain / dB	14.3	16.4
Input return loss / dB	7.3	12.2
Output return loss / dB	9.7	9.6
Input 1dB compression point / dBm	-9	-6.5

3 Circuit optimized for Noise Figure

3.1 Summary of Measurement Results

Table 2 Performance with min. NF at Vcc=Von=2.8 V, Vgs=0V

Parameter	Symbol	Value	Unit	Note/Test Condition
Frequency Range	Freq	78-108	MHz	
DC Voltage	Vcc	2.8	V	
DC Current	Icc	5.7	mA	
Gain	G	14.3	dB	Pin=-30dBm
Noise Figure	NF	1.3	dB	SMA and PCB loss of 0.1 dB included
Input Return Loss	RLin	7.3	dB	Pin=-30dBm
Output Return Loss	RLout	9.7	dB	Pin=-30dBm
Reverse Isolation	IRev	28.8	dB	Pin=-30dBm
Input P1dB	IP1dB	-9.3	dBm	Measured @ 100MHz
Output P1dB	OP1dB	4	dBm	
Input IP3	IIP3	-7.2	dBm	In-band, f1=100MHz, f2=101MHz, Pin=-30dBm
Output IP3	OIP3	7.1	dBm	
Stability	k	>1	--	Unconditionally stable from DC to 10GHz

3.2 Schematic Diagram

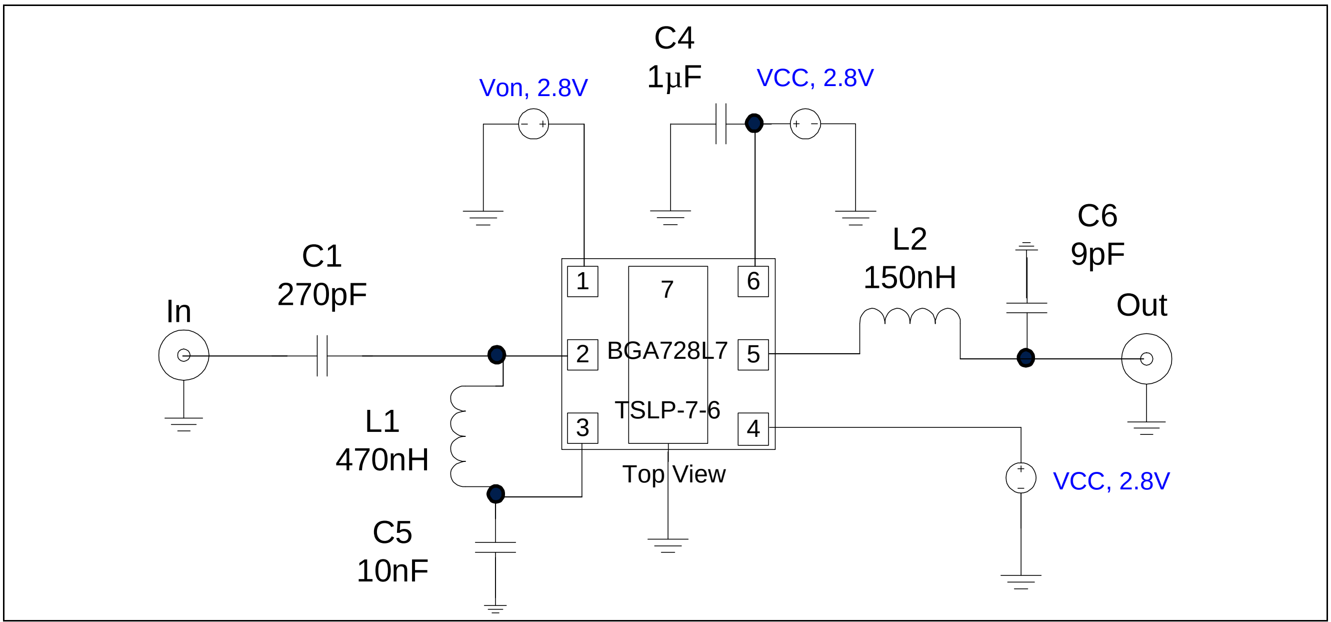


Figure 2 Schematic diagram for minimum NF.

Table 3 Bill-of-Materials for minimum NF

Symbol	Value	Unit	Size	Manufacturer	Comment
C1	270	pF	0402	Various	Input matching
C4	1	uF	0402	Various	HF to ground
C5	10	nF	0402	Various	HF to ground
C6	9	pF	0402	Various	Output matching
L1	470	nH	0603	Tayio Yuden LK	DC Feed/ Input matching
L2	150	nH	0402	Murata LQG15A	Output matching
N1	BGA728L7		TSLP-7-1	Infineon Technologies	SiGe:C LNA MMIC

3.3 Measured Graphs

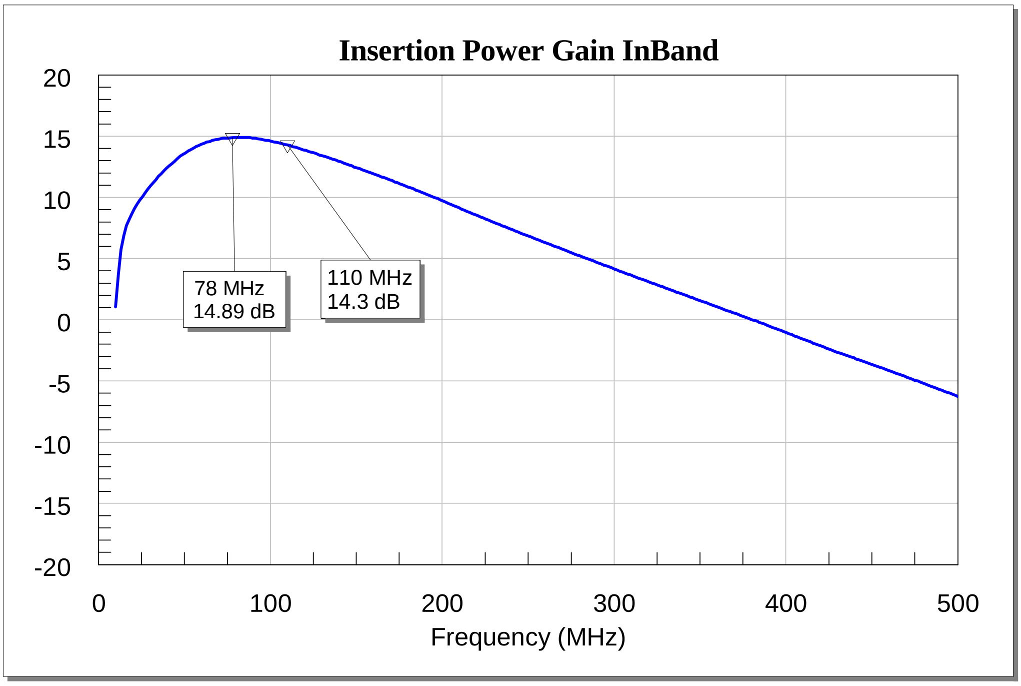


Figure 3 Insertion power gain at minimum NF.

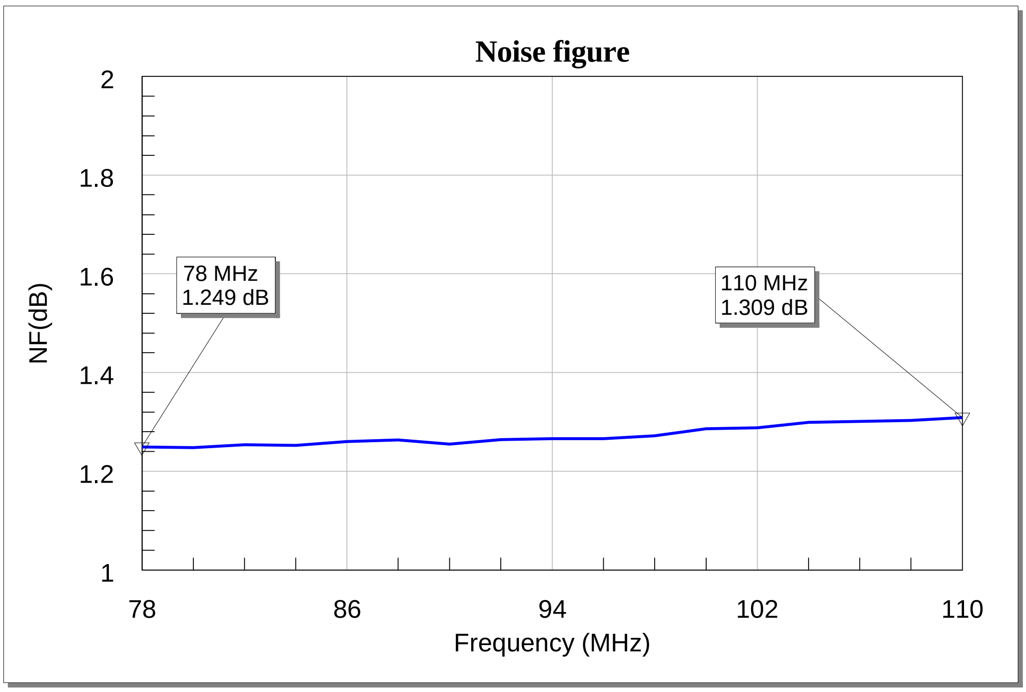


Figure 4 Noise figure at minimum NF.

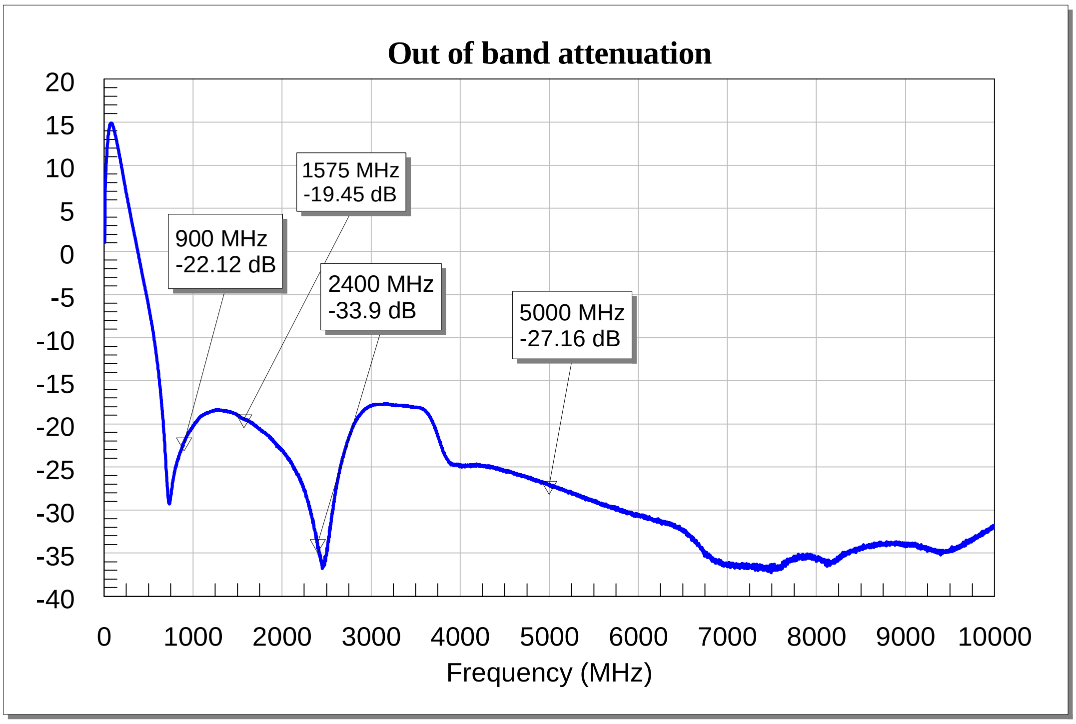


Figure 5 Out-of-band Gain at minimum NF

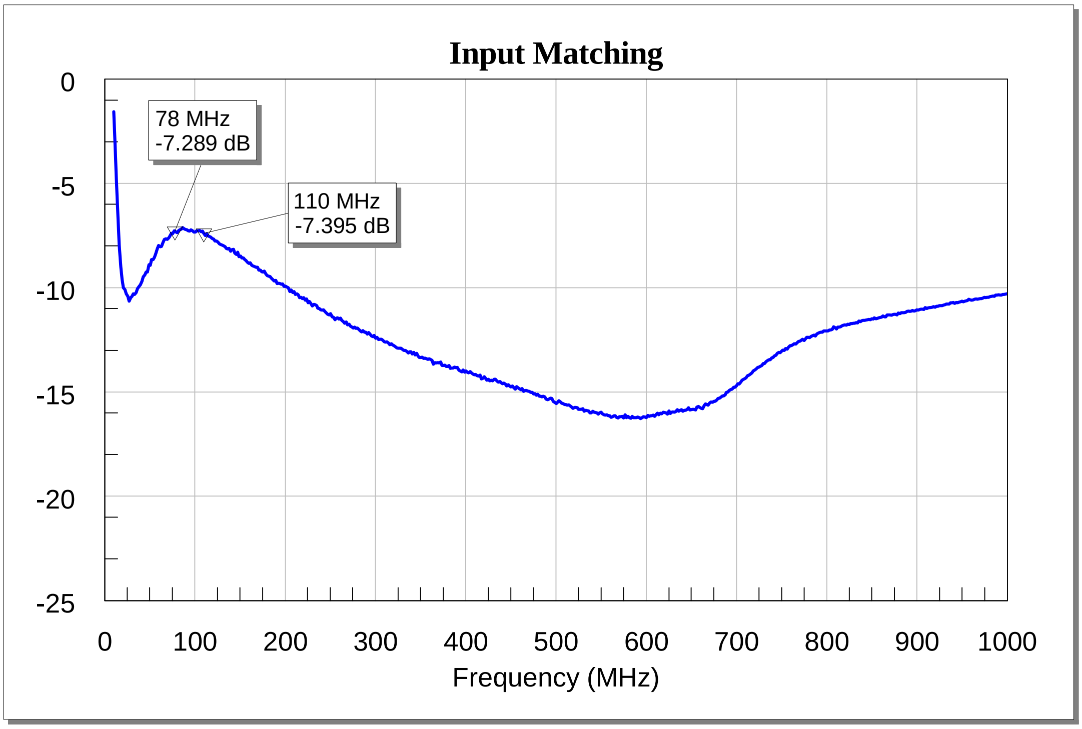


Figure 6 Input matching at minimum NF.

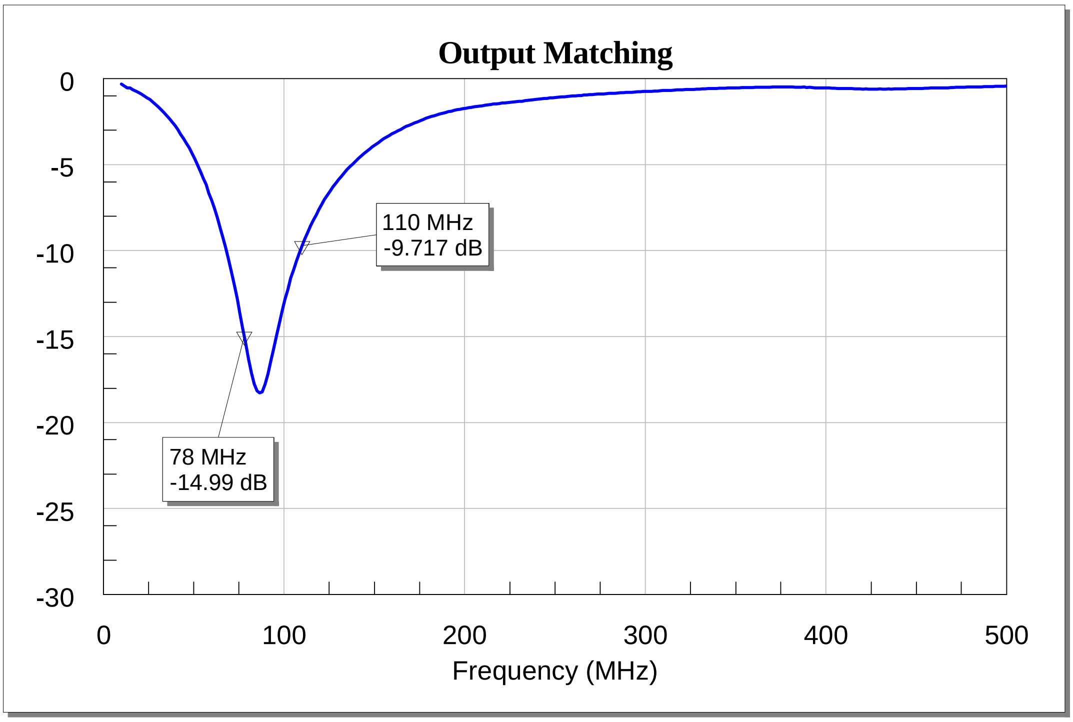
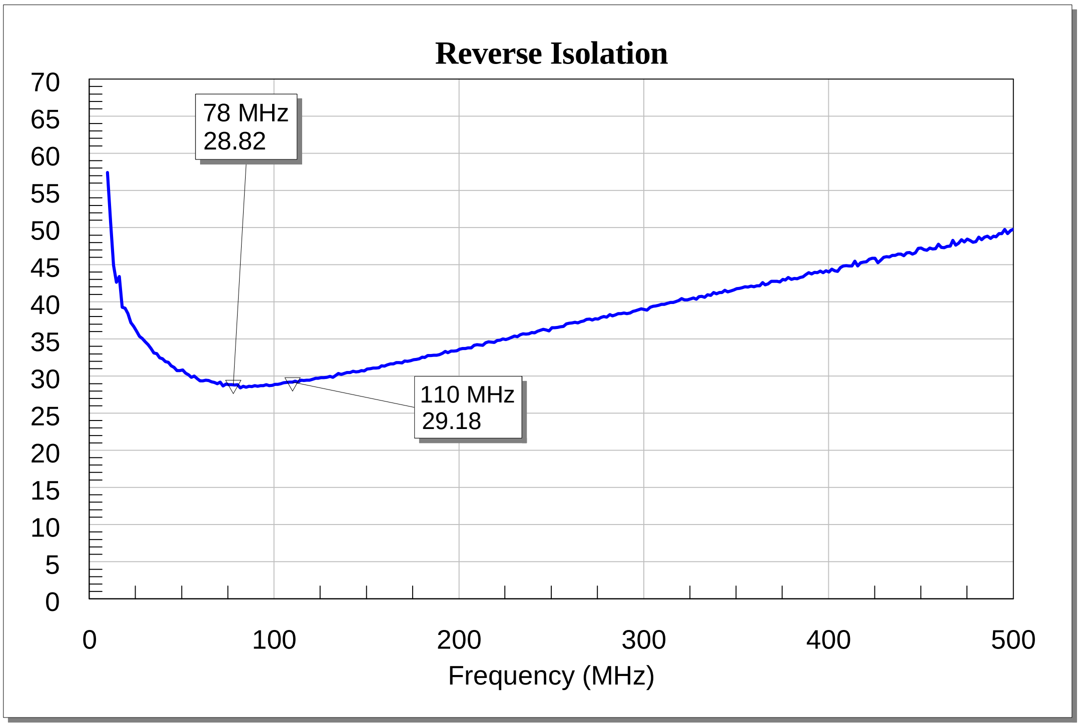


Figure 7 Output matching of at minimum NF.



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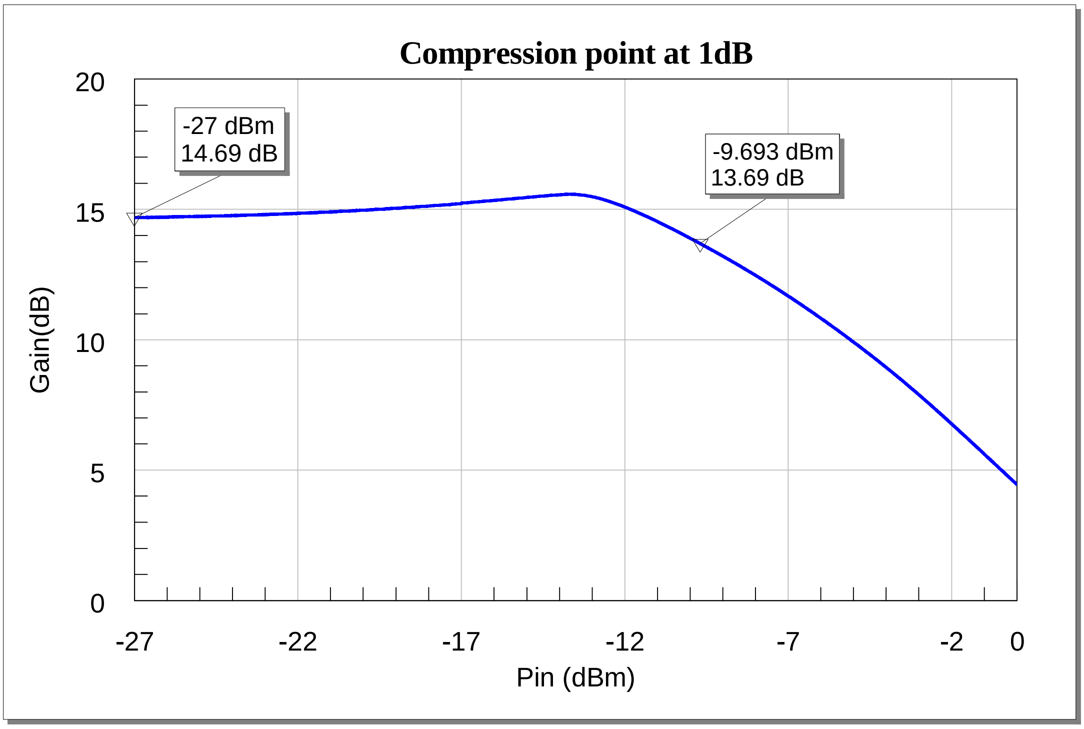

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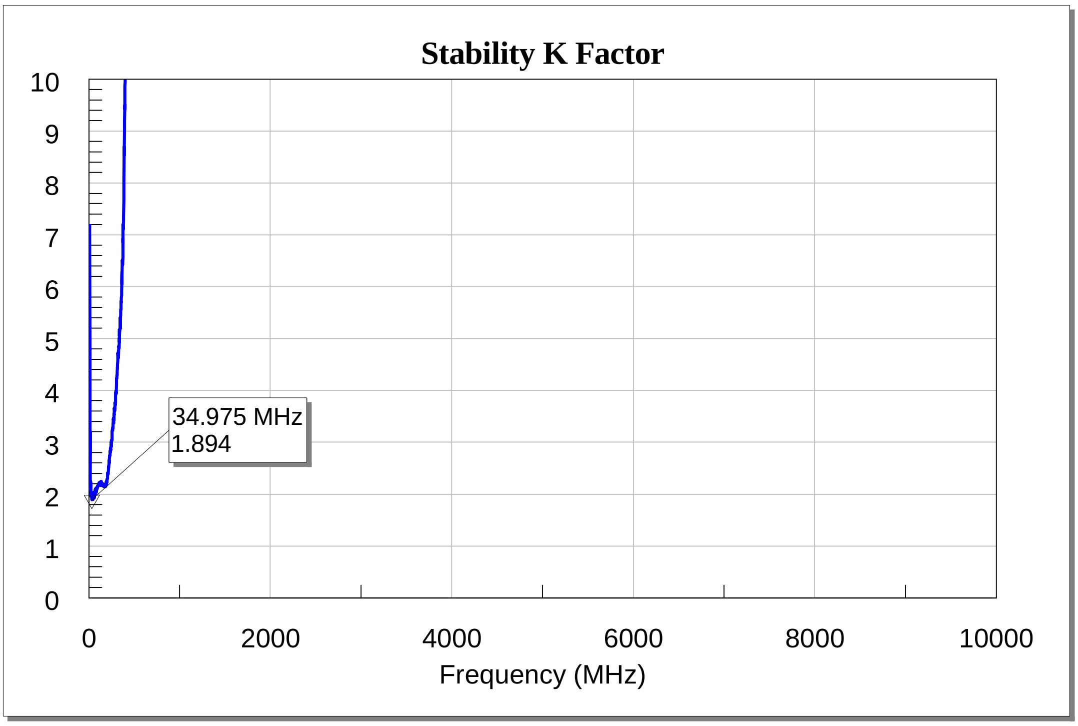
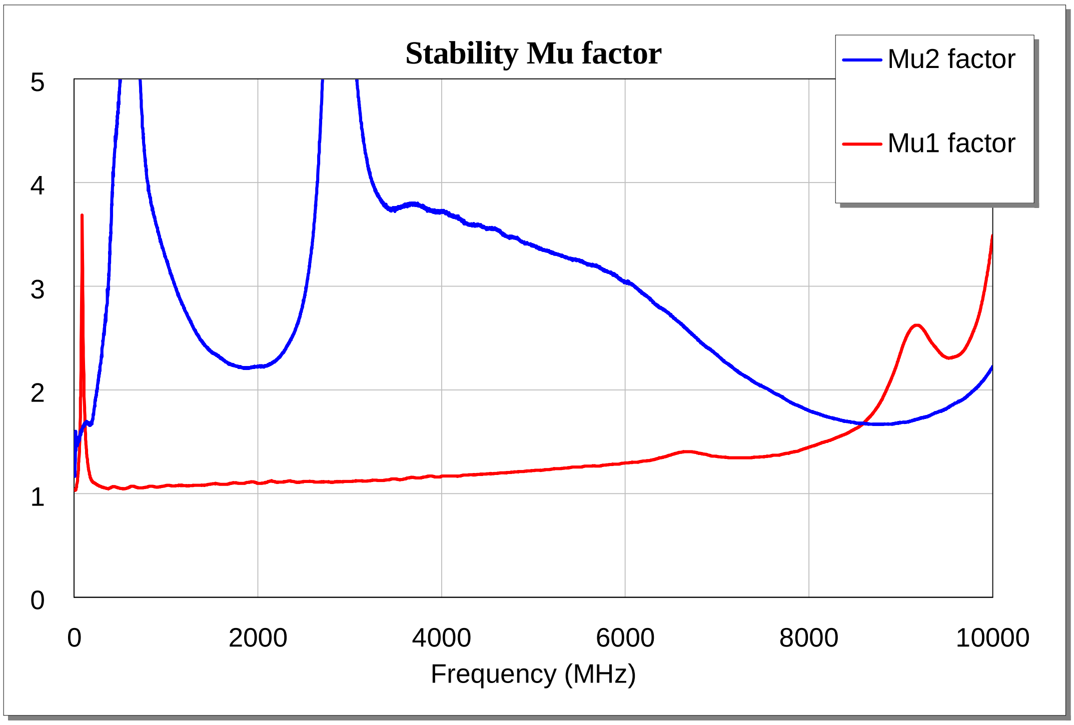


Figure 10 Stability factor K at minimum NF.



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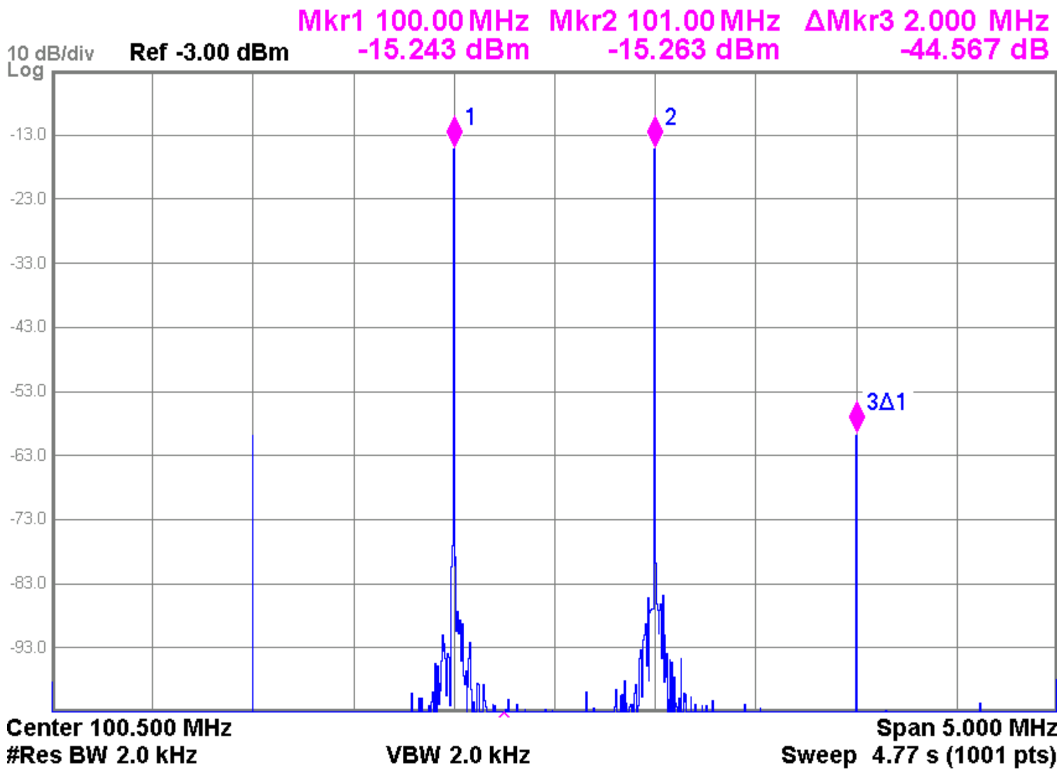

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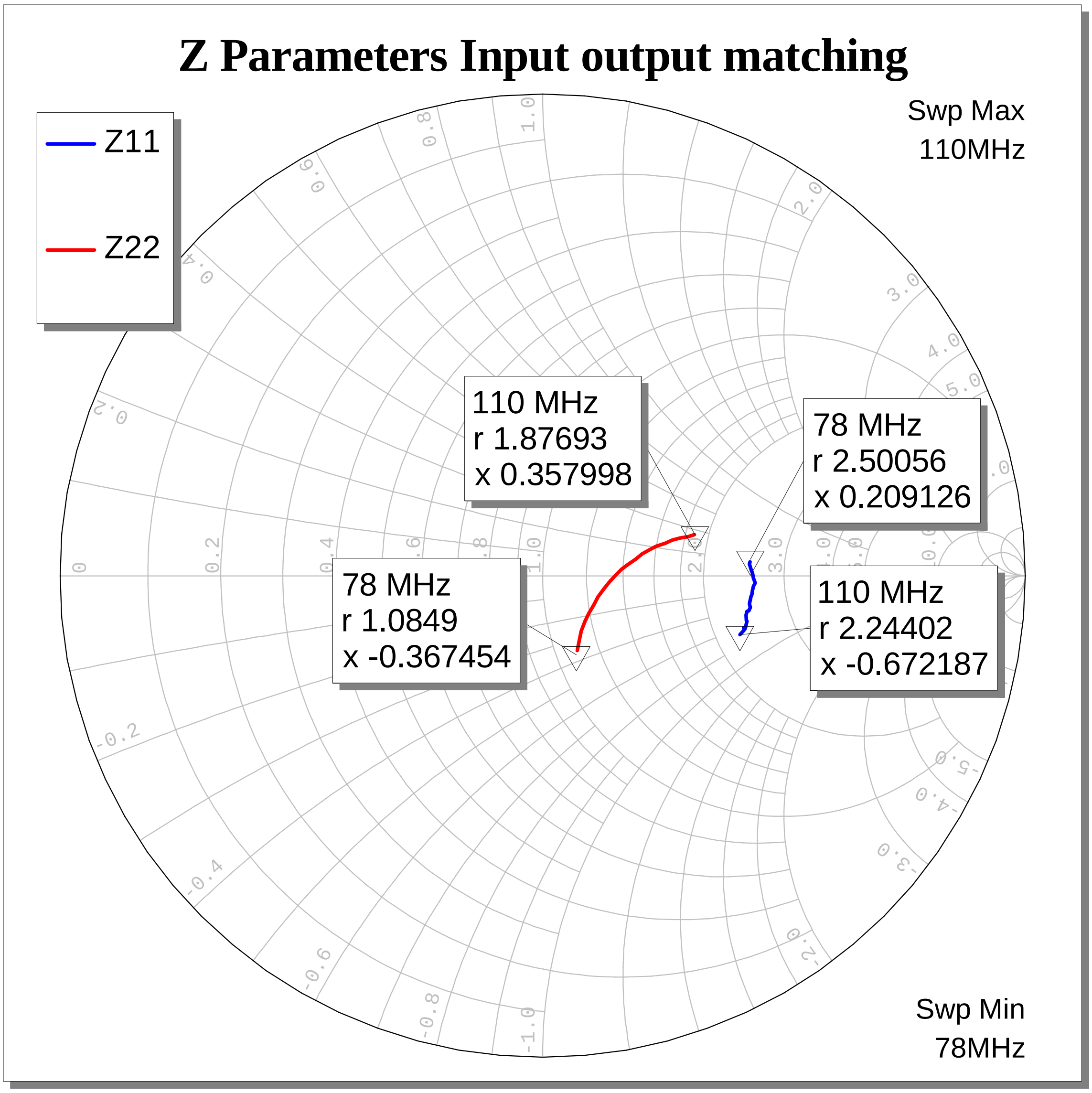


Figure 13 Input and Output impedance at minimum NF.

4 Circuit optimized for input matching

4.1 Summary of Measurement Results

Table 4 Performance with best input matching at Vcc=Von=2.8 V, Vgs=0V

Parameter	Symbol	Value	Unit	Note/Test Condition
Frequency Range	Freq	78…110	MHz	
DC Voltage	Vcc	2.8	V	
DC Current	Icc	5.8	mA	
Gain	G	14.6	dB	Pin=-30dBm
Noise Figure	NF	1.65	dB	SMA and PCB loss of 0.10 dB included
Input Return Loss	RLin	12.2	dB	Pin=-30dBm
Output Return Loss	RLout	9.6	dB	Pin=-30dBm
Reverse Isolation	IRev	28.8	dB	Pin=-30dBm
Input P1dB	IP1dB	-10.4	dBm	Measured @ 100MHz
Output P1dB	OP1dB	3.7	dBm	
Input IP3	IIP3	-6.4	dBm	In-band, f1=100MHz, f2=101MHz, Pin=-30dBm
Output IP3	OIP3	8.2	dBm	
Stability	k	>1	--	Unconditionally stable from DC to 10GHz

4.2 Schematic Diagram

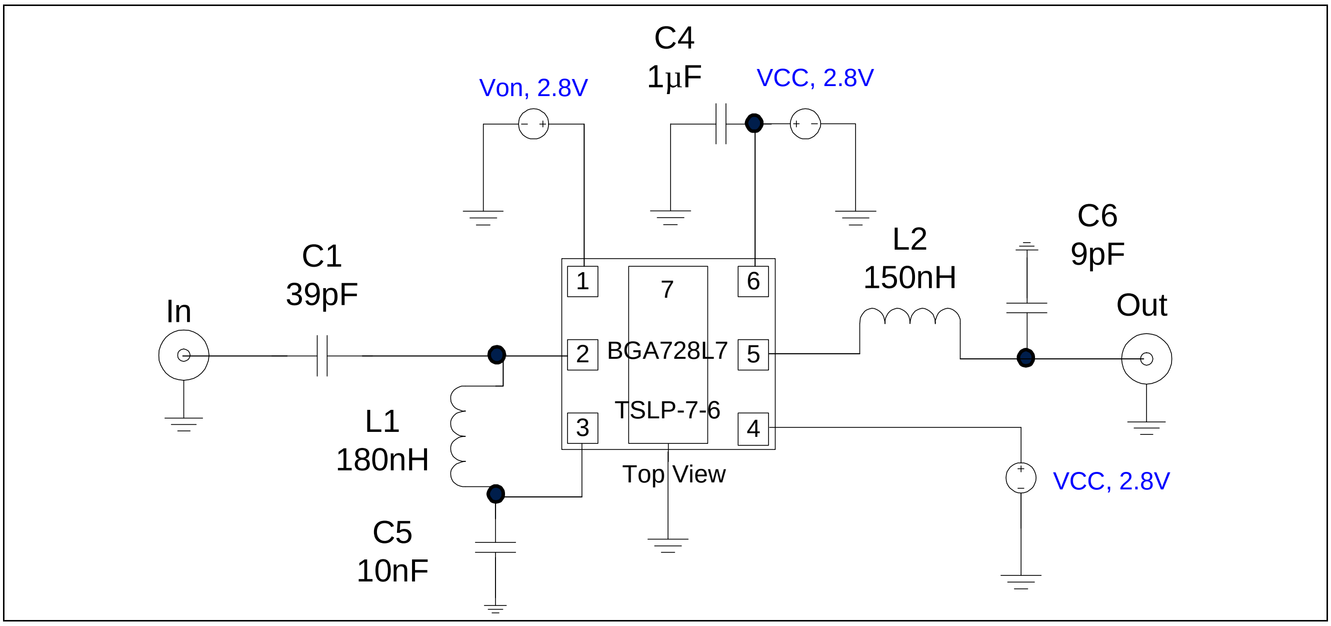


Figure 14 Schematic diagram for best input matching.

Table 5 Bill-of-Materials for best input matching

Symbol	Value	Unit	Size	Manufacturer	Comment
C1	39	pF	0402	Various	Input matching/DC block
C4	1	uF	0402	Various	HF to ground
C5	10	nF	0402	Various	HF to ground
C6	9	pF	0402	Various	Output matching
L1	180	nH	0402	Murata LQG15A	DC Feed/ Input matching
L2	150	nH	0402	Murata LQG15A	Output matching
N1	BGA728L7		TSLP-7-6	Infineon Technologies	SiGe:C MMIC LNA

4.3 Measured Graphs

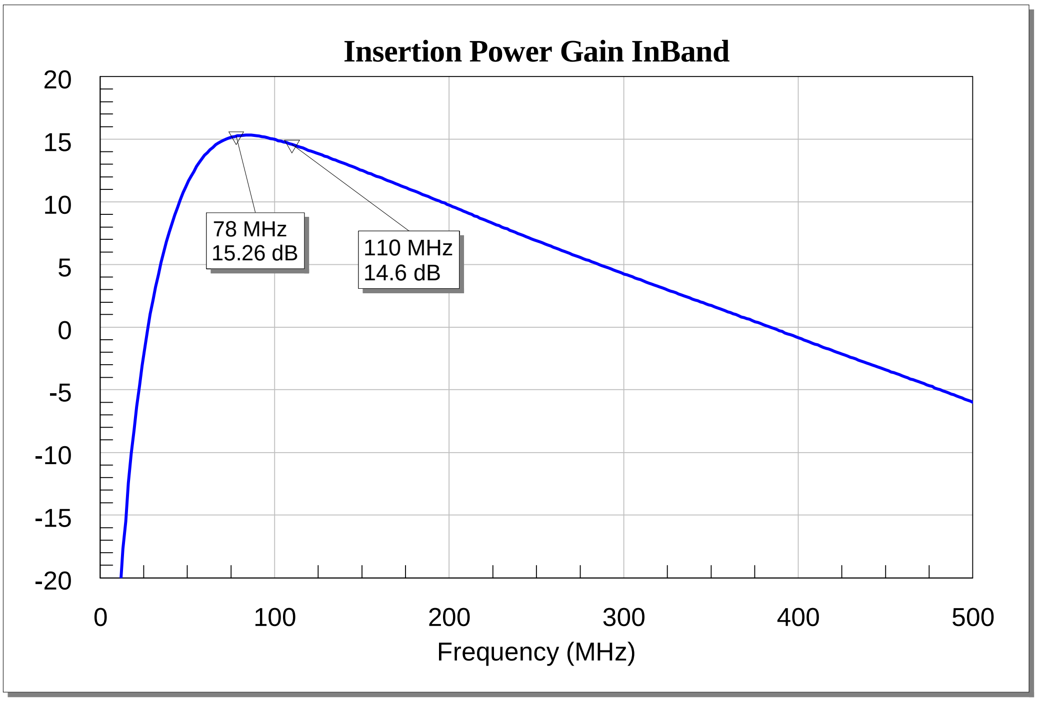
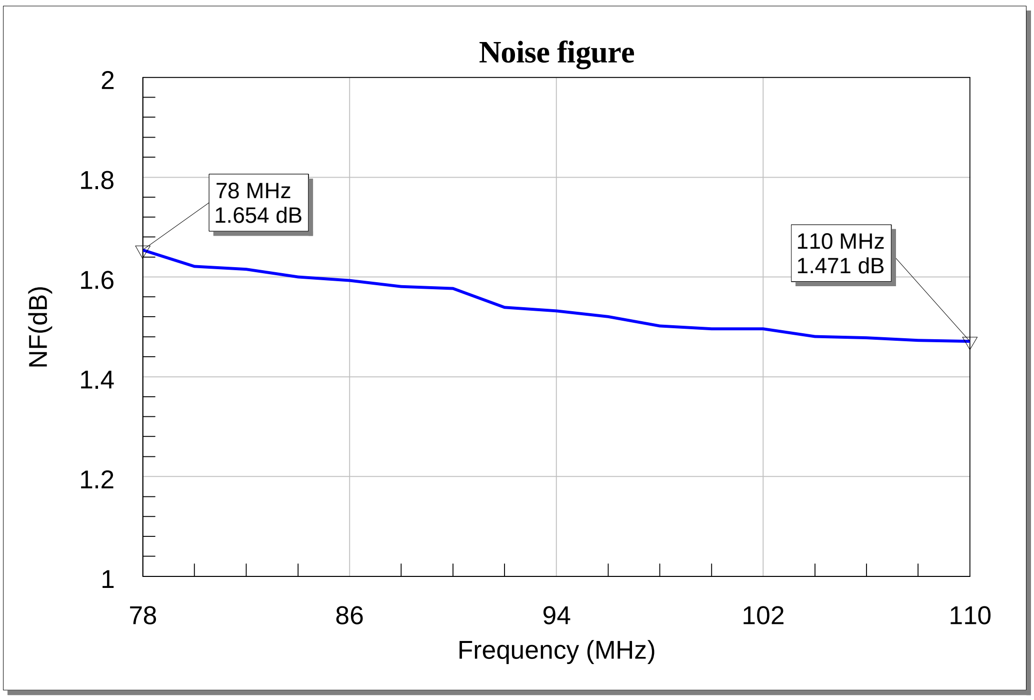


Figure 15 Insertion Power Gain with best input matching



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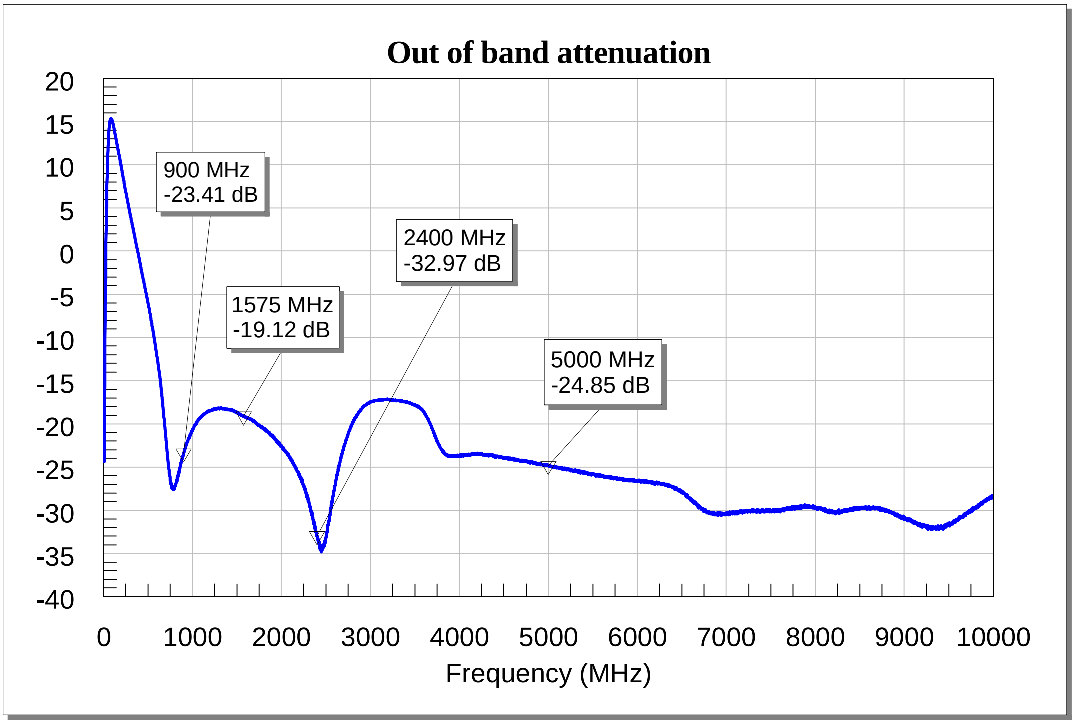


Figure 17 Out-of-Band attenuation with best input matching

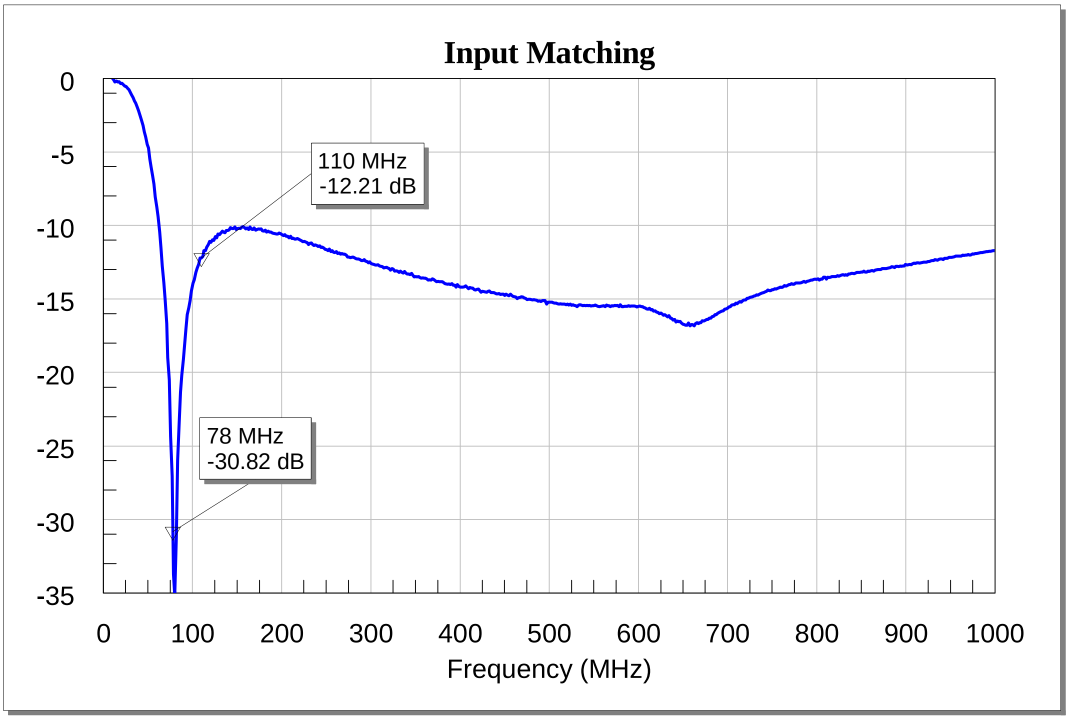


Figure 18 Input matching with best input matching

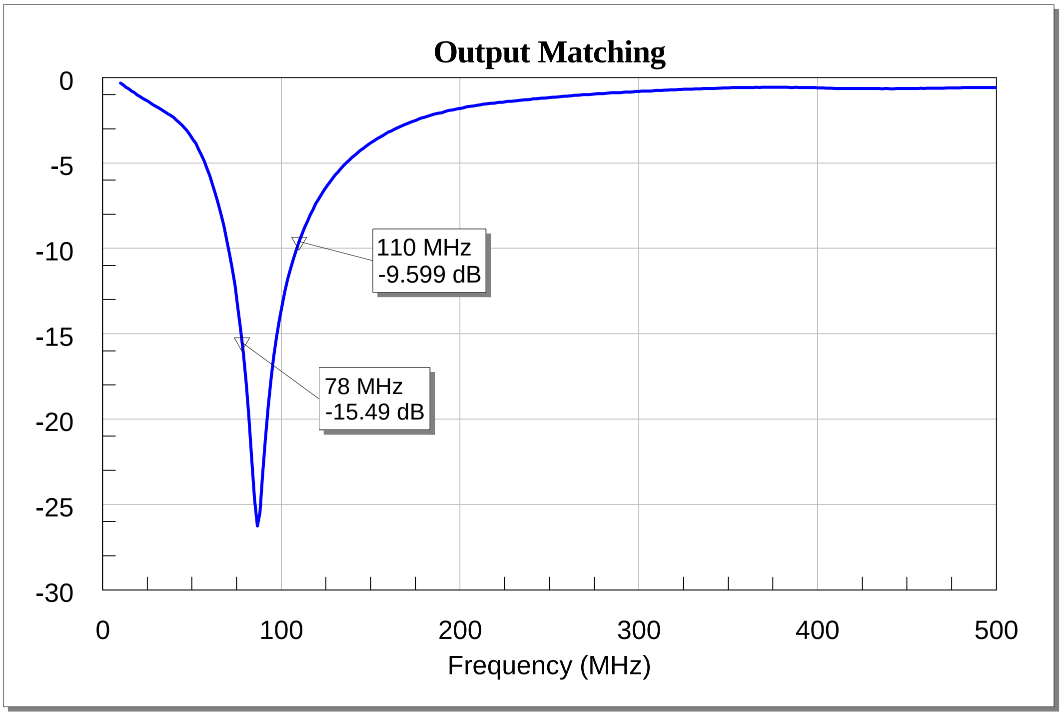
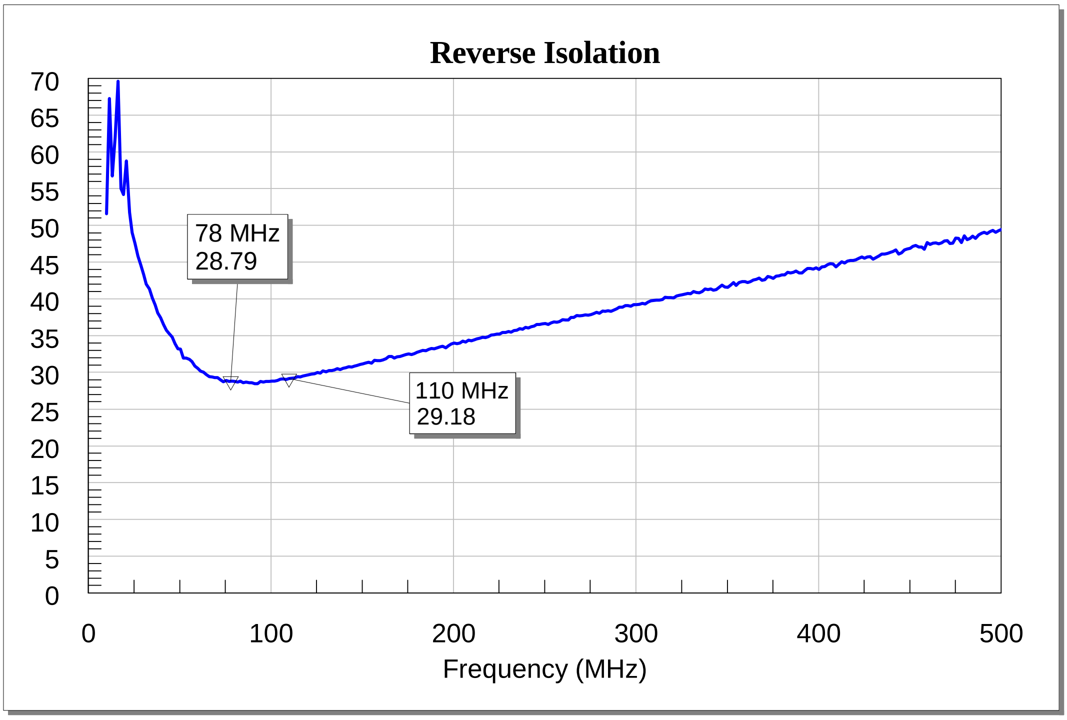


Figure 19 Output Matching with best input matching



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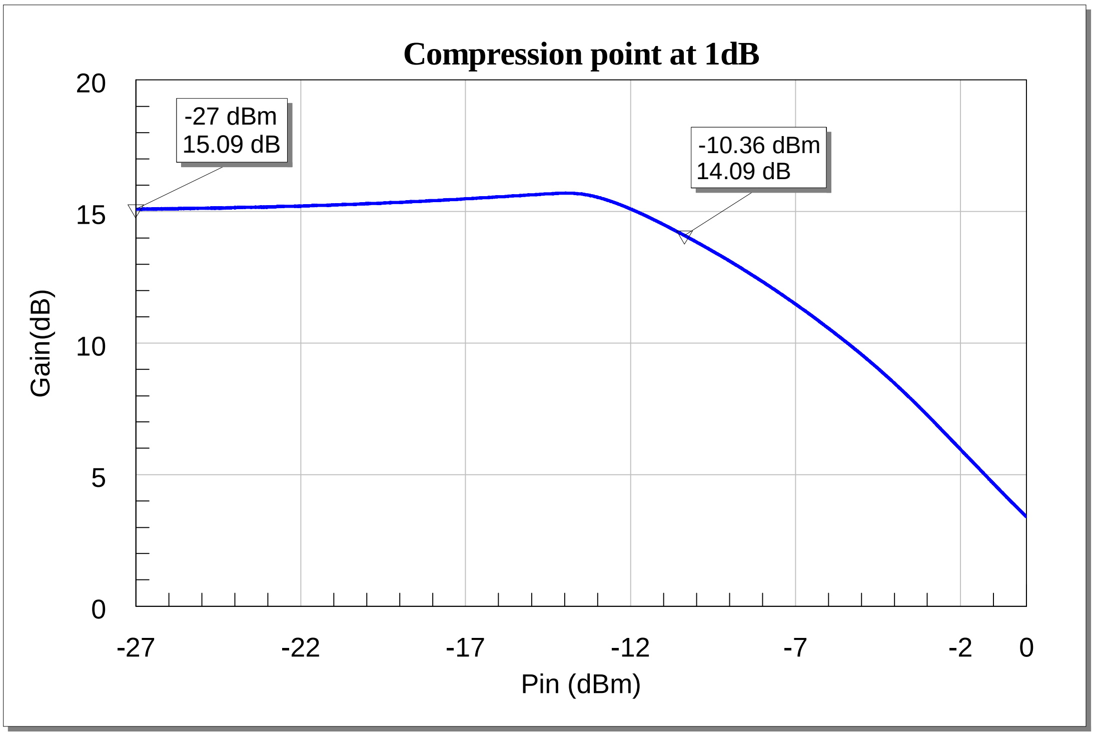

Figure 21 Input 1dB ompression point with best input matching

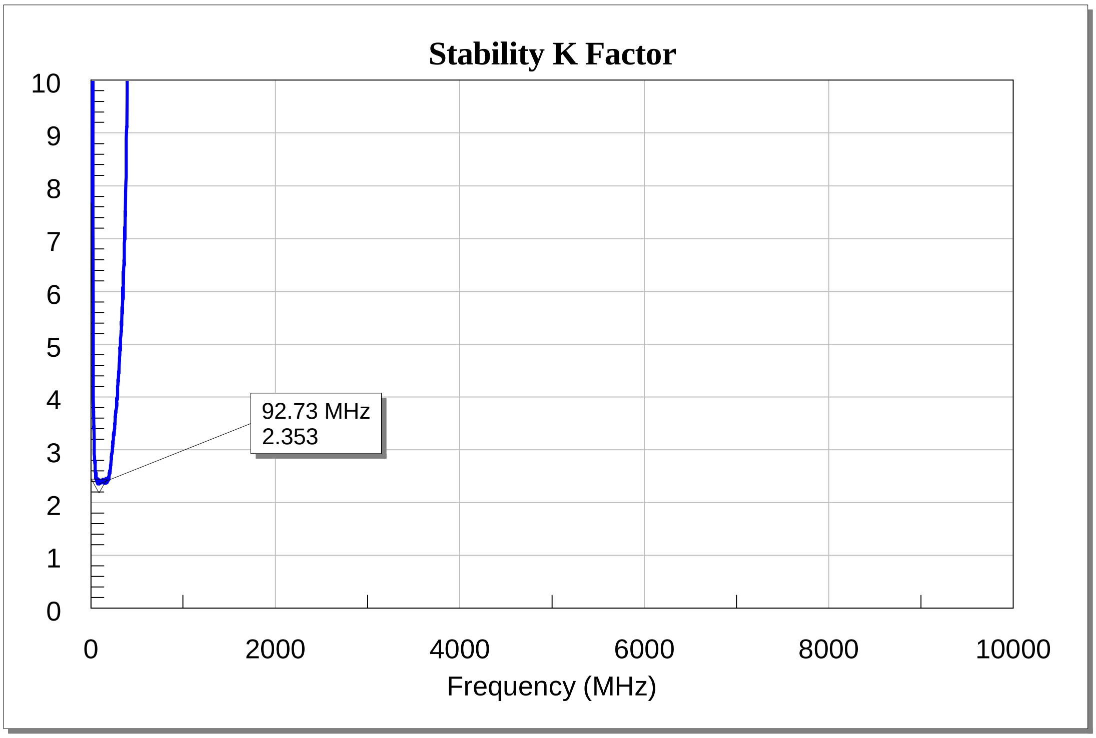

Figure 22 Stability factor K with best input matching.

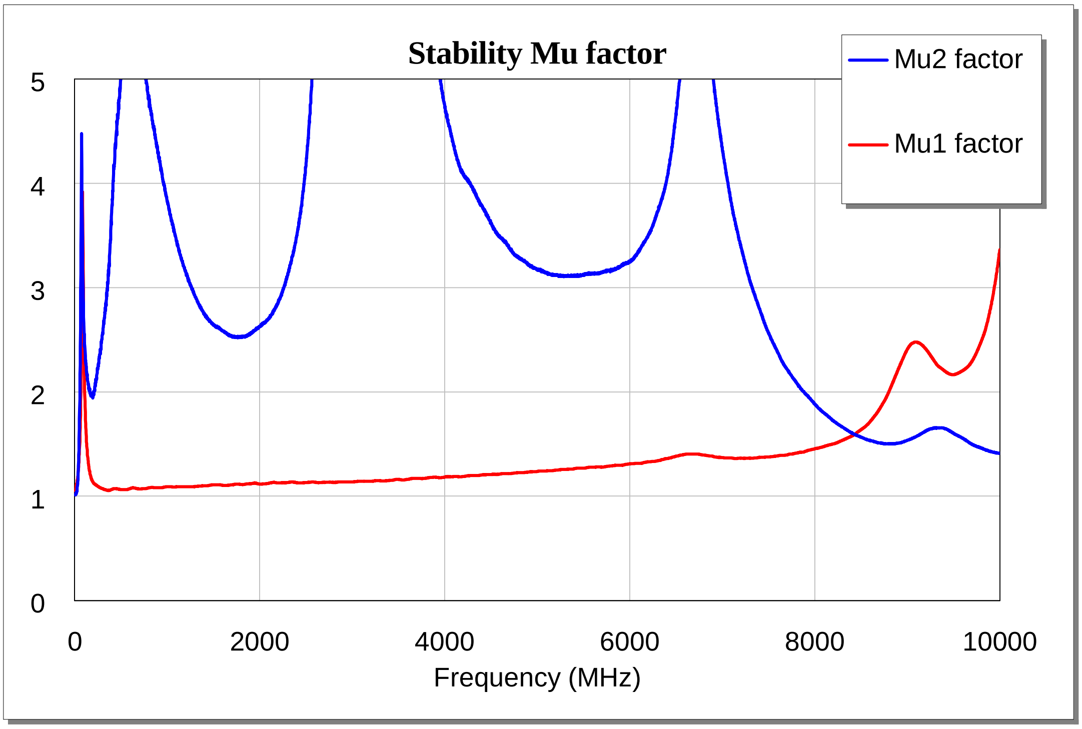

Figure 23 Stability factor μ1 and μ2 of with best input matching

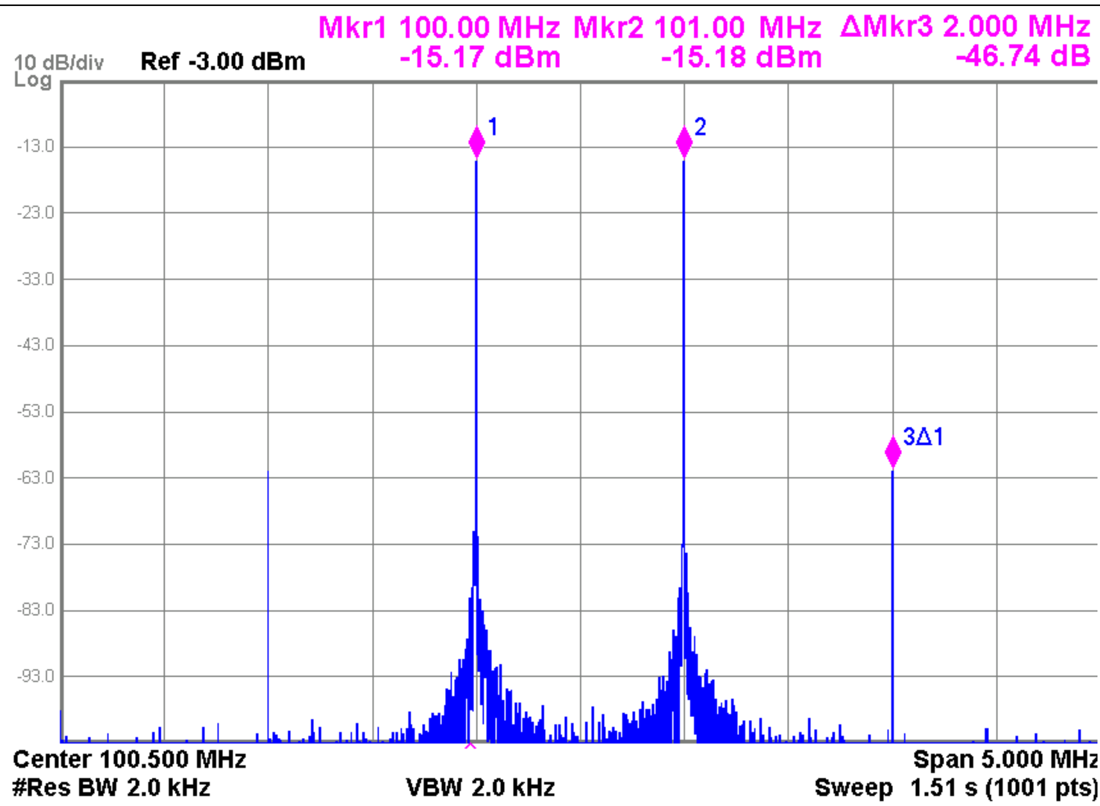

Figure 24 Output 3rd order intermodulation distortion with best input matching

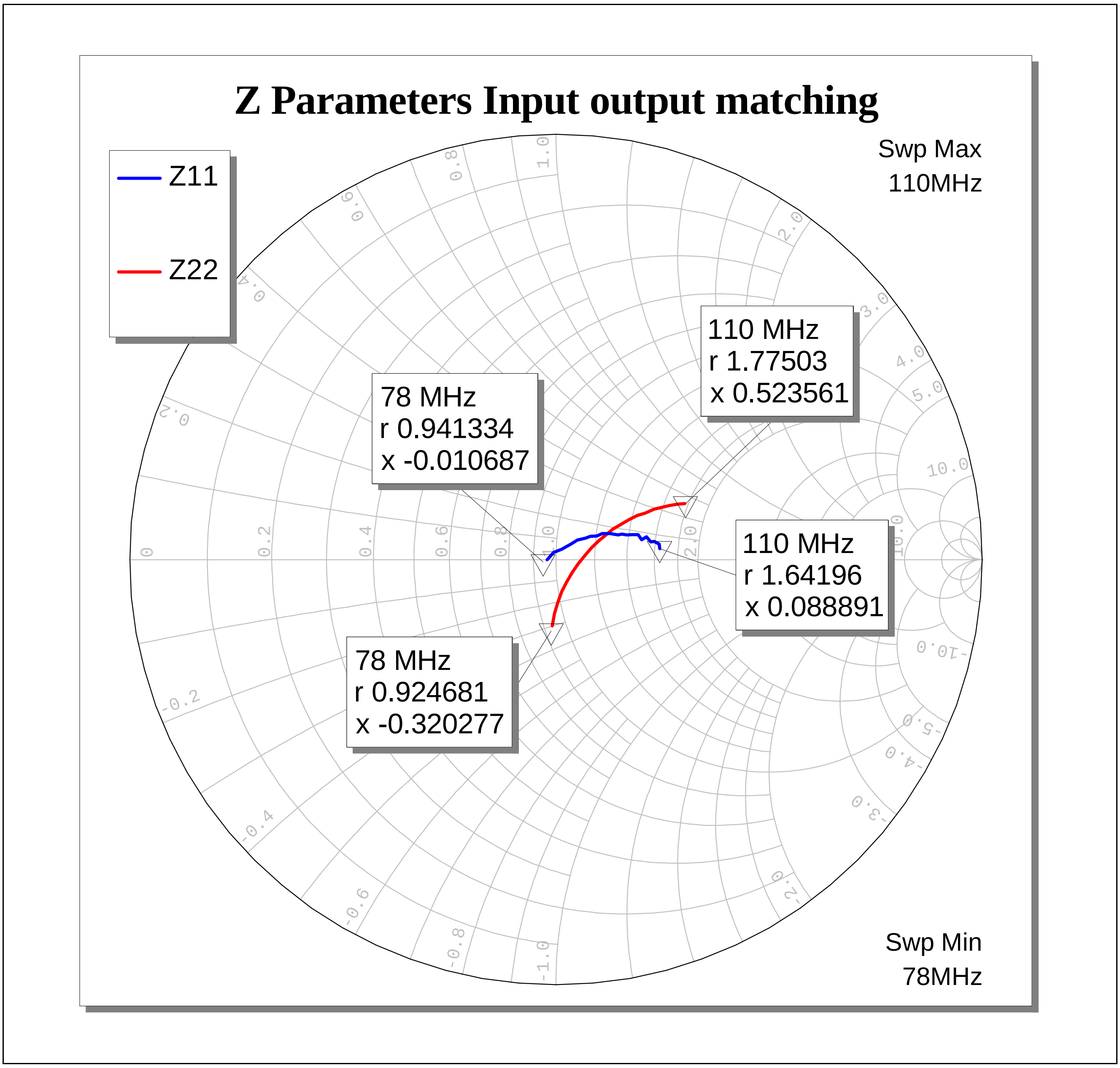

Figure 25 Input and Output impedance with best input matching.

5 Evaluation Board

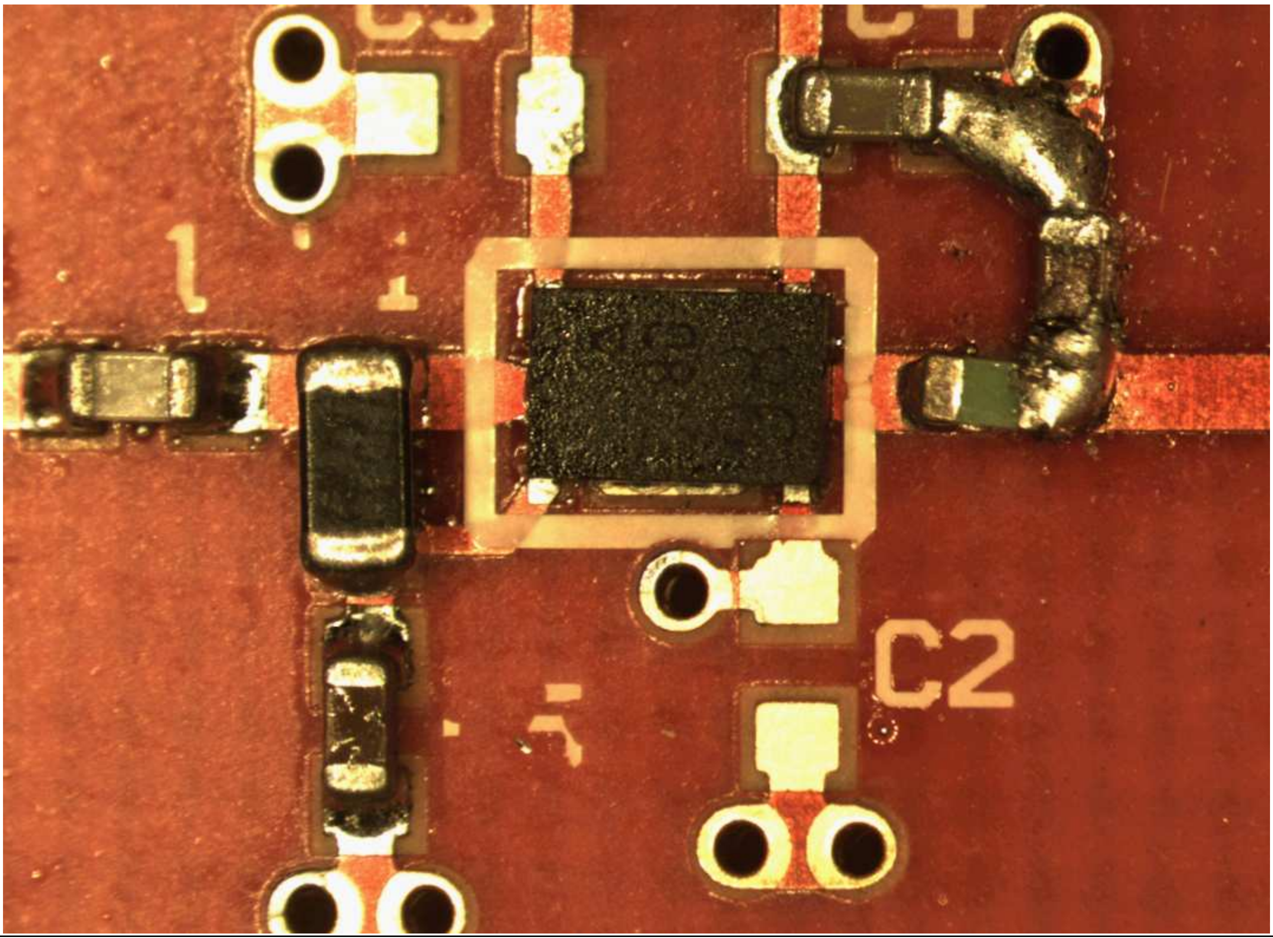

Figure 26 Picture of Evaluation Board

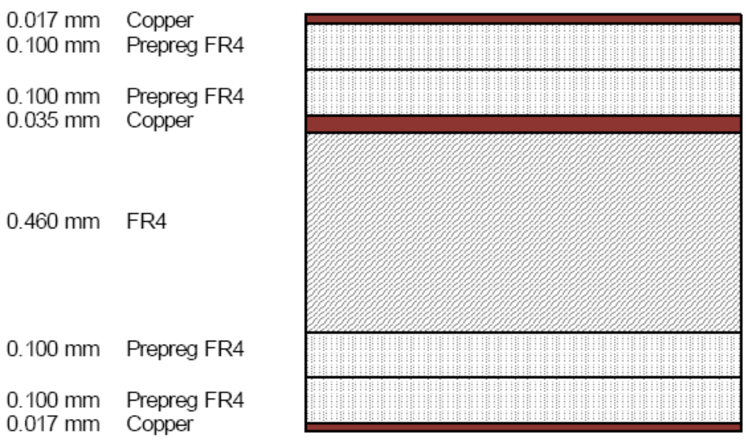

Figure 27 PCB Layer Information

Appendix 1: ESD protection circuit for system level ESD robustness

Introduction

With the advancement in miniaturization of semiconductor structures, ESD handling capability of the devices is becoming a concern. Increasing ESD handling capability of the I/O ports costs additional chip size and affects the I/O capacitance significantly. This is very important for high frequency devices, especially when high linearity is required. Therefore, tailored and cost effective ESD protection devices can be used to build up an ESD protection circuit. To handle ESD events during assembly, devices normally have on-chip ESD protection according to the device level standards e.g. “Human Body Model” JEDEC 22-A-115. To fulfill the much more stringent system level ESD requirements according to IEC61000-4-2 as shown in Figure 28, the external ESD protection circuit has to handle the majority of the ESD strike. The best external ESD protection is achieved using a TVS diode assisted by additional passive components.

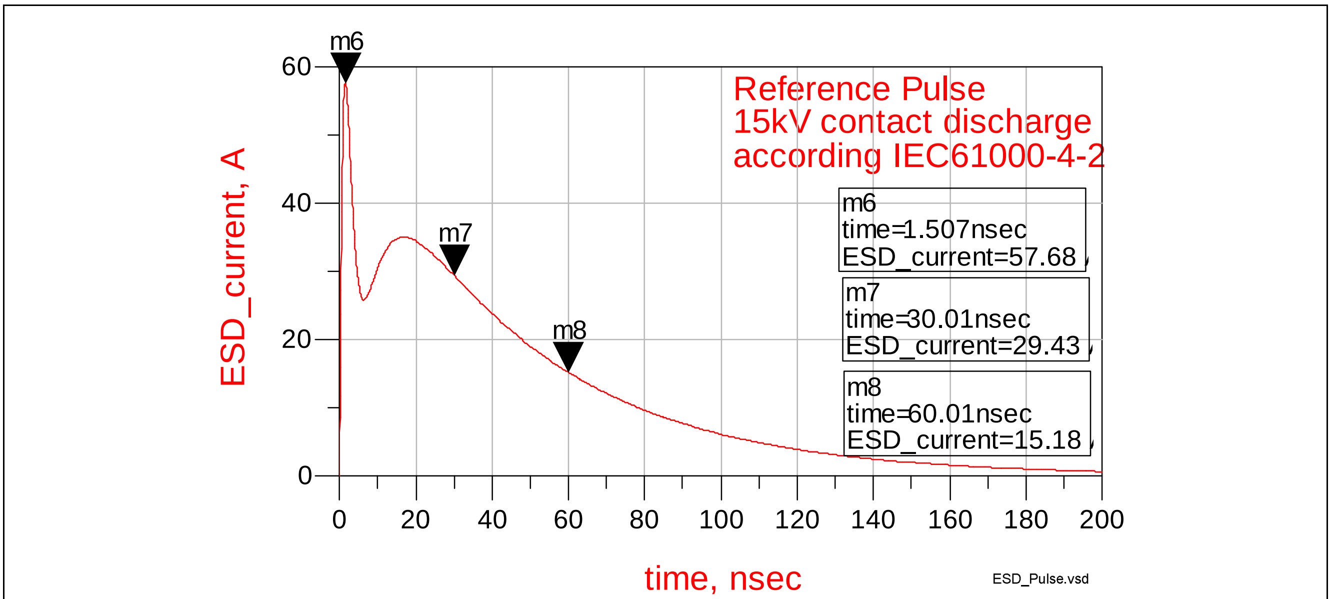

Figure 28 ESD test pulse according to system level specification IEC61000-4-2 – Contact Discharge 15kV

Some examples of RF applications addressed by the Infineon ESD protection proposal are given below:

- FM Radio (76 MHz -110 MHz)
- WLAN 802.11b/g/n (2.4 GHz, Tx ~ +20 dBm)
- Bluetooth (2.4 GHz, Tx ~ +20 dBm)
- Automatic Meter Reading, AMR (900 MHz, TX ~ +20 dBm)
- Remote Keyless Entry, RKE (315 MHz - 434 MHz - 868 MHz - 915 MHz, Tx~13 dBm)
- GPS (1575 MHz, Rx only but can be affected by RF interferer)

For an ESD protection device tailored for medium power RF signals (=< +20 dBm), following requirements are essential:

1. RF requirements
   a) Bidirectional characteristic to handle DC free signals without clipping / signal distortion
   b) A highly symmetrical behavior of the ESD device for positive and negative voltage swings is mandatory to keep the power level of even Harmonics low
   c) Breakdown voltage of 5 V-10V, to avoid signal distortion at high RF voltage swing applied at the TVS diode, located close to the antenna
   d) High linearity
   e) Low leakage current and stable diode capacitance vs. RF voltage swing
   f) Ultra low diode capacitance is mandatory

2. ESD requirements
   a) Lowest dynamic resistance R_{dyn} to offer best protection for the RFIC; R_{dyn} is characterized by Transmission Line Pulse (TLP) measurement
   b) Very fast switch-on time (<<1nsec) to ground the initial peak of an ESD strike according to IEC61000-4-2
   c) No performance degradation over a large number of ESD zaps (>1000)

Two-step ESD Protection approach

General structure for a 2-step ESD approach according to Figure 29 enables to split the entire ESD current between the internal and external ESD protection device. The external device is much more robust and handles the majority of the ESD current. To avoid any impact on the RF behavior of the system and to minimize non linearity effects, the TVS diode should possess an ultra low device capacitance.

Therefore the bi-directional (symmetrical) Infineon TVS Diode ESD0P2RF is well suited, which provides a diode capacitance as low as 0.2 pF and a Rdyn of only 1 Ohm. ESD robustness can be improved one step more by adding a small serial resistor between the external TVS diode and the RF amplifier input. A resistor of ~2.2 Ohm is a good compromise between additional ESD performance and insertion loss. The TVS diode ESD0P2RF in combination with the 2.2 Ohm ESD resistor would incur less than 0.23dB insertion loss up to 3 GHz.

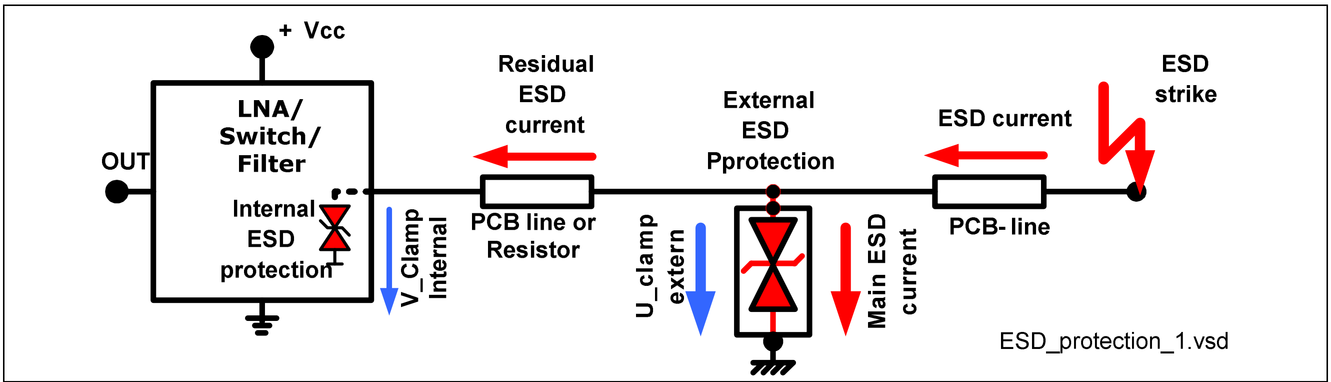

Figure 29 Smart 2-step ESD protection approach based on external and internal ESD protection structure

For further ESD improvement it is highly recommend to add a serial capacitor (C1). The capacitor cuts off most of the high energy created by the ESD strike. For better ESD robustness, C1 should be as small as possible, but has to match to the intended application frequency as well. For a broadband ESD protection (80MHz…3GHz) C1 should be about 100pF…150pF. Optional matching can be implemented with a serial inductor L1 for a dedicated frequency. In combination with L1, C1 can be reduced significantly which improves the ESD performance.

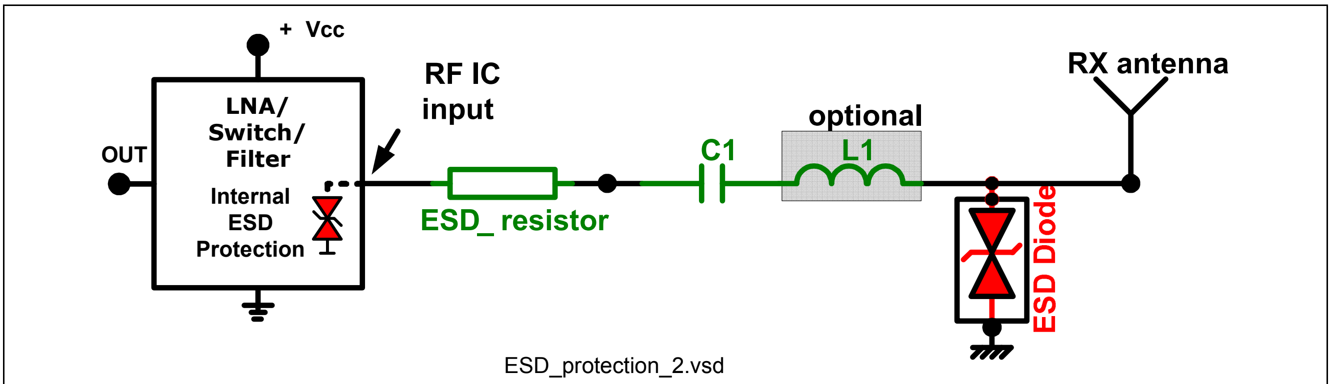

Figure 30 Standard ESD protection topology with optional ESD resistor, blocking capacitor and a serial inductor

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