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New SiC Thin-Wafer Technology Paving the Way of Schottky Diodes with Improved Performance and Reliability

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This article presents the new thinQ!™ 5th Generation (G5) of SiC Schottky diodes from Infineon Technologies. In G5, both the capacitive charge and the forward voltage have been minimized through a new and exclusive production process. The improvements with respect to previous generations are discussed, with the support of direct application tests results. **Vladimir Scarpa, Uwe Kirchner, Ronny Kern, and Rolf Gerlach, Infineon Technologies, Villach (Austria) and Neubiberg (Germany)**

Silicon Carbide (SiC) Schottky barrier diodes (SBDs) have been on the market since more than a decade and sell today in millions of pieces per year, with proven quality in the field. This confirms it as a mature technology, able to provide both full reliable and high-performance devices [6]. Moreover, the increasing request for energy efficiency experienced in the last years is at the base of the constantly growing observed in many applications. Besides high-end server and telecom SMPS, where SiC SBDs have become a standard, increasing adoption is recorded mainly in solar inverters, motor drives and lighting.

Figure 1 summarizes the sequence of 600 V SiC SBD launched by Infineon Technologies. Each new technology aimed to achieve a better price/performance ratio, thanks to new features, translated into key benefits at application level. In thinQ! second Generation (G2), a merged pn-junction has been integrated in the device structure, in order to reduce the diode losses under high current conditions, enhancing therefore the surge current capability of the devices [6].

In the third generation (G3) a new solder technique has been introduced, namely diffusion soldering [6], resulting into an improved thermal conduction between the device chip and the lead-frame. Main results are a lower junction-to-case thermal resistance Rth,JC, and consequently higher power dissipation per device area.

The newest fifth generation (G5) combines the above mentioned improvements of former technologies with new features. The breakdown voltage has been increased to 650 V, while the devices are now produced with the exclusive thin-wafer technology [6], combined with a compacter cell layout, which enable to obtain lower device capacitive charge.

Technology background

As extensively described in a previous publication [6], Infineon Technologies has developed a manufacturing process able to reduce the wafer thickness down to ~1/3 of the original one, as shown in Figure 2a, without increasing the number of defects per unit area in the SiC wafer. The thinning of the substrate results into a smaller differential resistance of the diode, with a clear effect on the output characteristics of the device for the same unit area (Figure 2b).

For a 650V SiC SBD, the substrate component is dominant in the overall diode resistance. Thin-wafer technology enables thus a significant reduction of the diode differential resistance, for identical chip sizes. This is graphically represented in the horizontal line in Figure 2b, which indicates the forward characteristics of two the wafers with different substrate thickness.

Together with the electrical characteristics, the thermal behavior of the G5 chip is also improved. A thinner chip results in a better thermal path between the wafer and the lead-frame. As a consequence, identical power dissipation leads to a smaller junction temperature increase in a G5 device compared to G2.

Figure 3 shows the thermal simulation of SiC Diodes with equal sized chips but different thicknesses in a TO220 package (P_{losses}=75 W). The color scheme indicates the temperature in °C. The backside of the lead-frame is hold to constant temperature (0°C). Here one can see that, for G5, the chip junction temperature is much lower due to improved thermal conduction to the lead-frame. In addition, better heat spreading into the copper lead-frame is observed in the G5 device.

Tailoring of the devices

Devices in G5 have been tailored to have forward voltage V_f=1.5 V under a given nominal current and junction temperature T_j=25°C. Figure 4a schematically shows the positioning of the actual three families of SiC SBDs, with respect to V_f and Q_c - the total capacitive charge at a reverse voltage V_R=400V, for the same nominal current. Figure 4b compares several current rated devices, from G2 and G5, where it is possible to see the massive reduction of the Q_c (30-40%) in G5 devices.

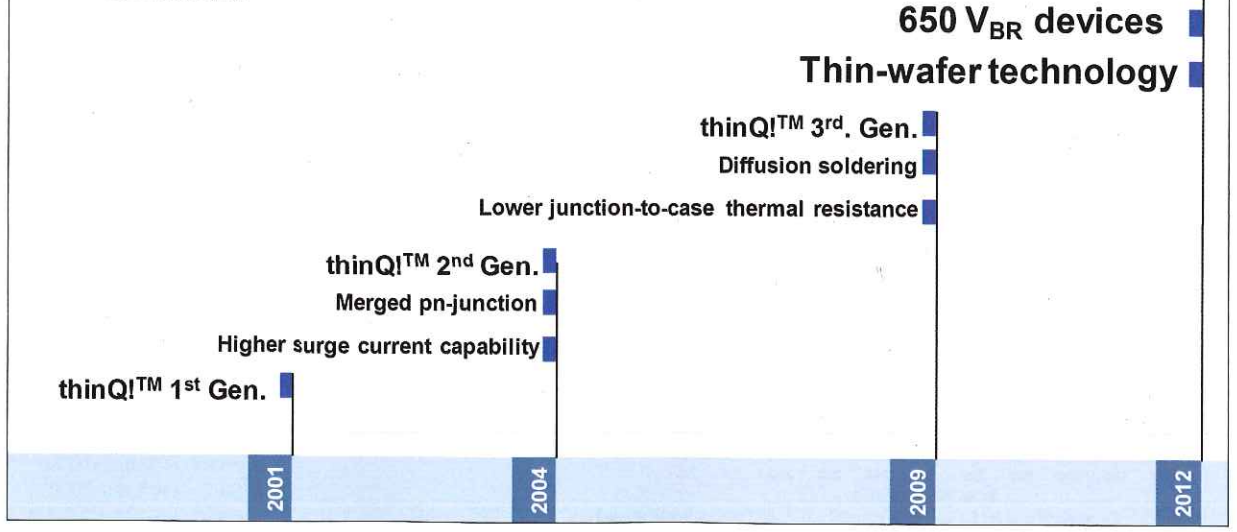
By comparing G2 with G5, the total charge Q_c is reduced despite same V_f, with consequent lower switching losses, as indicated by the blue arrow. By comparing G2 with G3, instead, G5 has comparable Q_c but lower V_f, and consequently lower conductions losses, as again indicated by the arrow.

Thermal resistance and surge current capability

With respect to device reliability of a power device, at least two other parameters are of great importance, namely the thermal resistance between junction and case, $R_{th,JC}$, and the surge current capability [6]. Therefore the datasheets contain as parameters the $R_{th,JC}$, the maximum surge current, IF,SM, evaluated for 10 ms sinusoidal current pulse, and the non-repetitive peak forward current If,MAX for after 10 µs rectangular current pulse.

In Figure 5 the three mentioned parameters for 8A devices in TO-220 package are plotted with respect to G5 values - absolute values can be found in [6]. As predicted by its better thermal behavior, G5 has a smaller R_{thJC} compared to G2 and G3. Moreover, $I_{F,SM}$ and $I_{f,MAX}$ of

Figure 1: Timeline of SiC SBD generations from Infineon Technologies



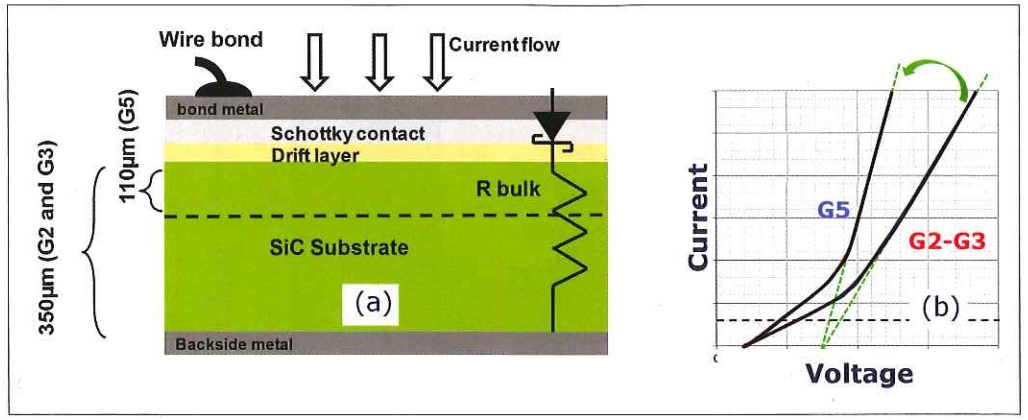


Figure 2: Schematic representation of a SiC diode with thick and thin wafers (a) and forward characteristics of identical sized devices with thick (G2-G3) and thin (G5) substrates (b)

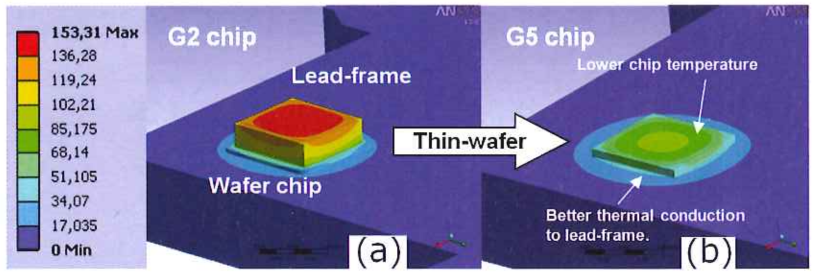


Figure 3: Thermal behavior of G2 device with thick chip thickness and soft soldering (a) while (b) shows a thin chip with diffusion soldering

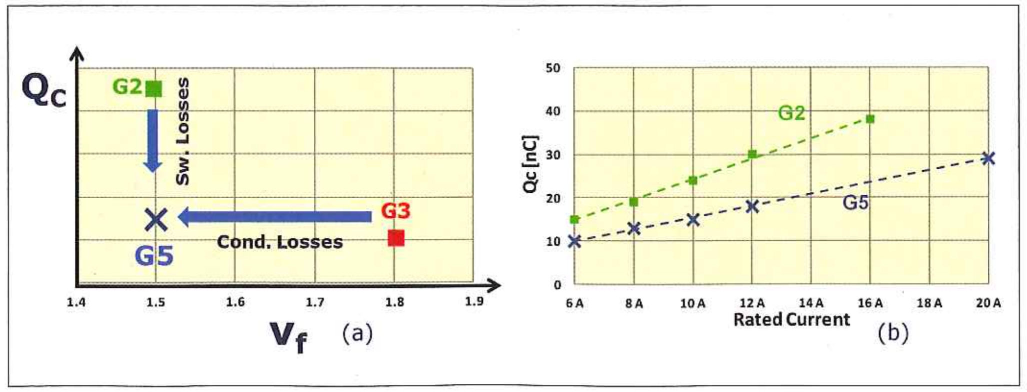


Figure 4: Device tailoring in G5, comparison with G2 and G3 regarding of Q_c and V_f (a). Arrows represent the benefit in terms of device lower losses. Comparison of device Q_c between 5G and G2 for several current ratings (b)

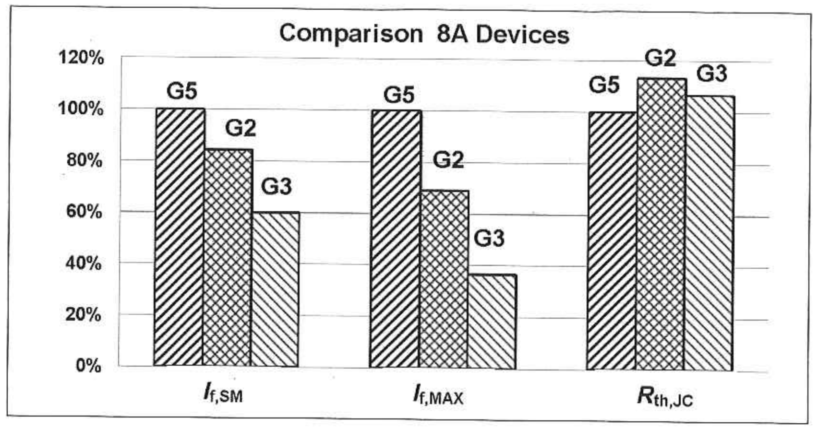


Figure 5: Comparison of surge current capabilities ($I_{F,MAX}$ and $I_{F,SM}$) and thermal resistance $R_{th,JC}$ between SiC SBD technologies (all data taken from datasheet of the corresponding 8A devices and are referenced to G5)

G5 is always larger than the other generations.

In G5, the lower $R_{th,JC}$ can be explained by the better heat dissipation of the thin chip. In addition, thermal behavior has also an impact on the surge current capability: G5 device is thus able to support higher current values, i.e. higher losses, before reaching the maximum junction temperature, and its consequent destruction.

CCM PFC application results

The performance of the G5 devices has been evaluated in a step-up circuit (boost). The setup is fed by the AC means (V_{in}=230 VAC) and contains a power factor correction (PFC) controller, for continuous current mode (CCM) operation. Further parameters and component values are presented in [4]. Figure 6 shows the CCM PFC circuit used in the experimental tests and its main parameters/component values. Figure 7a shows the efficiency curves of the above described circuit, as a function of the output power from different technology generations. In Figure 7b the efficiency is normalized to G5.

It is shown that the efficiency of G5 is higher than G2, especially at light load due to lower Q_c, i.e. lower switching losses. Vice versa, G5 is better than G3 is at high load conditions due to lower Vf values, i.e. lower conduction losses. Within the three discussed generations the G5 has the lower product Q_c x V_f, and becomes therefore benchmark in efficiency for the entire power range.

Conclusion

This article has introduced the new family of SiC Schottky barrier diodes from Infineon Technologies, produced through a new and exclusive thin-wafer technology. The main electrical and thermal benefits related to the thin-wafer technology have been addressed, as well as their impact in the device performance. As demonstrated by experimental tests in a PFC circuit, G5 offer the best balance between conduction and switching losses, offering the best efficiency to the system, over the full load range.

Literature

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Param.	Description	Value
V_{in}	Input voltage	$230V_{ac}$
V_{out}	Output voltage	$400V_{dc}$
$P_{o.max}$	Max. output power	1.5kW
S	Power switch	IPW60R075CP
L	Inductance	680µH
f_{sw}	Switching frequency	100 kHz
T_{hs}	Heat-sink temperature	60°C

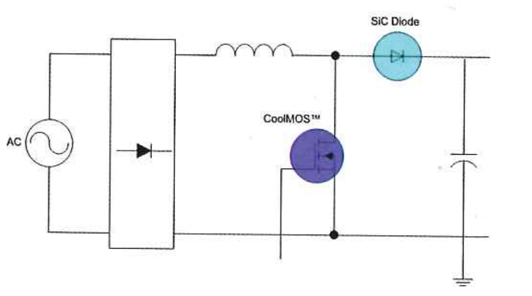

Figure 6: CCM PFC circuit used in the experimental tests and its main parameters/ component values

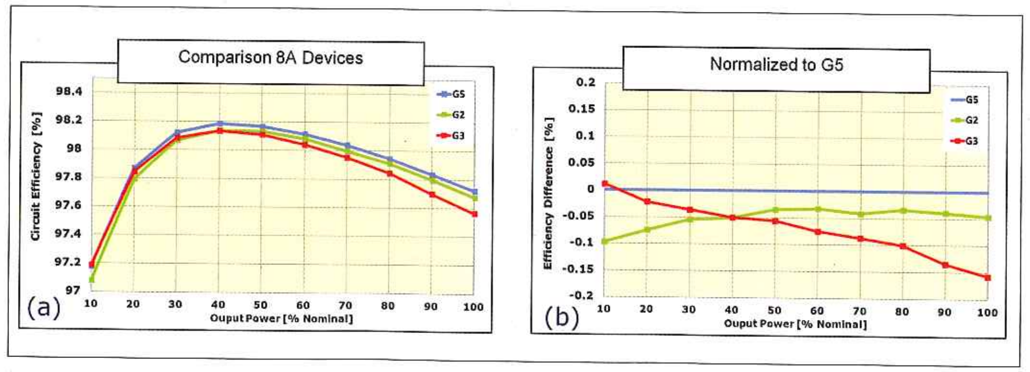

Figure 7: Efficiency results of PFC circuit with 8A devices from G2, G3, and G5 over full output range (parameters see Figure 6) in absolute values (a) and normalized values to G5 (b)