

# REF\_48V\_2X1KW\_ASFOC dual-motor drive for robotics applications

## About this document

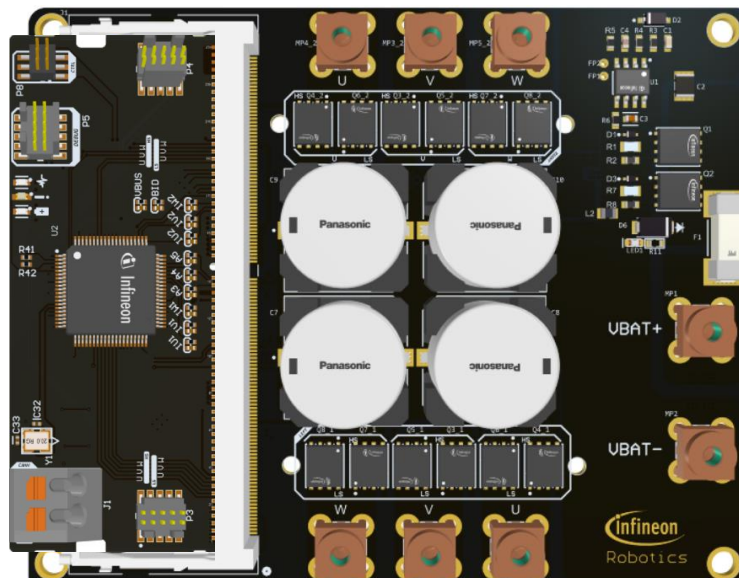
### Scope and purpose

This document describes the procedure for sensored field-oriented control (FOC) implemented on the REF\_48V\_2X1KW\_ASFOC Evaluation Board for a dual-wheel robotics solution. The following reference design highlights the efficient deployment of a single microcontroller's ability to synchronously drive two BLDC motors. The board provided in the evaluation kit is designed to run two motors rated at 1 kW per side with a switching speed of 20 kHz.

Detailed explanations of each component featured in the reference design should assist integrators effectively utilize the included components.

### Intended audience

Infineon applications engineers and technicians, and external partners who intend to develop a robotics dual-wheel drive system.



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## Important notice

### Important notice

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## Safety precautions

### Safety precautions

*Note:* Please note the following warnings regarding the hazards associated with development systems

**Table 1** Safety precautions

	<b>Warning:</b> The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.
	<b>Warning:</b> Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.
	<b>Caution:</b> The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.
	<b>Caution:</b> Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.
	<b>Caution:</b> The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	<b>Caution:</b> A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.
	<b>Caution:</b> The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.

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## Introduction

### 1 Introduction

REF\_48V\_2X1KW\_ASFOC is a reference design to demonstrate synchronous dual-BLDC motor control using a single microcontroller. The intended use case for the board is to drive the wheels of an autonomous mobile robot (AMR) or autonomous guided vehicle (AGV). The system includes the following Infineon components:

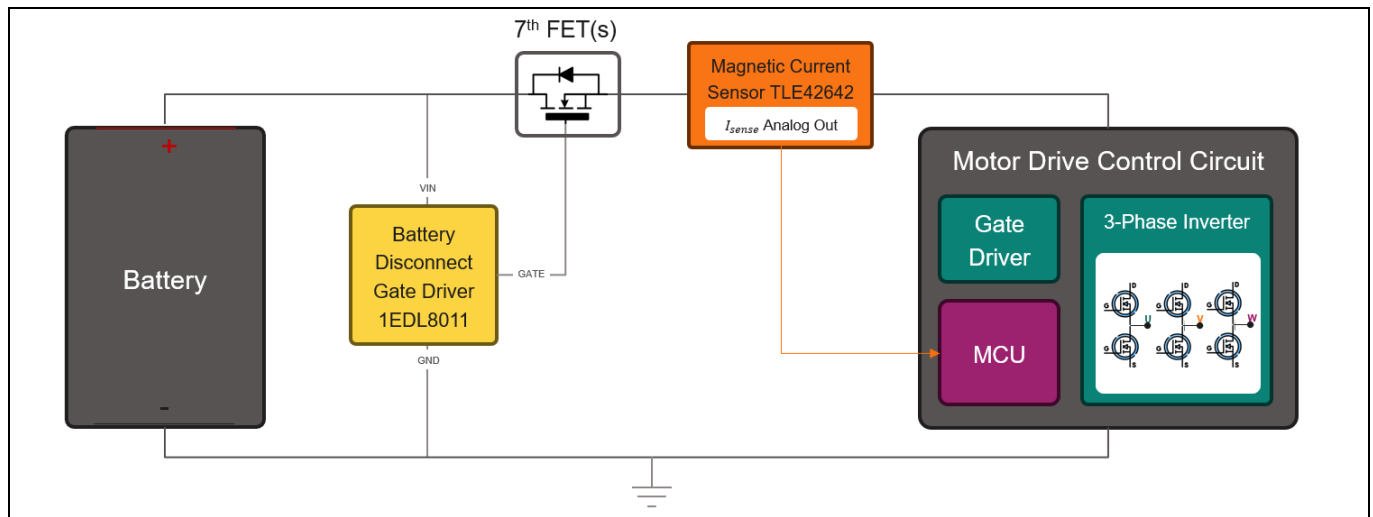
- PSC3M5FDS2AQ1 (MCU) X 1
- 6EDL7151 (Gate driver) X 3
- ISC031N08NM6 (80 V, 3.1 mΩ) X 12
- ISC025N08NM5LF2 (80 V, 2.55 mΩ, 5x6) X 2
- 1EDL8011 (Battery disconnect switch) X 1
- TLE42642 (Magnetic current sensor) X 1
- TLI5012B E1000 (Angle sensor) X 2
- TLE9351BVSJ (CAN transceiver) X 1

The description of how each of these components interact within the reference design is described in Section [1.2](#).

#### 1.1 System block diagrams

The system block diagrams cascade into two levels. The first block outlines the power input protection devices while the second illustrates purely the motor control portion of the circuit.

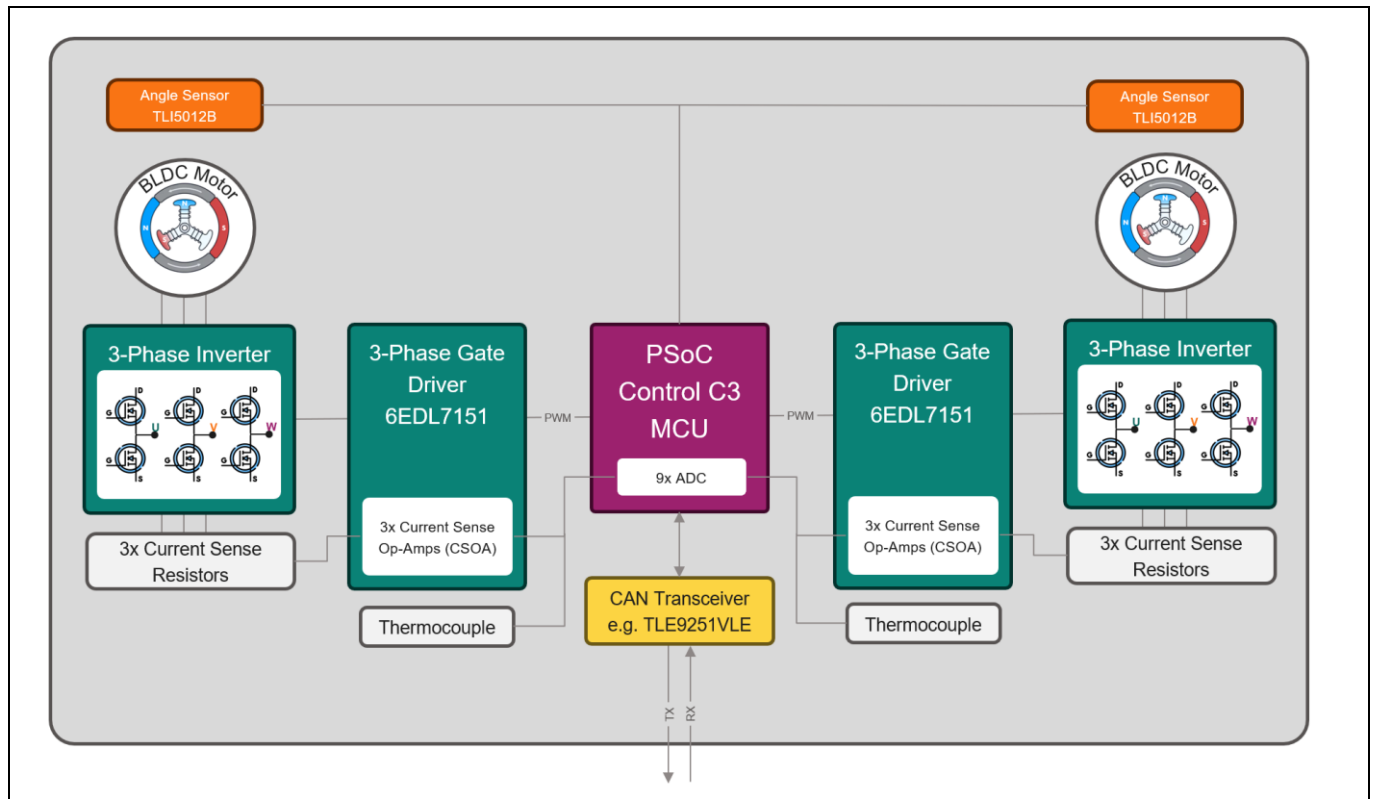
##### 1.1.1 Power input protection interconnect block diagram



**Figure 1** Block diagram: Power input protection interconnect

## Introduction

### 1.1.2 Motor drive block diagram



**Figure 2** Motor drive block diagram

## 1.2 System description

Understanding the behavior of this circuit involves two key aspects:

- Operation of the digital components
- Power provisioning from the battery to system

### 1.2.1 Operation of digital components

First, the document examines how each digital component functions within the circuit. This includes analyzing the roles of microcontrollers, sensors, and other integrated circuits that govern the digital logic and processing tasks.

Infineon's PSOC Control C3 (PSC3M5FDS2AQ1) is a 180 MHz Arm® Cortex® M33-based MCU that handles the FOC control loop. For each side, the peripheral components required for motor control include:

- A BLDC motor
- A magnetic angle sensor
- A three-phase gate driver
- Three shunt resistors
- Three current-sense op amps

## Introduction

Upon receiving the commands to spin the motor – either through the CAN bus or via SWD – PSOC Control C3 reads the position and speed of the motor using the TLI5012B magnetic angle sensor. Using this information as a parametric input to the field-oriented control loop, the controller calculates and broadcasts the correct switching sequences through its 6 PWM outputs. The 6EDL7151 gate drivers amplify each of the low current PWM signals to drive the gates of each OptiMOS™ 6 (ISC031N08NM6) MOSFET. To read more on gate driver characteristics, see References [1].

Each phase in the inverter contains a high-side and low-side switch. The electrical load of the motor can be anywhere from 0 to 1000 W. For an operating voltage of 48 V, this means the continuous current should be between 0 to 20 A. The source of each low side switch is connected to a shunt resistor. The reference voltage sampled across the shunt must be offset and amplified before being read by the ADC, so a current sense op amp is required. However, 6EDL7151 contains three current sense op amps (pins CSOA, CSOB, and CSOC). Once the current measurement data has been acquired by the control loop, the MCU updates the state based on any various service routine inputs (such as directional changes, speed changes, or safety lockout modes).

### 1.2.2 Power delivery and protection

This section looks at how power is supplied from the battery to the system. This involves understanding the power management techniques and circuitry that ensure stable and efficient power delivery to all parts of the system. The input of the reference board is a dual M3 terminal. The ideal mechanical connection of power input leads include using spade terminal connectors, zinc split loc washers, and finally M3\*6 mm machine screws to secure the leads in place.

The REF\_48V\_2X1KW\_ASFOC board contains two power management ICs (PMIC) that prevent overcurrent protection (OCP), overvoltage protection (OVP), and in-line current sensing. In many power applications, including motor drivers and SMPS, the supply architecture often requires a module to be capable of being disconnected from the main supply rail when a malfunction occurs. To achieve this functionality in the reference design, a high-side disconnect switch (1EDL8011) in conjunction with two LinearFETs (OptiMOS™ 5 ISC025N08NM5LF2) act as a disconnect gate driver and switch pair.

*Note: Driving the 1EDL8011 high-side gate driver requires the following power sequence to function:*

1. *V<sub>batt</sub> to has to enter the VIN pin*
2. *A high dv/dt pulse on signal from 0 to 3.3 V; either through the MCU or other logic control method*

After the LinearFETs start operating in conduction mode, the power through the system passes through a magnetic current measurement sensor (TLI4971-A050T5-E0001). The TLI4971 is a high precision coreless current sensor. The current flowing through the current rail on the primary side induces a magnetic field that is differentially measured by two Hall probes. The differential measurement principle of the magnetic field combined with the current rail design provides superior suppression of any ambient magnetic stray fields.

A high-performance amplifier combines the signal resulting from the differential field and the internal compensation information provided by the temperature and stress compensation unit. Finally, the amplifier output signal is fed into a differential output amplifier, which is able to drive the analog output of the sensor.

After the battery input passes through the two power protection ICs, they make their way through the bulk capacitors and into the batt\_sense voltage divider, the result is which is observed by the MCU. The power travels into the two 6EDL7151 gate drivers, both containing onboard buck converters and configurable

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## Introduction

(3.3 V/5 V) logic level outputs. The outputs of the two buck converters enter an ORring diode, an LDO, and finally to the power input pins of the PSOC Control C3 MCU.

Each duty cycle, the MCU reads the batt\_sense voltage divider to verify the battery output voltage remains at an appropriate level (you can define minimum and maximum battery voltage level cutoffs in firmware). If no undervoltage condition is triggered, system continues to run.



## Implementation of REF\_48V\_2X1KW\_ASFOC

## 2 Implementation of REF\_48V\_2X1KW\_ASFOC

This section highlights a few design considerations while implementing the REF\_48V\_2X1KW\_ASFOC reference board into a robotic drivetrain. Setup of the board is described in subsequent sections of the document.

### 2.1 Application considerations

When designing the drive train of a robot, several key parameters must be defined early in the design stage. In this document, following are the two guiding principles paramount for successful system design:

1. **Design with the end in mind:** Consider the ultimate purpose and outcome of a design from the very beginning of the process. This approach involves carefully analyzing the requirements and specifications of the project and anticipating potential challenges and constraints that may arise throughout the development and implementation phases.
2. **Plan for the most difficult operational circumstances:** Anticipate and prepare for extreme or challenging conditions during the operational phase of a project. Think about the harshest environments that your design may need to operate in: High incline, low traction, or heavy load, etc.

#### 2.1.1 Checklist of key parameters

Here are few key parameters crucial in designing the electromechanical system, which should help you determine whether the system solution can deliver the proper output to the system in question.

1	Does your system have a host controller that can send out commands and receive telemetry data over CAN?	<p>What will your communication integration look like?</p> <p><b>Windows/Linux computer</b></p> <ul style="list-style-type: none"> <li>• Background process that can monitor a CAN-to-USB and handle the motion control processing required to steer a robot in its required directions.</li> <li>• CAN-to-USB adapter to send and receive CAN/CAN-FD signals</li> <li>• This might look like using a library – such as python-CAN – to interface with a CAN-to-USB adapter that sends information wheel rotation and receives information such as distance travelled or slippage conditions to make an informed next-decision</li> </ul> <p><b>High Level MCU (i.e., Arduino)</b></p> <ul style="list-style-type: none"> <li>• Runtime script that runs a high-level state machine for controlling the robot's distance and direction travelled</li> <li>• Using a breakout CAN adapter such as the MCP2515 CAN Bus module board for Arduino</li> </ul> <p><b>Raspberry Pi/NVIDIA Jetson type development SoC</b></p> <ul style="list-style-type: none"> <li>• ROS/ROS2 node sending and receiving motor control commands and odometry data</li> <li>• Using a breakout CAN adapter such as the MCP2515 CAN Bus module board or the onboard CAN interface</li> </ul>
2	What is the required torque for the system and what wheel is used for driving the wheels?	See the calculations below:

## Implementation of REF\_48V\_2X1KW\_ASFOC

Torque requirement for motor selection given friction values. In preparation for calculating key parameters for the motor selection, several assumptions need to be made:

### Defining force requirement:

- The mobile robot will operate at a nominal speed of 1 m/s
- Determine  $\mu_F = 0.7$  (We make this critical assumption based on understanding the values of  $\mu_{Fmarble} = 0.4$   $\mu_{Fwood} = 0.2$  and  $\mu_{Fcarpet} = 0.7$ . Since carpet is the most difficult terrain, the robot is anticipated to traverse, we will calculate with this value)
- The mass of the robot in this calculation will be 20 kg (battery + chassis + electronics + wiring)

$$N = 20 \text{ kg} * 9.8 \frac{N}{kg} = 196N$$

### Equation 1

$$F_{friction} = \mu_F * N = 0.7 * 196N = 137.2$$

### Equation 2

To calculate the force required to accelerate this mass,  $F = ma$  is used, where m is the mass of the robot and a is the acceleration.

- If you are aiming for the robot to achieve a velocity of 1 m/s in 5 seconds:

$$a = \frac{\frac{1 \text{ m}}{5 \text{ s}}}{5 \text{ s}} = 0.2 \text{ m/s}^2$$

### Equation 3

$$F_{acceleration} = 20 \text{ kg} * 0.2 \frac{N}{kg} = 4N$$

### Equation 4

Hence, the total force required for the robot to move is:

$$F = F_{friction} + F_{acceleration} = 137.2N + 4N = 141.2N$$

### Equation 5

### Wheel selection:

The wheels should be made of a soft material capable of providing adequate traction on a variety of surfaces. The wheel used should have rubber treads and have a radius of 0.05 m (5 cm).

### Motor parameter requirements:

To calculate the startup torque required to drive the robot,  $\tau = F * r$  is used:

# REF\_48V\_2X1KW\_ASFOC dual-motor drive for robotics applications

## Implementation of REF\_48V\_2X1KW\_ASFOC

$$\tau_{startup} = \frac{141.2N * 0.05m}{2} = 3.53 N.m$$

**Equation 6**

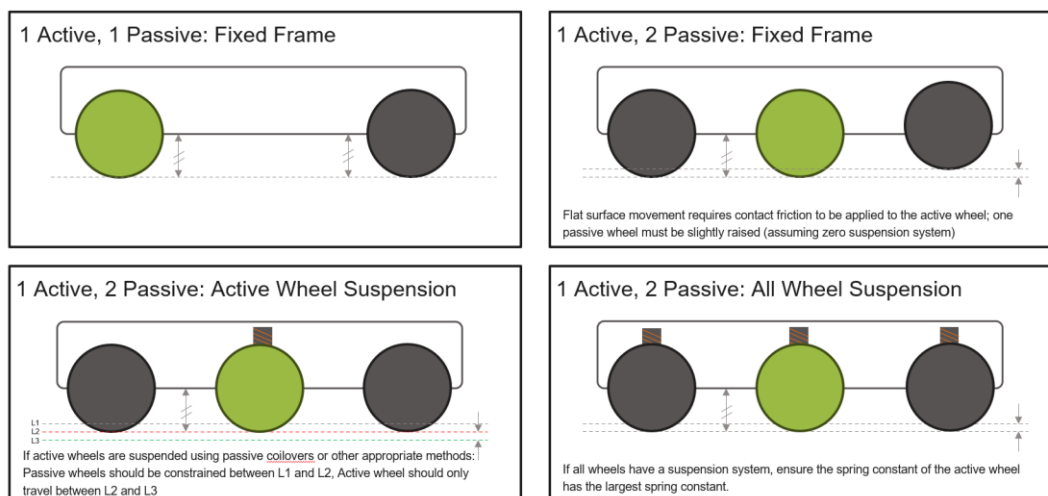
To calculate the nominal torque required to drive the robot, assuming you want to hold constant velocity:

$$\tau_{nominal} = \frac{137.2N * 0.05m}{2} = 3.43N.m$$

**Equation 7**

### Other key mechanical dynamics of the system:

- Each extra set of active wheels can distribute the required torque of each motor by a factor of 2. Hence a 2-wheel system requires a maximum of  $\frac{3.53 N.m}{2} = 1.765 N.m$  per wheel, with the assumption that the robot is driving in a straight line, carrying the load specified in the aforementioned calculation. Ensure the motor chosen is capable of outputting the calculated torque
- Each set of passive wheels does provide stability to the system. However, note the following behaviours of passive wheels confirmations:



3	What motor is used for driving the robot?	<p>The ideal motors to be used in high precision, high torque applications are typically outrunner BLDC motors which possess a high pole pair count.</p> <p>Minimum rating:</p> <ul style="list-style-type: none"> <li>200 W, 12 V supply, 2 A stall current</li> </ul> <p>Maximum rating:</p> <ul style="list-style-type: none"> <li>1000 W, 48 V supply, 20 A</li> </ul>
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## Implementation of REF\_48V\_2X1KW\_ASFOC

4	Is a gearbox be used for this design?	<p>A gearbox can be used to decrease speed and increase the torque of a dynamic system without changing power characteristics.</p> <p>In an example system rated at 1m/s with <math>\tau = 1 \text{ N.m}</math> operates at 0.5 m/s with <math>\tau = 2 \text{ N.m}</math>, if a 2:1 gear ratio is introduced.</p> <p>Planetary gearboxes are popular for their cost and availability. Harmonic/Cycloidal gearboxes are more expensive, but offer near-zero backlash.</p>
5	What battery is used to power the robot?	<p>Are any DCDC converters required for supplying lower voltages to other parts of the system? In the case of a 48 V drive train system, the computer handling the high-level odometry might only require 3.3 to 12 V.</p>

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## Specifications

### 3 Specifications

#### Input and output at normal operation

- DC input voltage 12 to 60 V, nominal 48 V
- Maximum input current 25 A
- Output voltage three-phase FOC
- Maximum output current per phase 20 A<sub>RMS</sub>
- Maximum output continuous power 1000 W per side

#### Control scheme

- Sensor-based FOC
- Switching frequency 20 kHz
- Three current shunts

#### Protection features

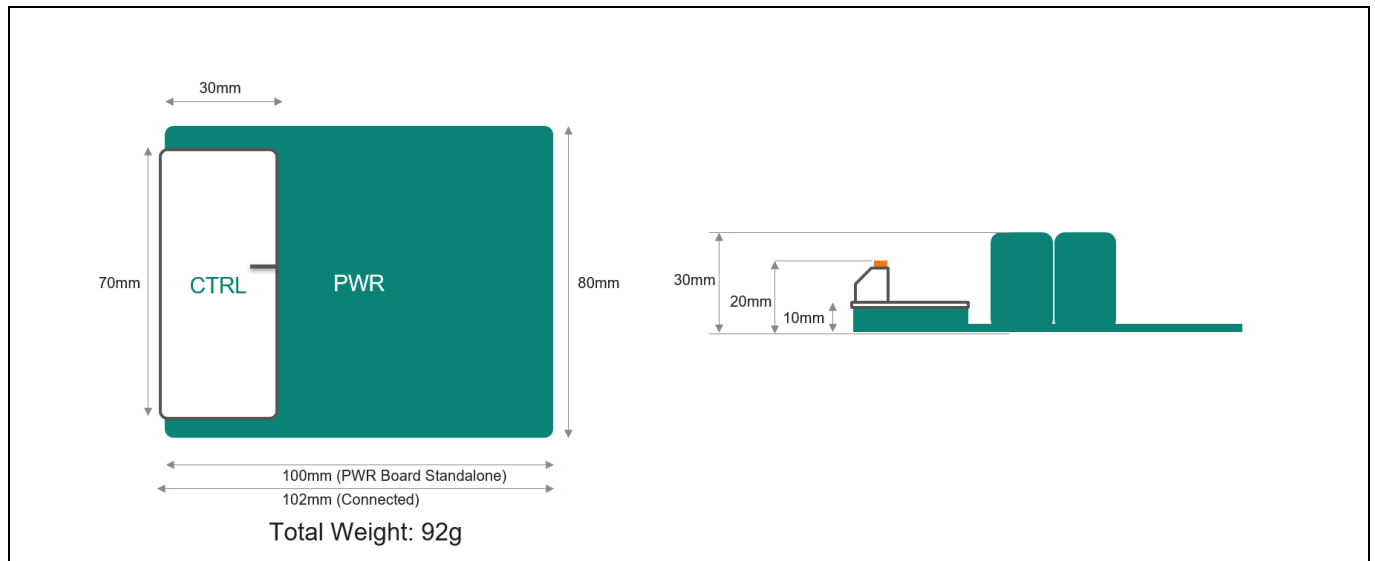
- Input fuse
- OCP/OVP
- High-side disconnect switch

#### Maximum component temperature

- Resistors less than 100°C
- Ceramic capacitors, film capacitors, and electrolytic capacitors less than 100°C
- MOSFET transistors and diodes less than 100°C
- ICs less than 100°C

## Specifications

### Dimensions of the evaluation board



**Figure 3** Evaluation board dimensions

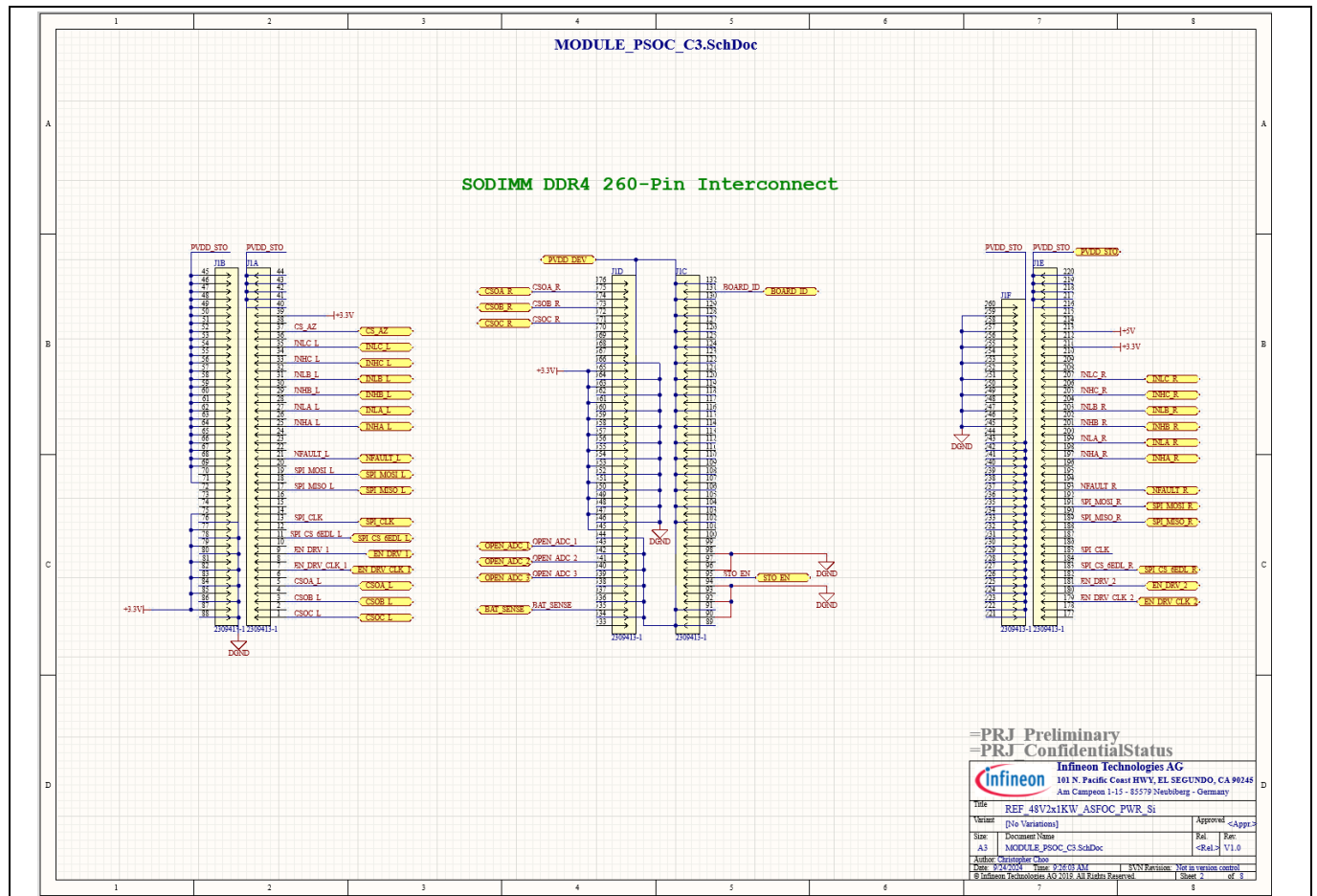
**Note:** In order for this board to operate, the firmware must be configured correctly for the specific motor being driven. This requires motor parameters such as phase-winding inductance and resistance to be entered into the motor control mtb application before flashing the firmware to the target board.

**Attention:** The board should only be tested by qualified engineers and technicians.

## 4 Schematics

**Figure 4** REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - top level schematic

## Schematics



**Figure 5** REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - MODULE\_PSOC\_C3



MODULE\_1EDL8011.SchDoc

STO (Safe Torque-Off)

2x Options 5 LinearFET should be parallel to prevent dissipation of >1W through single FET

STO (Safe Torque-Off)

2x Options 5 LinearFET should be parallel to prevent dissipation of >1W through single FET

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REF 48V2x1KW_ASFOC_PWR_Si		[No Variations]		[No Variations]	
Size:	Document Name	File:	Rev:		
A3	MODULE_1EDL8011.SchDoc	File:	Rev:		
Author:	Designer: Chao	File:	Rev:		
Date:	2-24-2024	Time:	0:58:37 AM		
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**Figure 6** REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - MODULE\_1EDL8011

Schematics

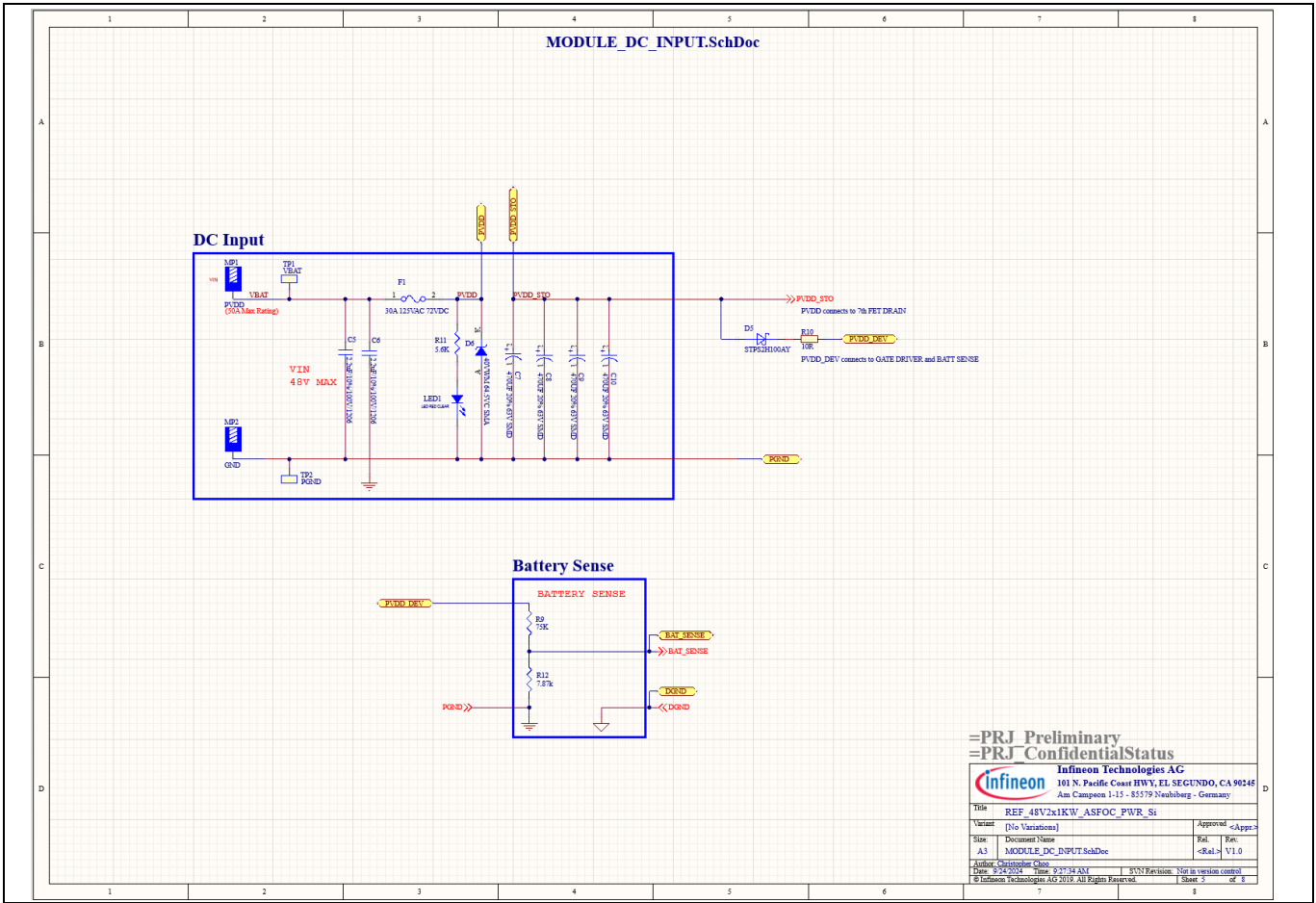


Figure 7 REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - MODULE\_DC\_INPUT

# REF\_48V\_2X1KW\_ASFOC dual-motor drive for robotics applications

## Schematics

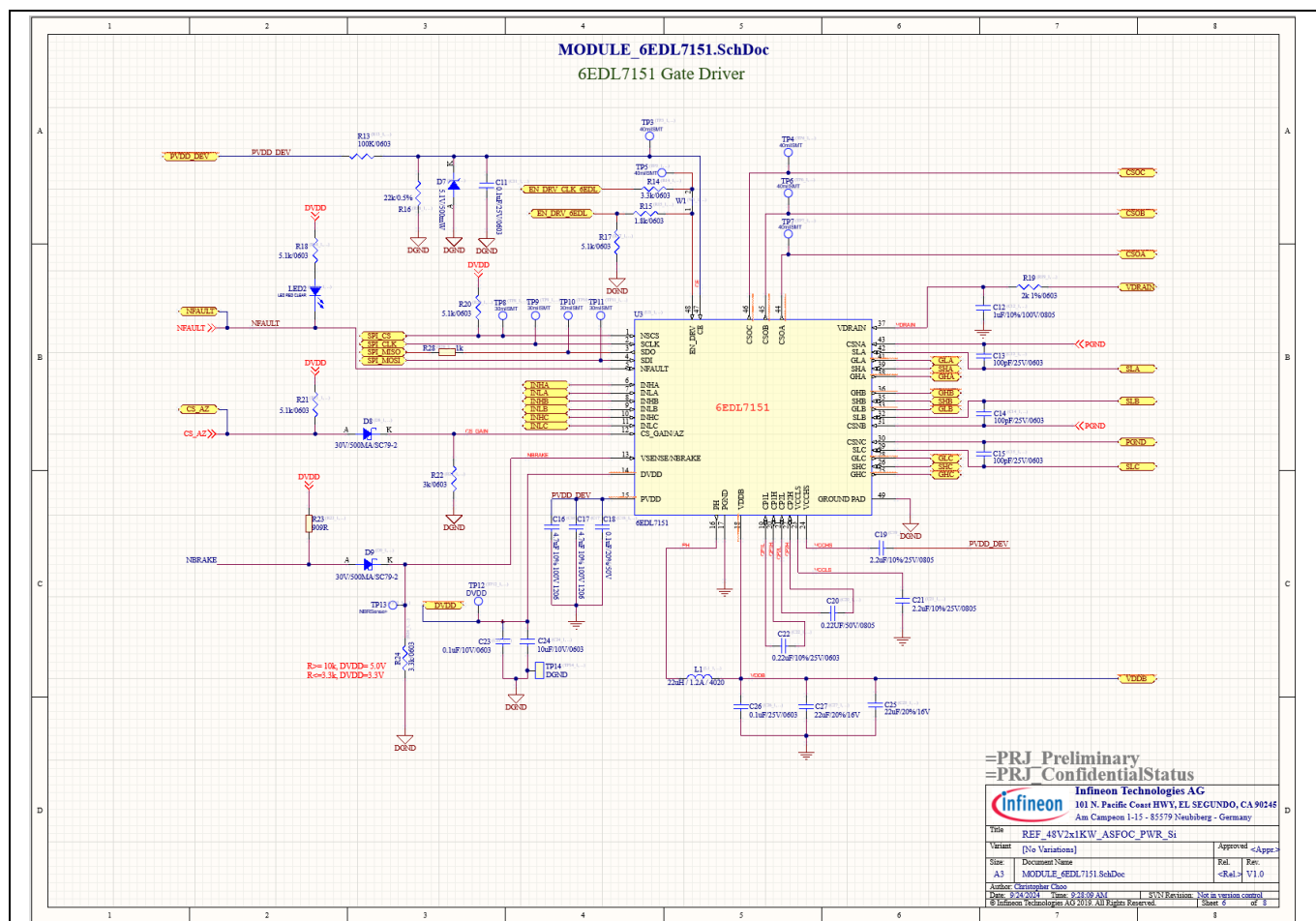
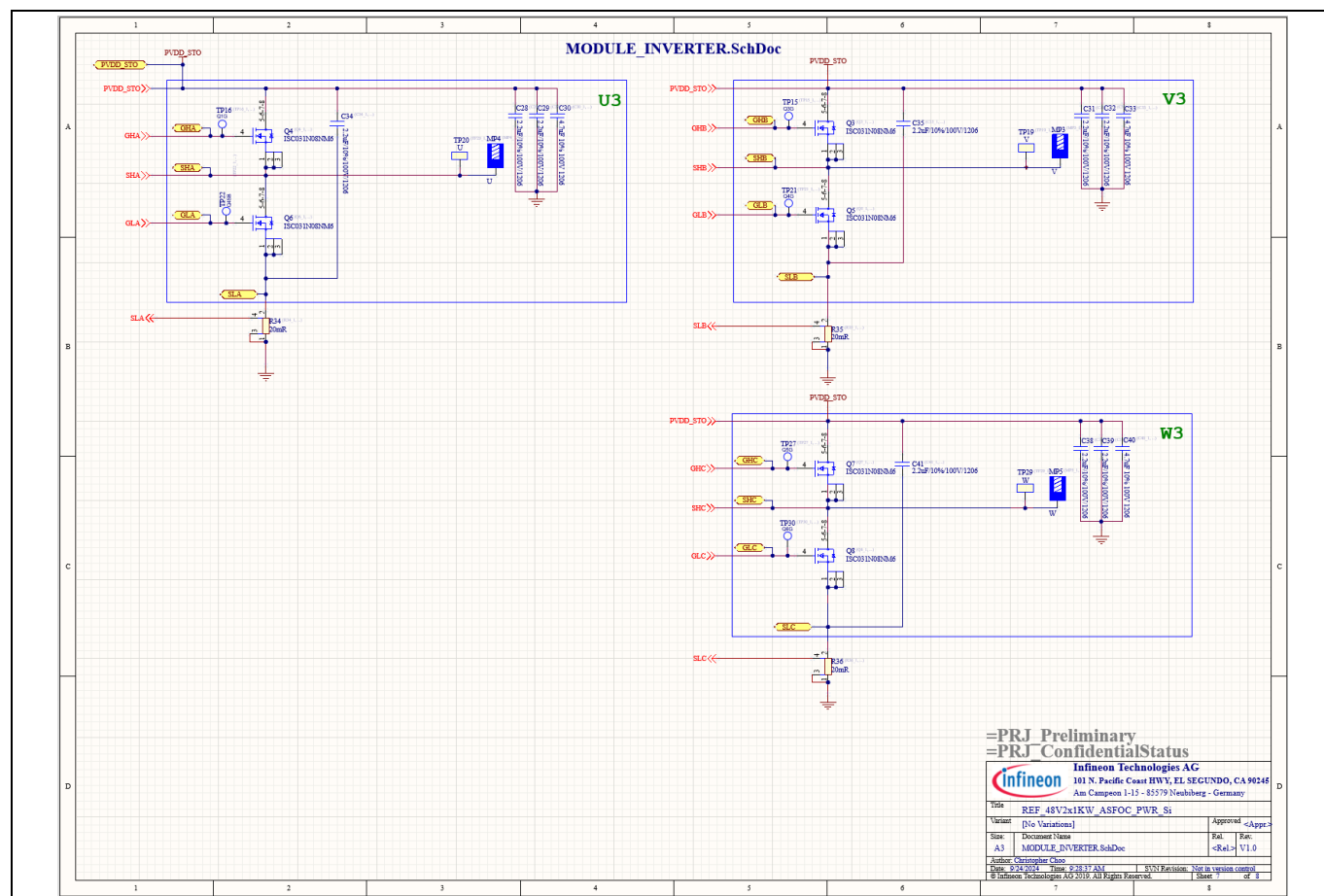


Figure 8 REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - MODULE\_6EDL7151 (gate driver)

## Schematics



**Figure 9** REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - MODULE\_INVERTER

**MODULE\_3V3\_ORING.SchDoc**

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**Figure 10** REF\_48V\_2X1KW\_ASFOC\_PWR\_Si - MODULE\_3V3\_ORING

Schematics

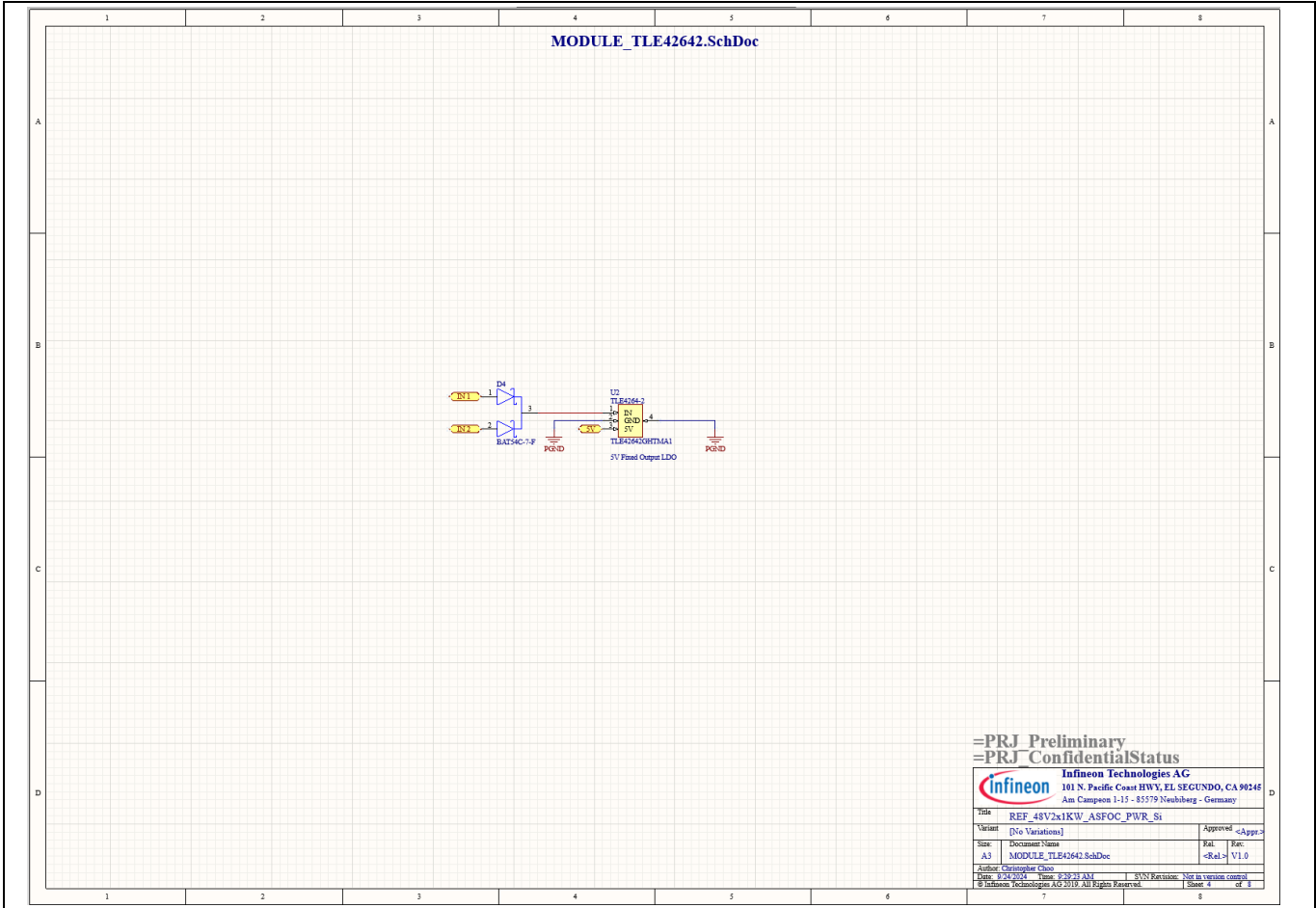


Figure 11 REF\_48V\_2X1KW\_ASFOC\_PWR\_Si – MODULE\_5V\_ORING

## Schematics

### 4.2 Power board layout

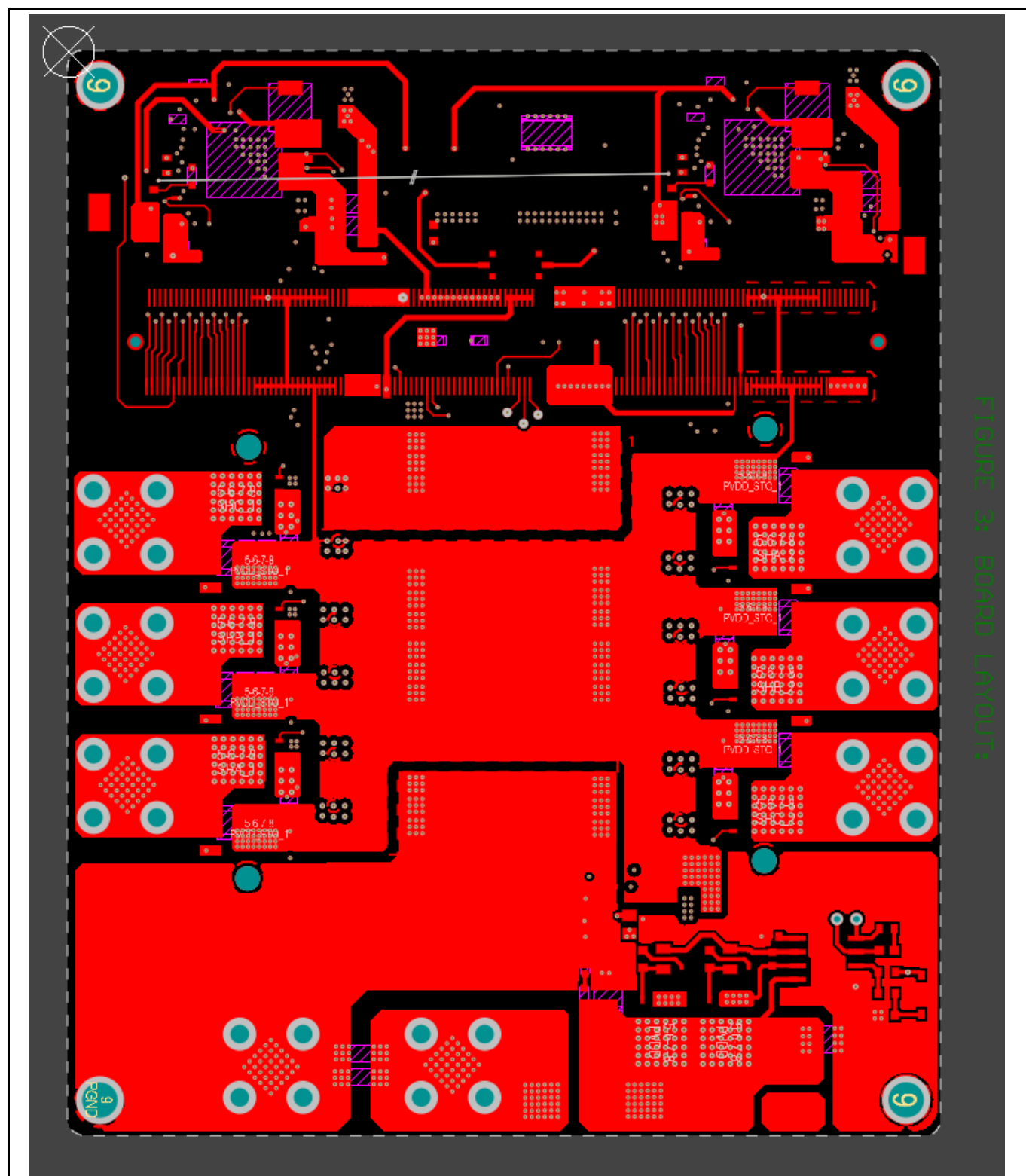


Figure 12 L1: Top layer

## Schematics

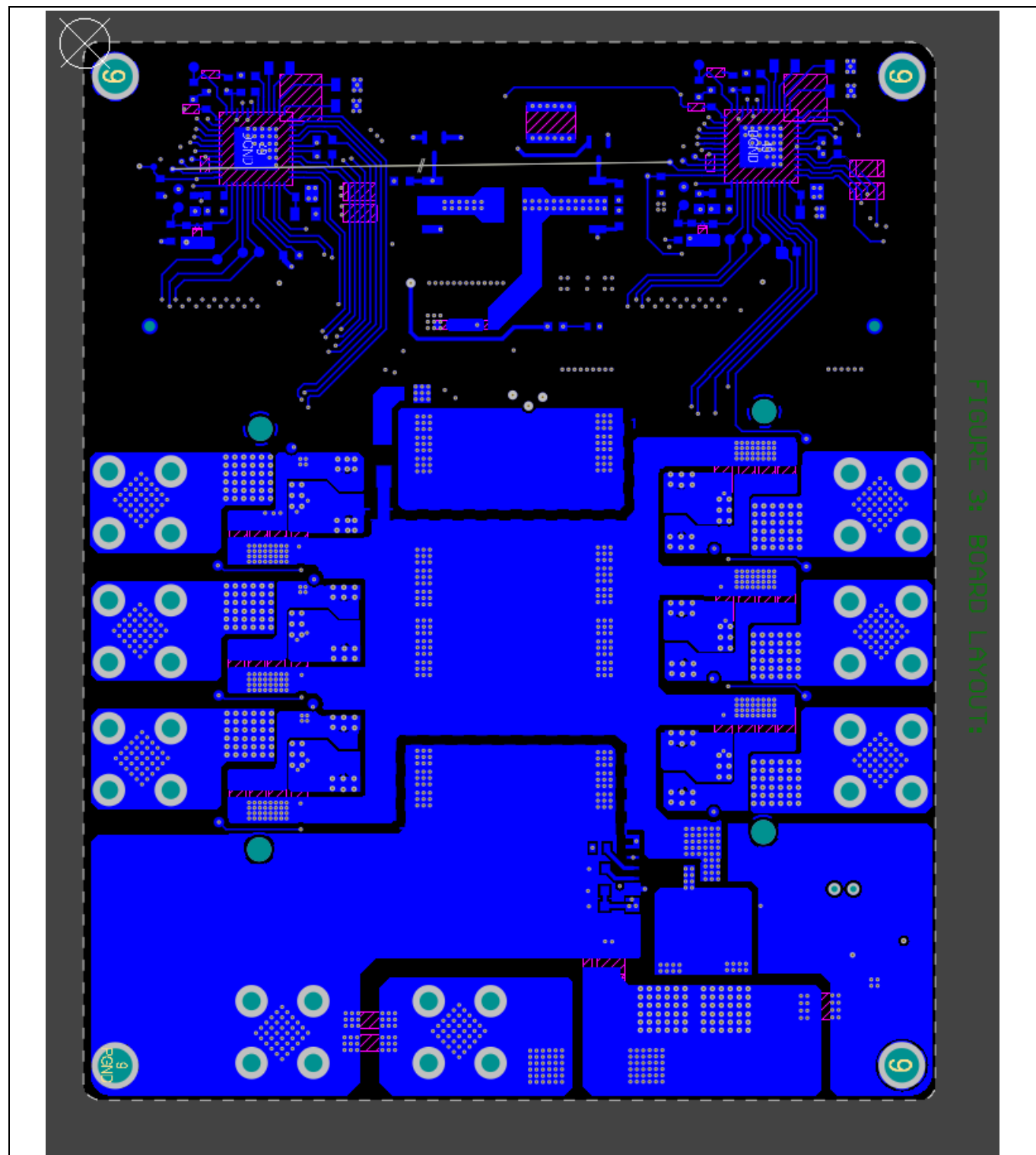


Figure 13 L4: Bottom layer



## Schematics

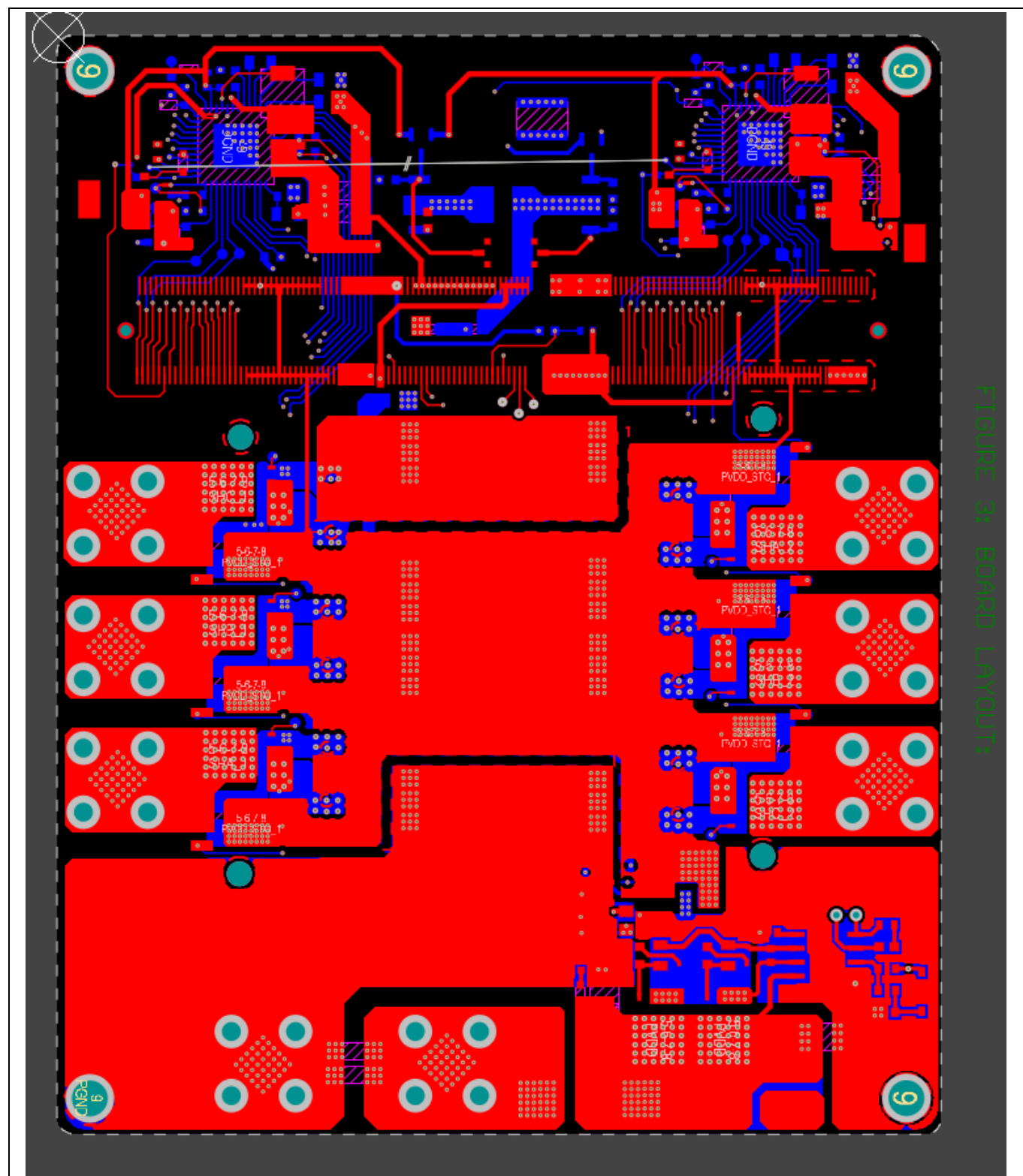


Figure 14 L1 over L4: Top overlaying bottom layer

## Schematics

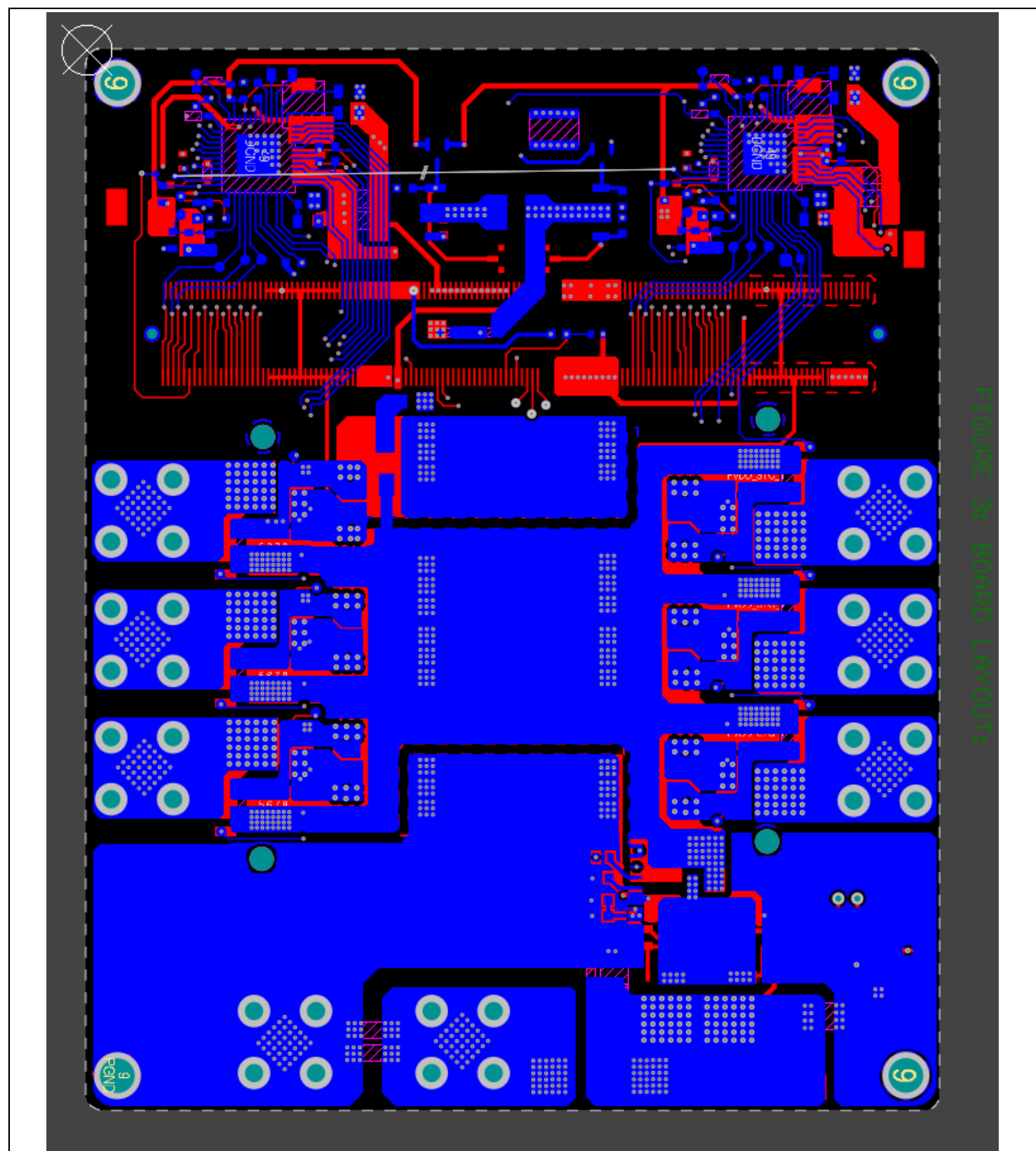
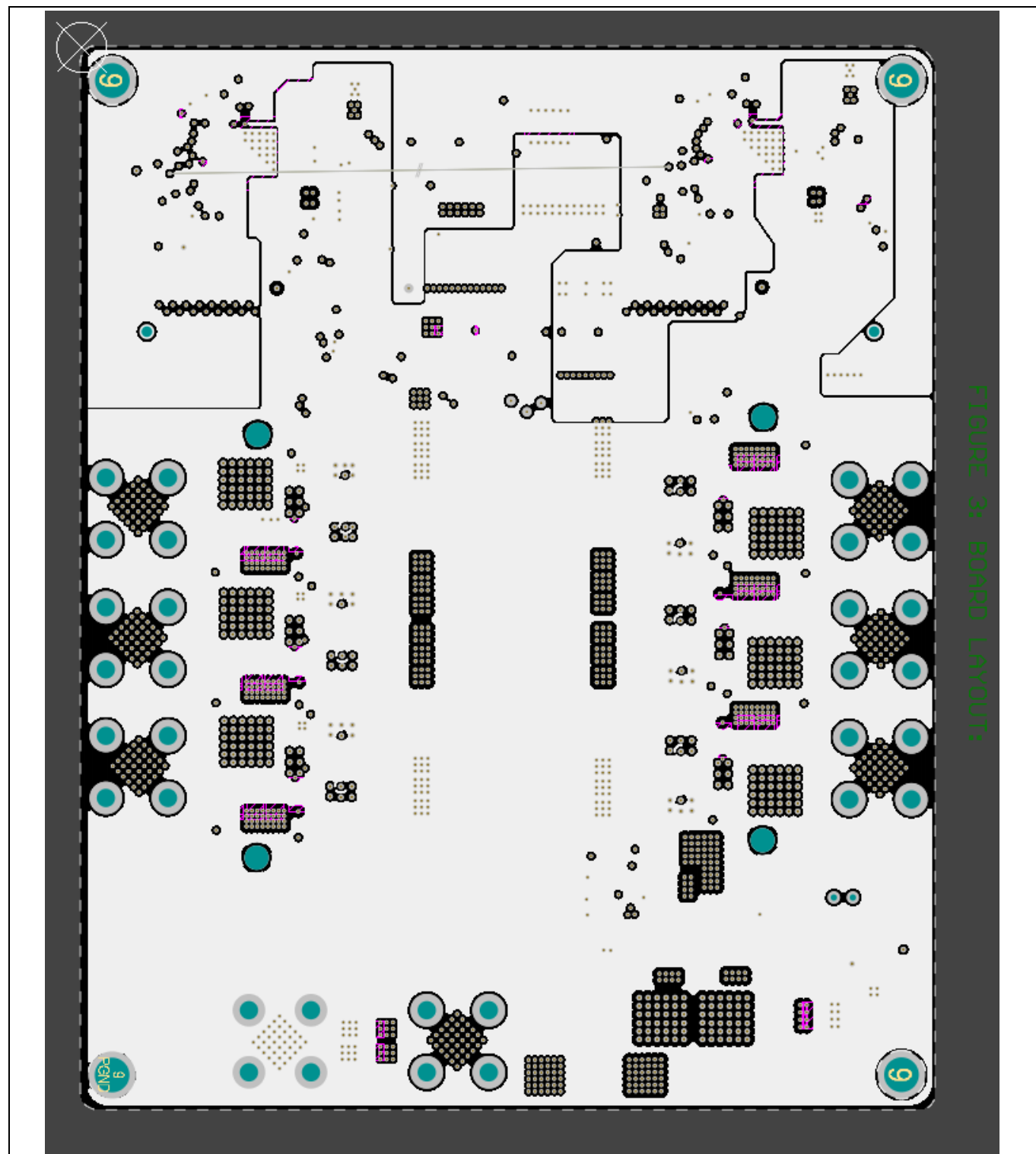


Figure 15 L4 over L1: Bottom overlaying top layer

## Schematics



**Figure 16** L2: Mid layer, ground plane: signal ground (upper) isolated with power ground (lower), connected with the OR resistor

## Schematics

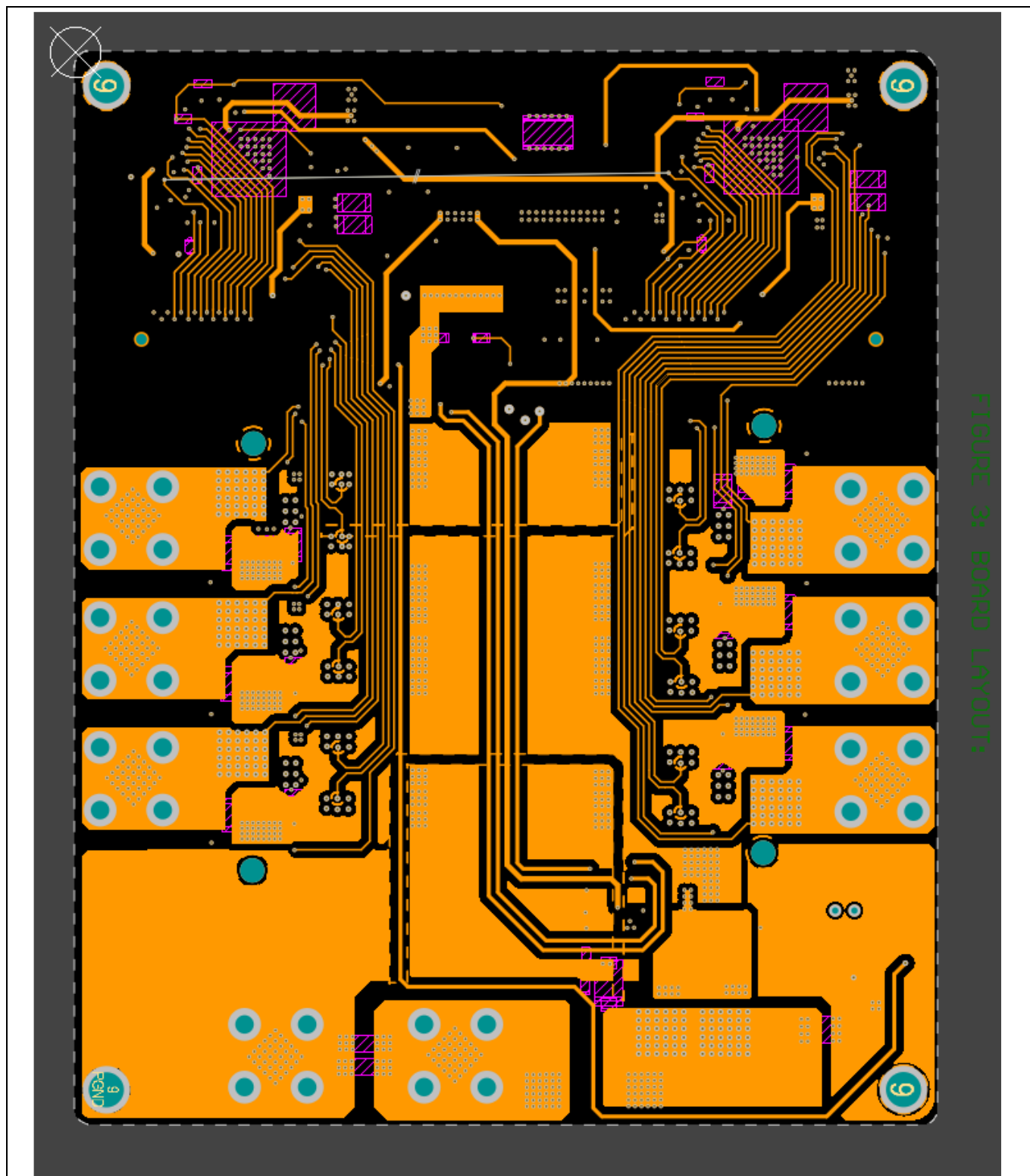


Figure 17 L3: Mid-layer, additional polygons, and signal routing

## Schematics

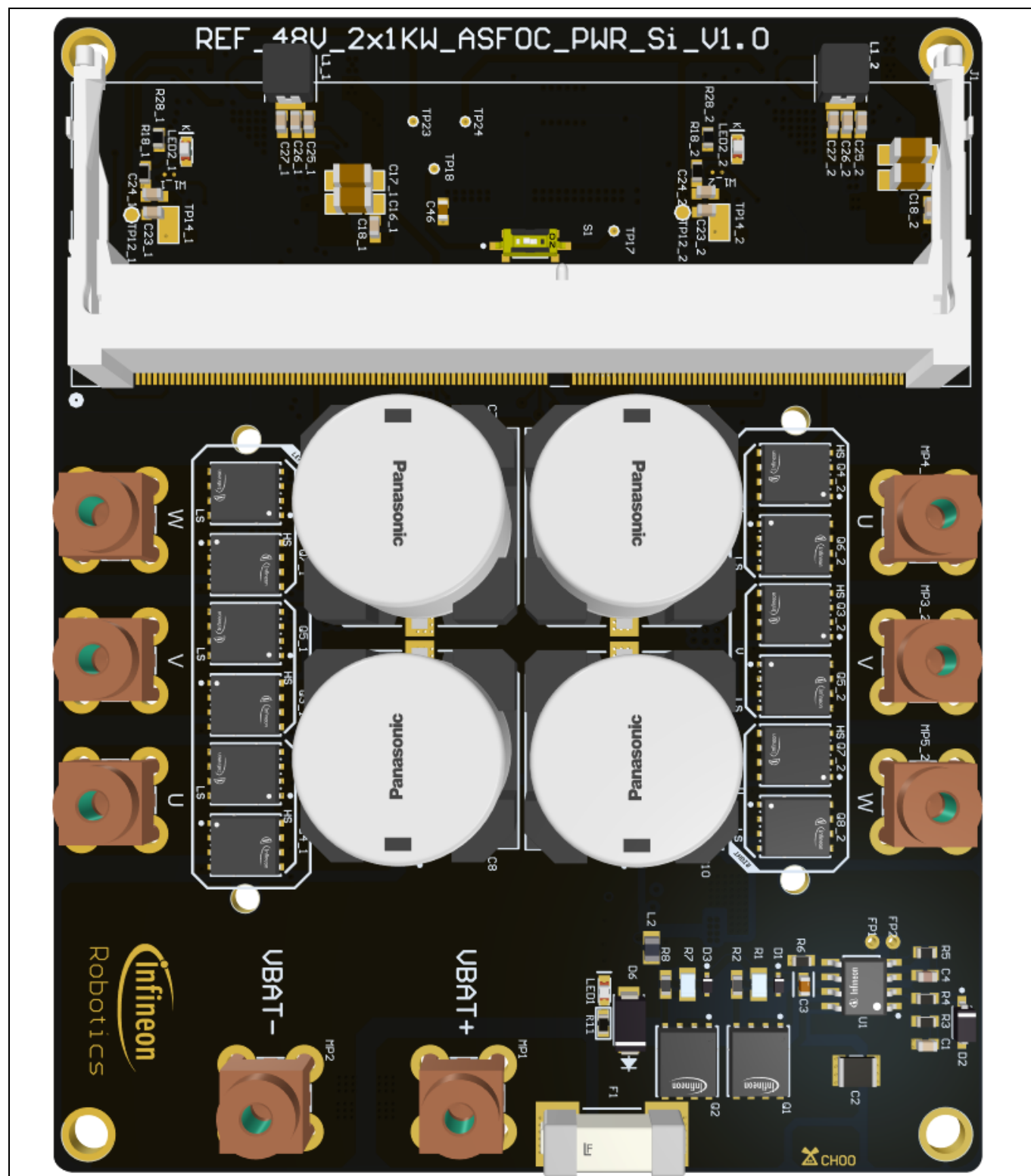
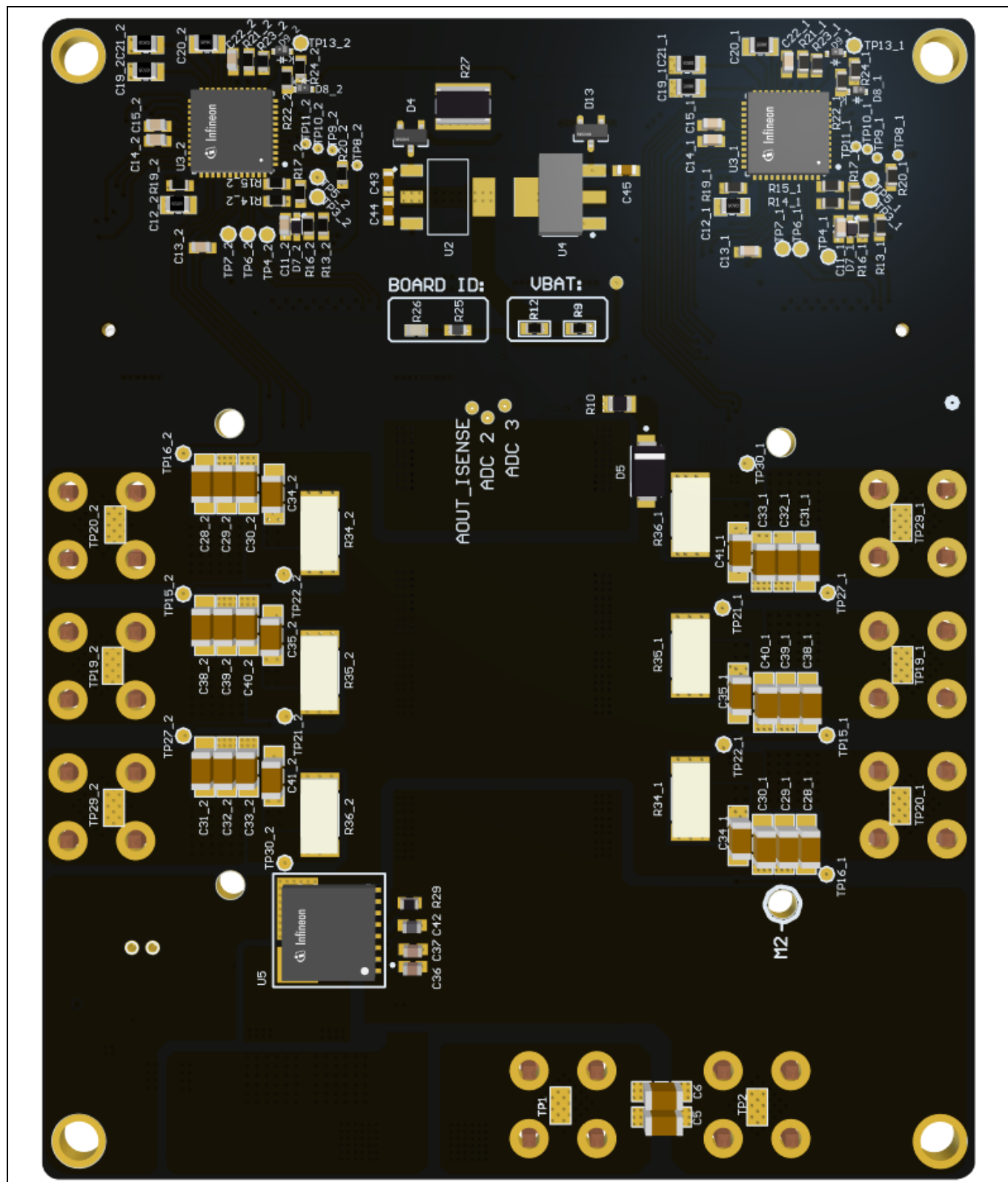


Figure 18 3D view of the top



## Schematics



**Figure 19** 3D view of the bottom

Schematics

4.3 Control card schematics

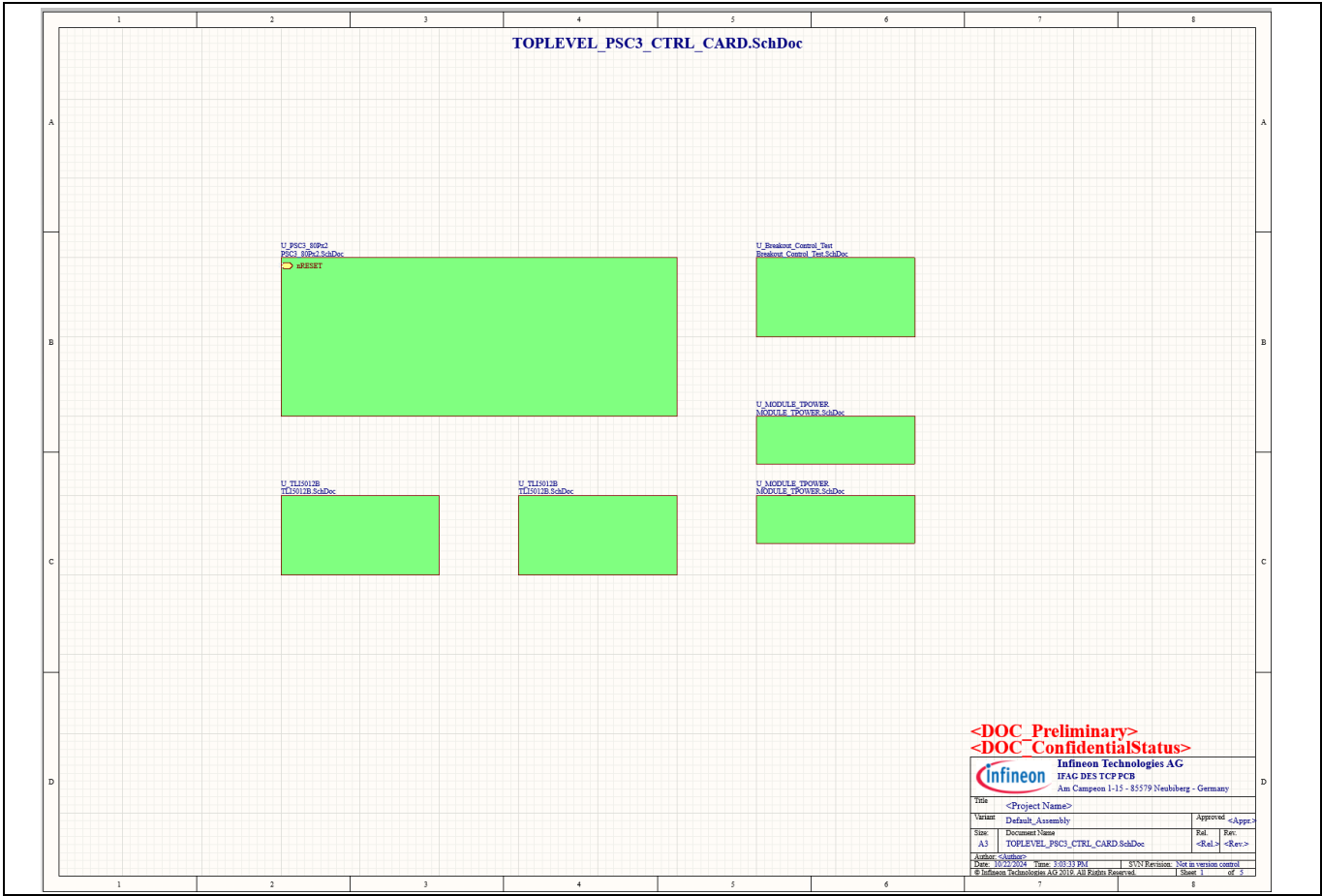


Figure 20 REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3\_1x80P – TOPLEVEL

## Schematics

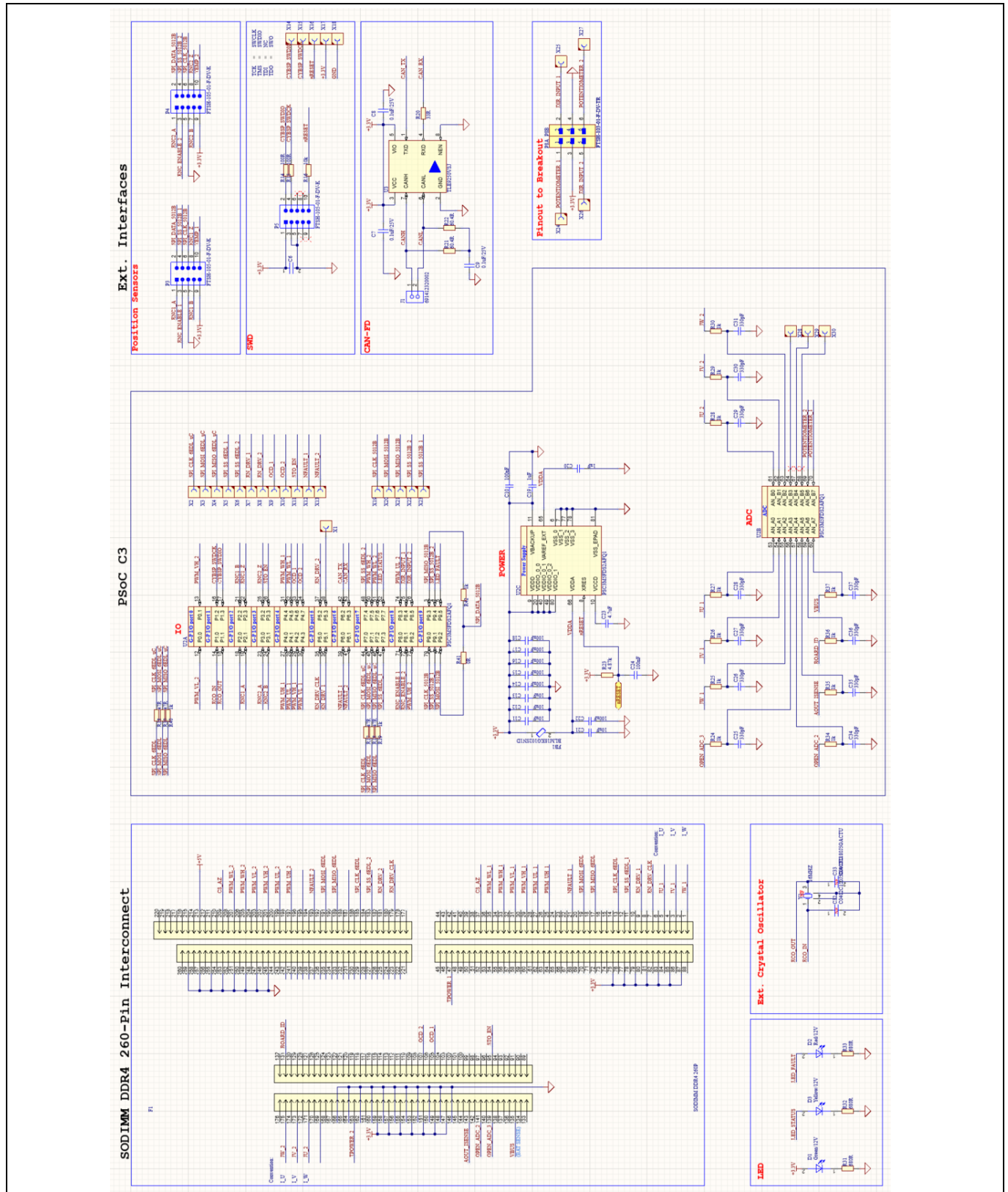


Figure 21 REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3\_1x80P - CONTROL CARD



[illegible]

**Figure 22** REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3\_1x80P - TLI5012B ANGLE SENSE

**Breakout\_Control\_Test.SchDoc**

**SPEED/POS CTRL Breakout**

The schematic diagram illustrates the SPEED/POS CTRL Breakout circuit. It features a FT232RL-01 F-DV-TR module connected to a breakout board. The breakout board has two sections, each with a 3.3V supply, a 10k resistor, a 10nF capacitor, and a switch (SW1, SW2) connected to a CL-SB-12B-02T component. The diagram is labeled with components like POT1, POT2, R4, R5, R7, R8, R10, R11, C3, and SW1, SW2.

**<DOC Preliminary>**  
**<DOC Confidential>**  
**Status**  
  
 Infineon Technologies AG  
 IFAG DES TCF PCB  
 Am Campeon 1-15 - 85579 Neuburg - Germany

Title		<Project Name>	
Version	Default_Assembly	Approved	<Appr>
Size	Document Name	Edi.	Rev.
A3	Breakout_Control_Test.SchDoc	<Edi>	<Rev>
Author: _____ Date: 10/22/2024 Time: 1:04:11 PM © Infineon Technologies AG 2019. All Rights Reserved.			
		Sheet 4	of 4

**Figure 23** REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3\_1x80P – breakout controller

Schematics

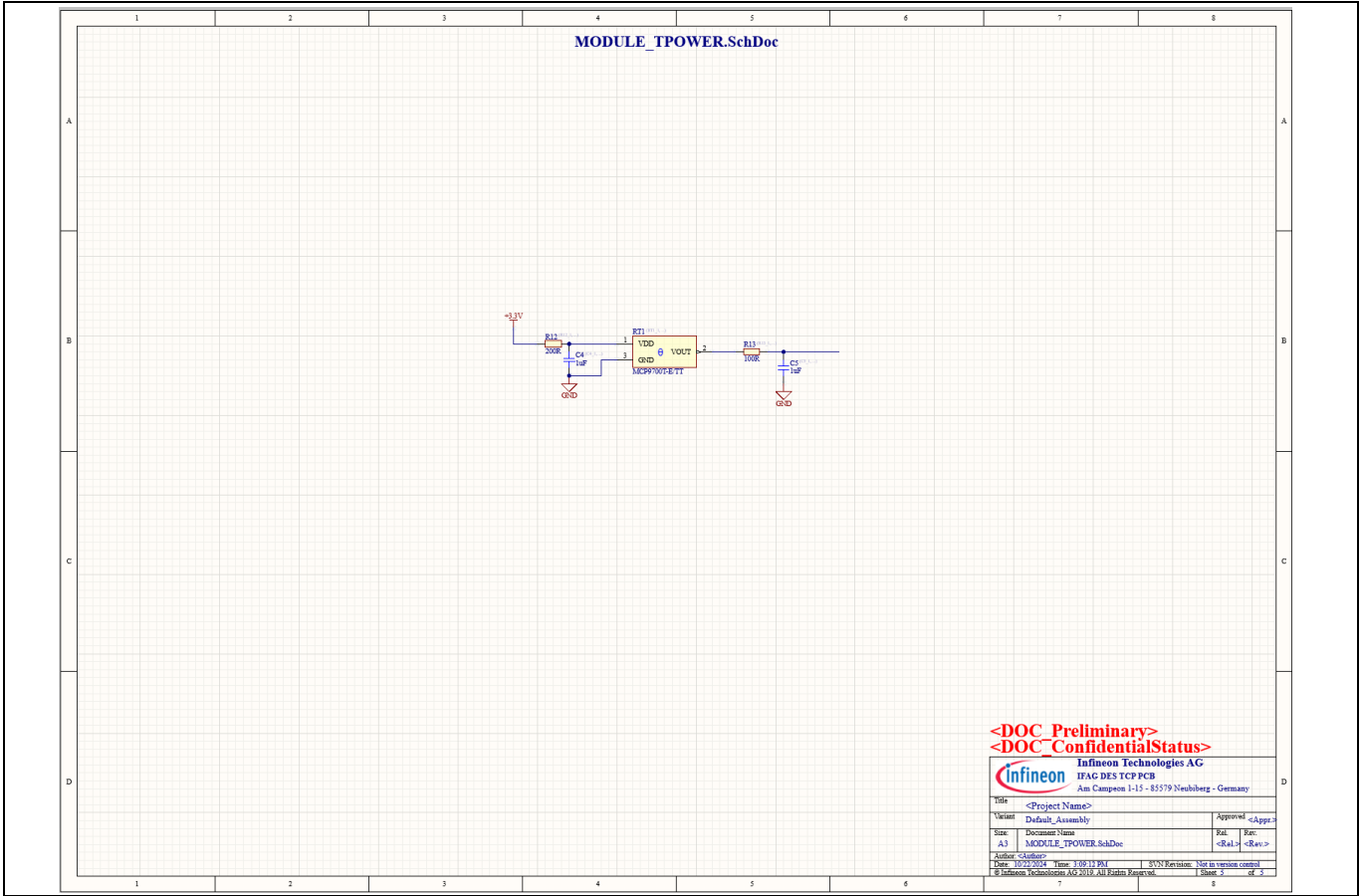
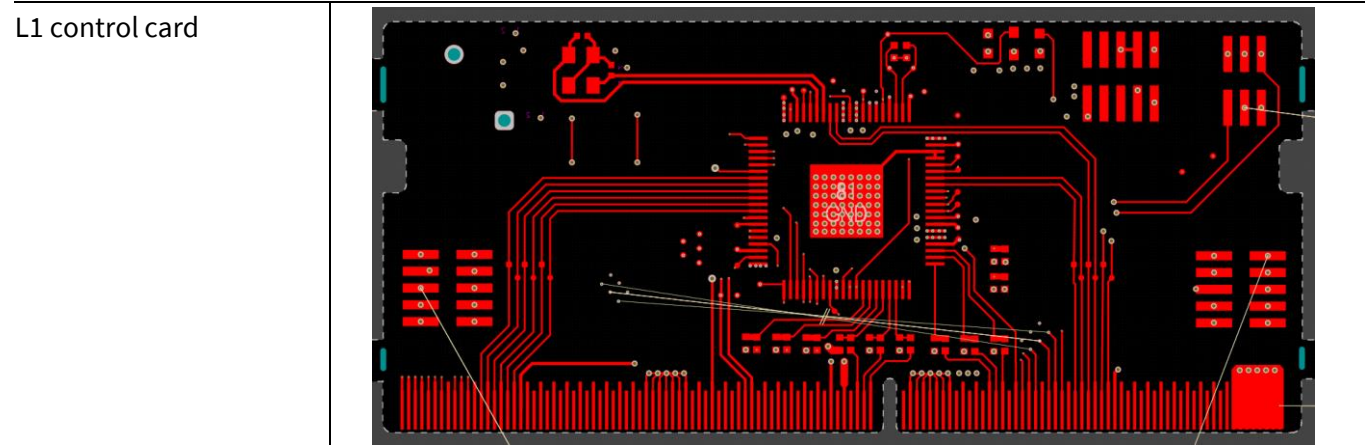


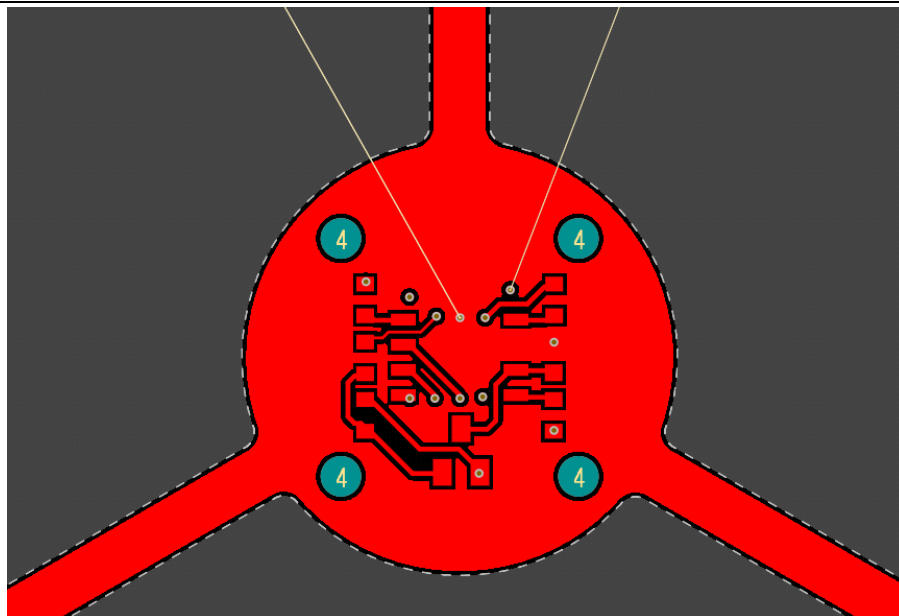
Figure 24 REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3\_1x80P - TEMP SENSE

4.4 Control card layout

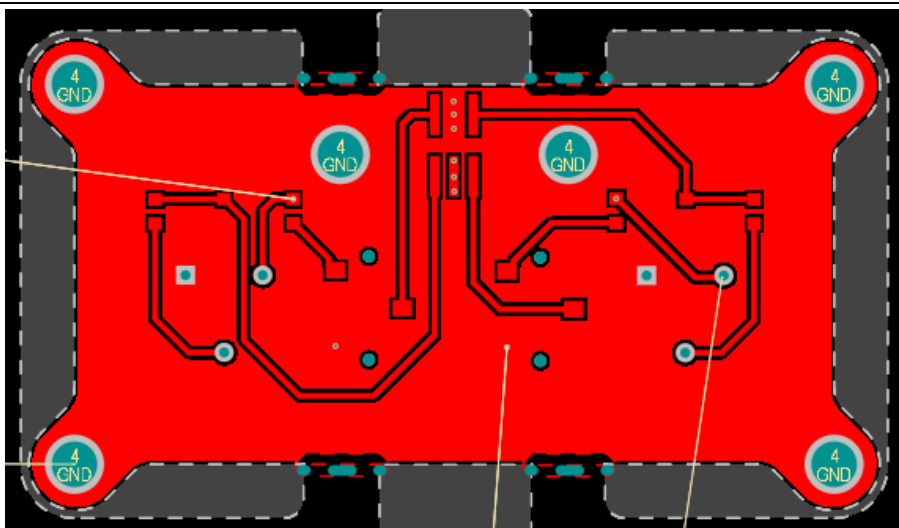


## Schematics

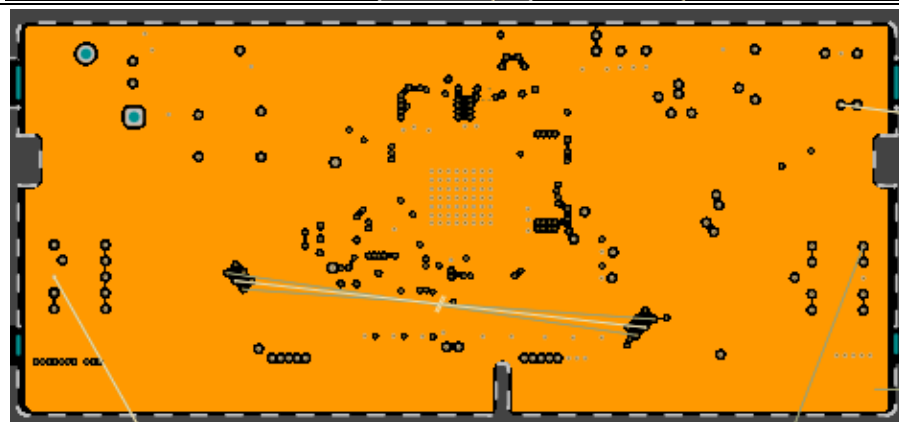
L1 angle sensor



L1 breakout potentiometer board

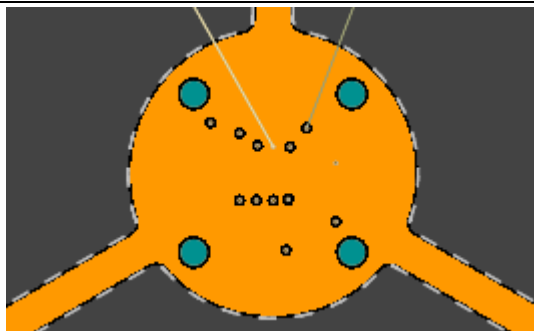


L2 control card

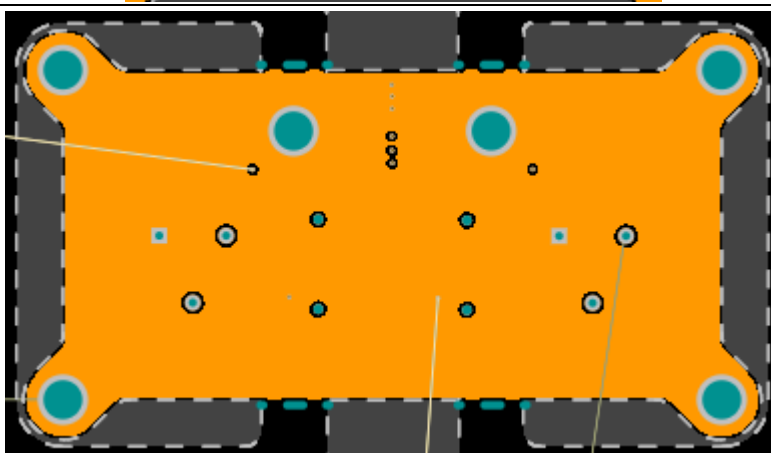


## Schematics

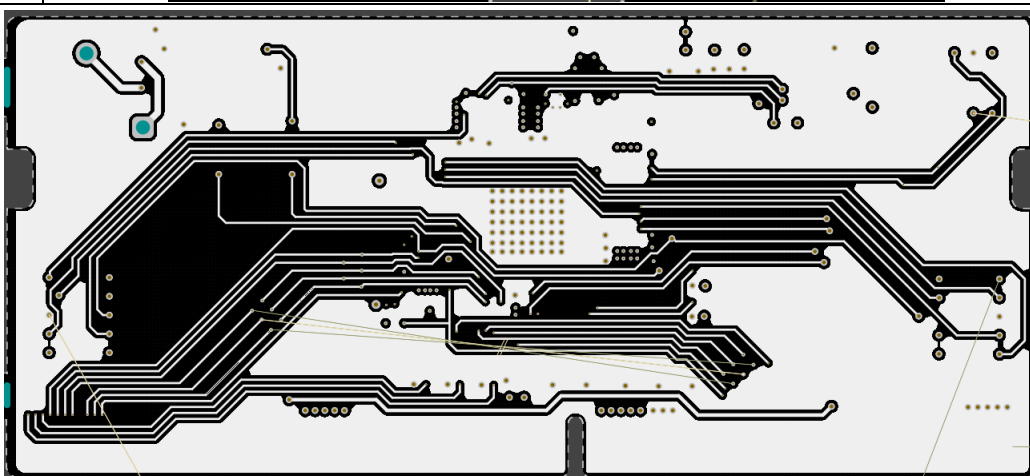
L2 angle sensor



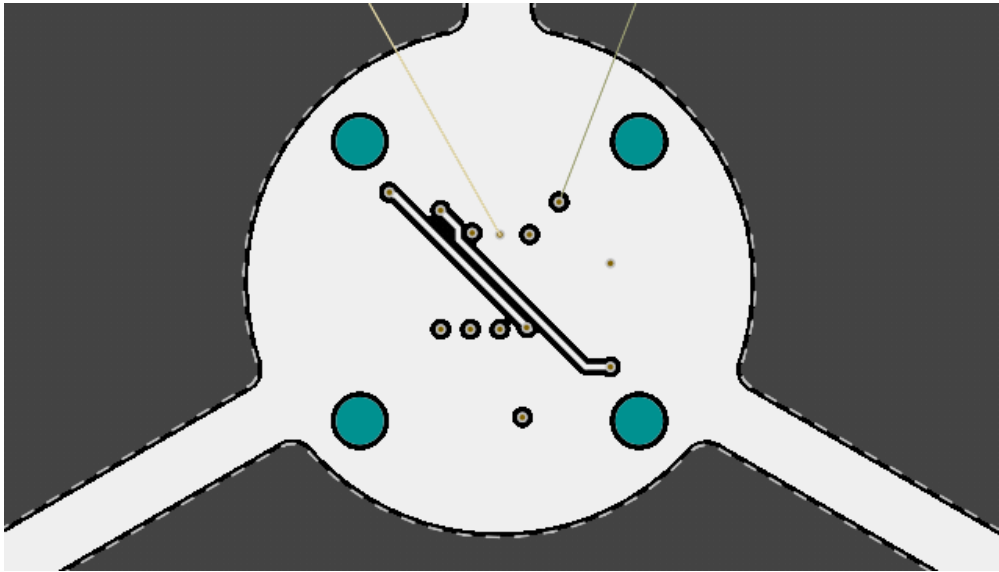
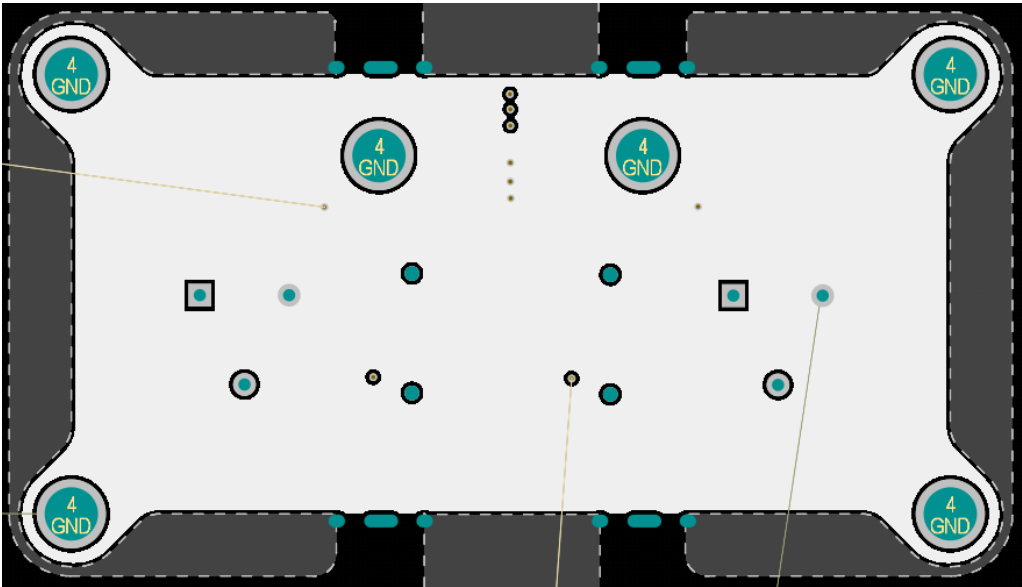
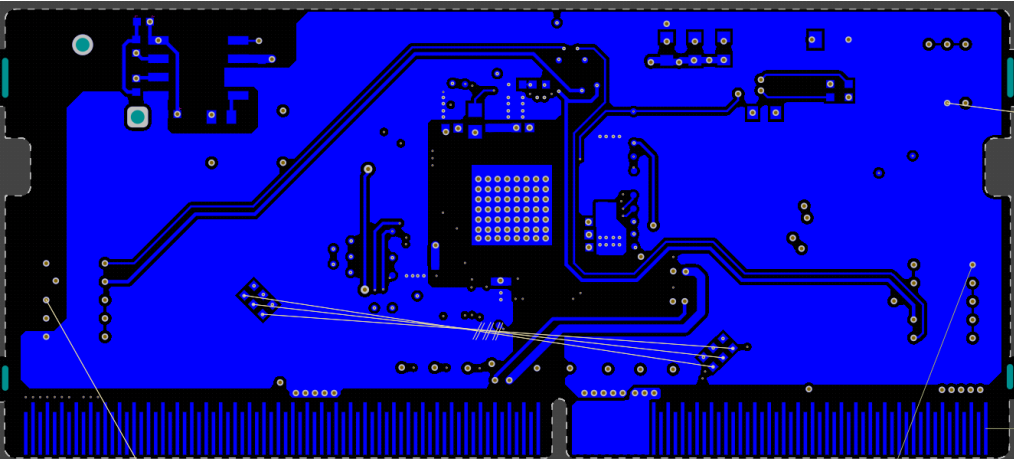
L2 breakout potentiometer board



L3 control card

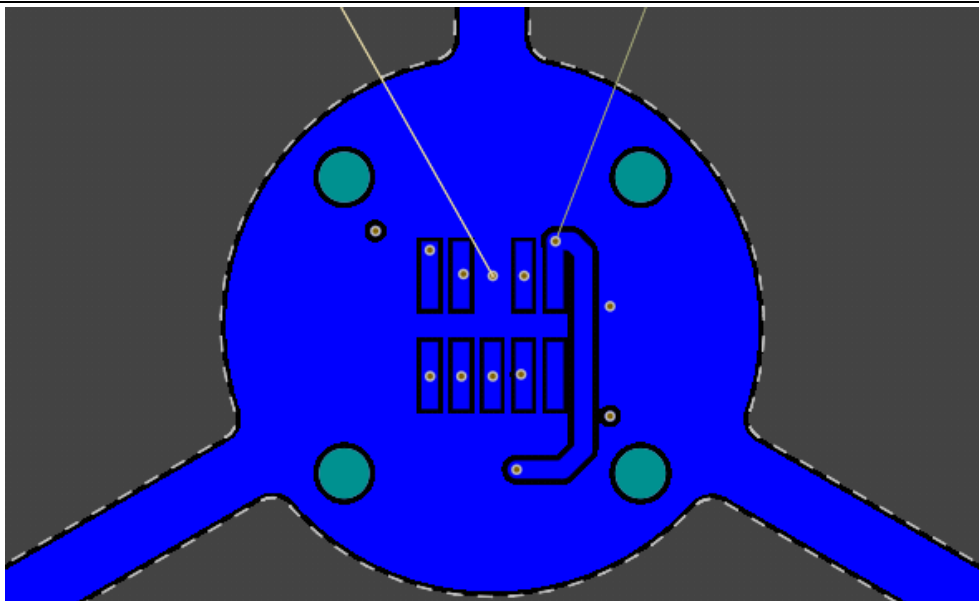


Schematics

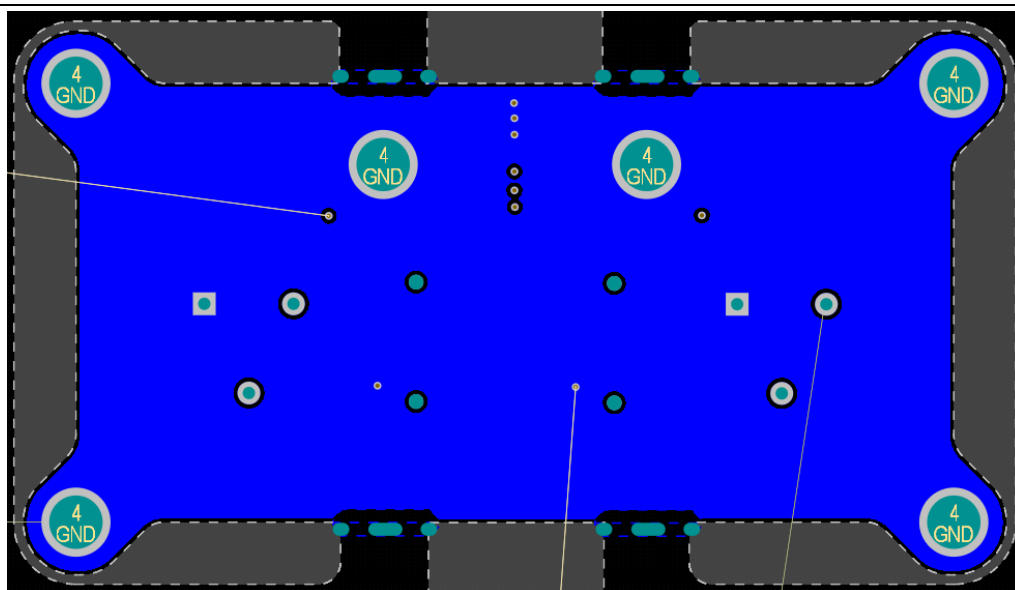
L3 angle sensor	
L3 breakout potentiometer board	
L4 control card	

## Schematics

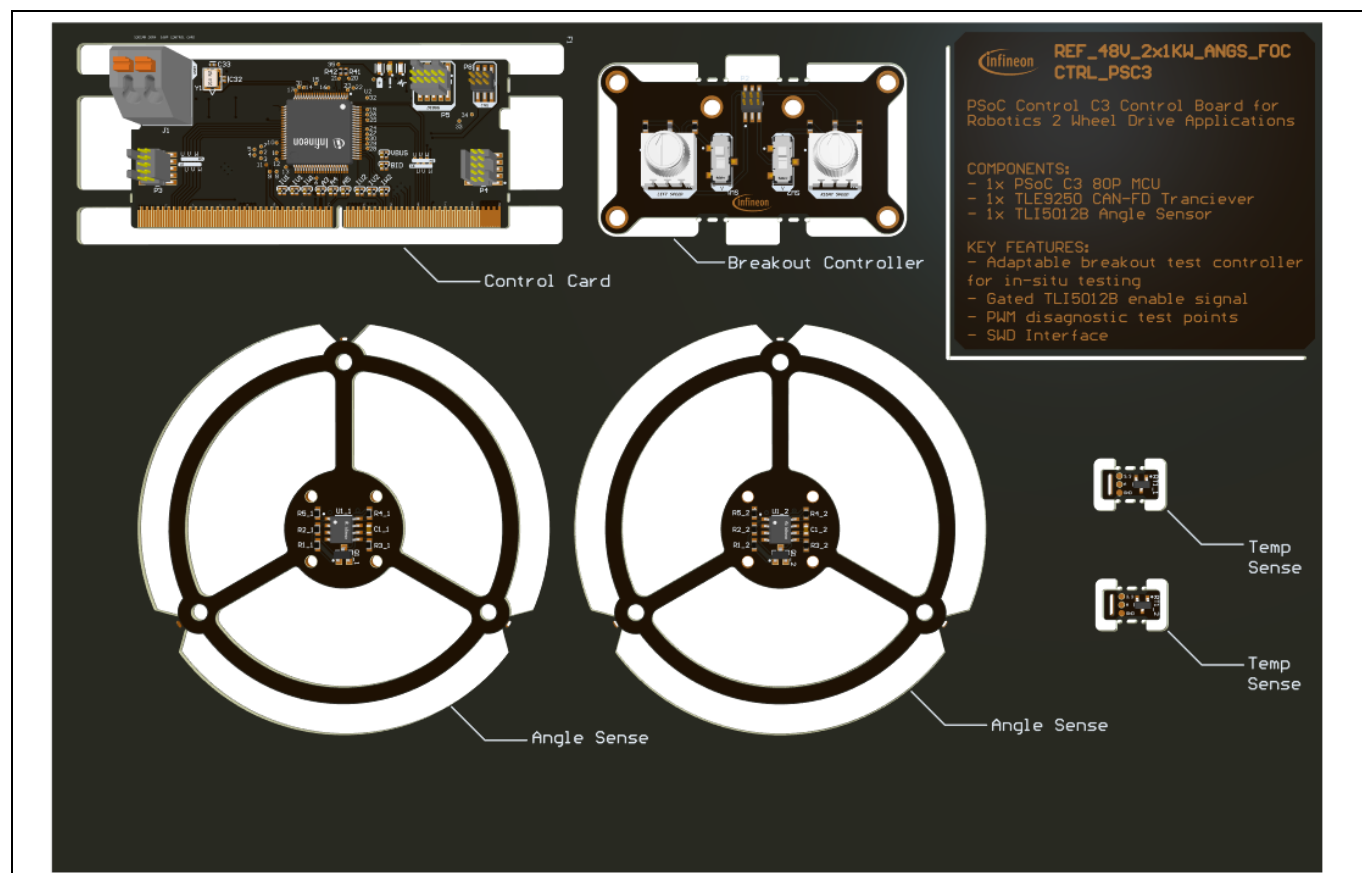
L4 angle sensor



L4 breakout potentiometer board



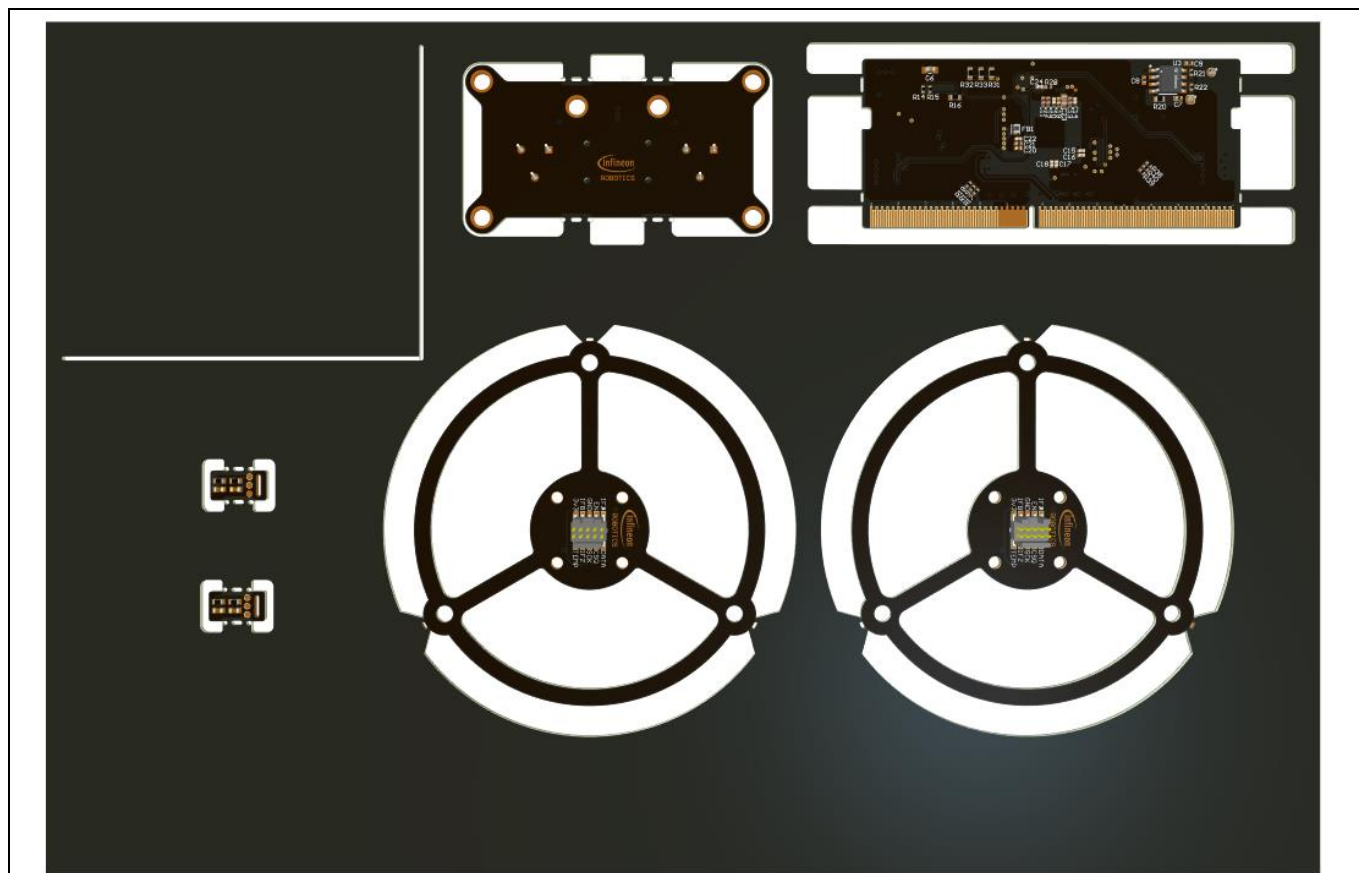
## Schematics



**Figure 25** Top of the control card panel



## Schematics



**Figure 26** Bottom of the control card panel

## Bill of materials

### 5 Bill of materials

#### 5.1 REF\_48V\_2X1KW\_ASFOC\_PWR\_Si: Power board

**Table 2 BOM for REF\_48V\_2X1KW\_ASFOC\_PWR\_Si: Power Board**

Item	Qt	Description	Designator	Part Number	Manufacturer
1	1	0.1 uF, 50 V, 10%, 0603, X7R	C1	06035C104K4Z2A	AVX
2	1	10 uF, 100 V, 10%, 1210, X7S	C2	GRM32EC72A106K E05L	Murata
3	2	0.022 uF, 100 V, 10%, 0603, X7R	C3, C4	GCM188R72A223K A37J	Murata
4	20	2.2 uF, 100 V, 10%, 1206	C5, C6, C28_1, C28_2, C29_1, C29_2, C31_1, C31_2, C32_1, C32_2, C34_1, C34_2, C35_1, C35_2, C38_1, C38_2, C39_1, C39_2, C41_1, C41_2	C3216X7S2A225K1 60AB	TDK Corporation
5	4	470 uF, 63 V, 20%, SMD	C7, C8, C9, C10	EEEFK1J471AM	Panasonic
6	4	0.1 uF, 25V, 10%, 0603	C11_1, C11_2, C26_1, C26_2	CGA3E2X8R1E104 M080AA	TDK Corporation
7	2	1 uF, 100 V, 10%, 0805	C12_1, C12_2	GCM21BC72A105K E36L	Murata
8	6	100 pF, 25 V, 10%, 0603	C13_1, C13_2, C14_1, C14_2, C15_1, C15_2	C0603C101K3GAC7 867	KEMET
9	10	4.7 uF, 100 V, 10%, 1206	C16_1, C16_2, C17_1, C17_2, C30_1, C30_2, C33_1, C33_2, C40_1, C40_2	GRM31CC72A475K E11L	Murata
10	2	0.1 uF, 100 V, 20%, 0603	C18_1, C18_2	CC0603KRX7R0BB 104	Yageo
11	4	2.2 uF, 25 V, 10%, 0805	C19_1, C19_2, C21_1, C21_2	CL21A225KAFNNN G	Samsung
12	2	0.22 uF, 50 V, ±10%, 0805	C20_1, C20_2	C0805C224K5RACA UTO	KEMET
13	2	0.22 uF, 10%, 50 V, 0603	C22_1, C22_2	CL10A224KB8NNN C	Samsung
14	2	0.1 uF, 10 V, 10%, 0603	C23_1, C23_2	C0603C104K8PAC7 867	KEMET

## Bill of materials

Item	Qt	Description	Designator	Part Number	Manufacturer
15	2	10 uF, 10 V, 10%, 0603	C24_1, C24_2	CL10A106KP8NNN C	Samsung
16	4	22 uF, 16 V, 20%, 0603	C25_1, C25_2, C27_1, C27_2	CL10A226MO7JZN C	Samsung
17	1	10 uF, 10 V, 10%, 0603, X7R	C36	GRM188Z71A106K A73D	Murata
18	2	100 nF, 100 V, 10%, 0603, X8L	C37, C42	CL10E104KC8VPN C	Samsung
19	4	1 uF, 50 V, 10%, 0603, X5R	C43, C44, C45, C46	CL10A105KB8NNN C	Samsung
20	2	80 V, 125 MA, SOD523	D1, D3	1N4148WT-7	Diodes Incorporated
21	1	100 V, 300 MA, SOD123	D2	1N4148W-13-F	Diodes Incorporated
22	2	30 V, 200 MA, SOT23	D4, D13	BAT54C-7-F	Diodes Incorporated
23	1	100 V, 2 A, SMA	D5	STPS2H100AY	STMicroelectronics
24	1	TVS DIODE 40 VWM 64.5 VC SMA	D6	SMAJE40A	Eaton - Electronics Division
25	2	Zener, 5.1 V, 500 mW, SOD-523 SMD	D7_1, D7_2	SZMM5Z5V1T1G	On-Semi
26	4	DIODE SCHOTTKY 30 V 500 MA SC79-2	D8_1, D8_2, D9_1, D9_2	BAS3005A02VH632 7XTSA1	Infineon Technologies
27	1	30 A, 125 VAC, 72 VDC	F1	0456030.ER	Littelfuse Inc.
28	1	DDR4 SODIMM 260P 9.2H STD	J1	2309413-1	TE Connectivity AMP Connectors
29	2	FIXED IND 22 µH 1.2 A 500 MOhm SMD	L1_1, L1_2	SRP4020TA-220M	Bourns
30	1	FIXED IND 2.2 µH 150 MA 364 MOhm SM	L2	LQM21FN2R2N00	Murata
31	3	LED RED CLEAR	LED1, LED2_1, LED2_2	LTST-C190KRKT	Lite-On Inc, Lite-On Inc.
32	8	TERM REDCUBE M3 4PIN PCB	MP1, MP2, MP3_1, MP3_2, MP4_1, MP4_2, MP5_1, MP5_2	74650173R	Würth Elektronik
33	2	OptiMOS™ 5 LinearFET 80 V	Q1, Q2	ISC025N08NM5LF2	Infineon Technologies
34	12	MOSFET N-Ch 80 V 49 A TDSO8-8	Q3_1, Q3_2, Q4_1, Q4_2, Q5_1, Q5_2, Q6_1, Q6_2, Q7_1, Q7_2, Q8_1, Q8_2	ISC031N08NM6	Infineon Technologies

## REF\_48V\_2X1KW\_ASFOC dual-motor drive for robotics applications



### Bill of materials

Item	Qt	Description	Designator	Part Number	Manufacturer
35	2	100 KOhm, 0.125 W, 1% , 0805	R1, R7	CRG0805F100K	TE Connectivity Passive Product
36	2	1 Ohm, 0.1 W, 1%, 0603	R2, R8	ERJ-3RQF1R0V	Panasonic
37	2	10 KOhm, 0.1 W, 1% , 0603	R3, R4	CRCW060310K0FK EBC	Vishay
38	1	22 Ohm, 0.1W, 1%, 0603	R5	CRCW060322R0FK EAC	Vishay Dale
39	1	182 K, 0.1 W, 1%, 0603	R6	RC0603FR-07182KL	Yageo
40	1	162 K, 0.1W, 1%, 0603	R9	CRCW0603162KFK EA	Vishay
41	1	10 Ohm, 0.125W, 1%, 0805	R10	CRCW080510R0FK EA	Vishay Dale
42	1	5.6 K, 0.1 W, 1%, 0603	R11	RMCF0603FT5K60	Stackpole
43	1	7.87 K, 0.1 W, 1%, 0603	R12	RC0603FR-077K87L	Yageo
44	2	100 K, 0.1 W, 1% , 0603	R13_1, R13_2	RC0603FR-07100KL	Yageo
45	4	3.3 K, 0.1 W, 1% , 0603	R14_1, R14_2, R24_1, R24_2	RC0603FR-073K3L	Yageo
46	2	1.8 K, 0.1 W, 0.1%, 0603	R15_1, R15_2	RT0603BRE071K8L	Yageo
47	2	22 K, 0.1 W, 1%, 0603	R16_1, R16_2	RC0603FR-1022KL	Yageo
48	8	5.1 K, 0.1 W, 5%, 0603	R17_1, R17_2, R18_1, R18_2, R20_1, R20_2, R21_1, R21_2	ERJ-3GEYJ512V	Panasonic
49	2	2 K, 0.1 W, 1%, 0603	R19_1, R19_2	RMCF0603FT2K00	Stackpole Electronics, Inc
50	2	3 K, 0.1 W, 1%, 0603	R22_1, R22_2	ERJ-3EKF3001V	Panasonic
51	2	909 Ohm, 0.1W, 1%, 0603	R23_1, R23_2	RC0603FR-07909RL	Yageo
52	1	14.7 KOhm, 0.1W, 1% , 0603	R25	RC0603FR-0714K7L	Yageo
53	1	32.4K Ohm , 0.1W, 1% , 0603	R26	CRCW060332K4FK EA	Vishay
54	1	0 OHM, JUMPER, 1W , 1218	R27	CRCW12180000ZS TK	Vishay
55	2	1 KOhm, 0.1W, 1%, 0603	R28_1, R28_2	ERJ-3EKF1001V	Panasonic

## Bill of materials

Item	Qt	Description	Designator	Part Number	Manufacturer
56	1	220 Ohm, 0.21W, 0.1%, 0603	R29	TNPW0603220RBY EN	Vishay
57	6	0.02 Ohm, 2W, 1% , 2512	R34_1, R34_2, R35_1, R35_2, R36_1, R36_2	MCS3264R020FER	Ohmite
58	1	High-side gate driver, 125 V, 5x6 mm	U1	1EDL8011	Infineon Technologies
59	1	IC REG LINEAR 5 V 150 MA SOT223-4	U2	TLE42642GHTMA1	Infineon Technologies
60	2	Gate driver IC for 3 phase BLDC or PMSM motor drive application	U3_1, U3_2	6EDL7151	Infineon Technologies
61	1	IC REG LINEAR 3.3 V 800 MA SOT223	U4	LD1117S33TR	STMicroelectronics
62	1	SENSOR CURRENT HALL 50 A 8TISON	U5	TLI4971-A050T5-E0001	Infineon Technologies
63	1	SWITCH SLIDE DIP SPST 0.1 A 6 V	S1	CVS-01TB	Nidec Components Corporation

## 5.2 REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3: Control card

**Table 3 BOM for REF\_48V\_2X1KW\_ASFOC\_CTRL\_PSC3: Control Card**

Item	Qt	Description	Designator	Part Number	Manufacturer
1	6	1 uF, 10 V, 10%, 0603, X5R	C1_1, C1_2, C4_1, C4_2, C5_1, C5_2	GRM188R61A105KA61D	MuRata
2	2	10 nF, 50 V, 10%, 0603, X7R	C2, C3	C0603C103K5RECAUTO	Kemet
3	1	0.1 uF, 50 V, 10%, 0603, X7R	C6	CGA3E2X7R1H104K080AA	TDK
4	3	0.1 uF, 25 V, 10%, 0402, X7R	C7, C8, C9	C1005X7R1E104K050BB	TDK
5	8	100 nF, 50 V, 10%, 0402, X8L	C10, C14, C15, C16, C17, C18, C22, C24	GCM155L8EH104KE07D	MuRata
6	4	10 uF, 10 V, 20%, 0402, X5R	C11, C12, C13, C21	KGM05CR51A106MH	Kyocera
7	2	1 uF, 25 V, 10%, 0402, X6S	C19, C20	GRM155C81E105KE11D	MuRata
8	1	4.7 uF, 35 V, 10%, 0603, X5R	C23	GRT188R6YA475KE13D	MuRata

## Bill of materials

Item	Qt	Description	Designator	Part Number	Manufacturer
9	11	330 pF, 50 V, 5% , 0402, COG	C25, C26, C27, C28, C29, C30, C31, C34, C35, C36, C37	GRM1555C1H331JA01D	MuRata
10	2	18 pF, 50 V, 5%, 0402, COG	C32, C33	C0402C180J5GACTU	Kemet
11	1	LED GREEN DIFFUSED 0603 SMD	D1	LGQ396-PS-35	ams-OSRAM USA INC.
12	1	LED RED DIFFUSED 1608 SMD	D2	SML-E12UWT86	Rohm Semiconductor
13	1	LED YELLOW DIFFUSED SMD	D3	Q65111A3365	ams-OSRAM USA INC.
14	1	FERRITE BEAD 1 KOhm 0603 1LN	FB1	BLM18KG102SN1D	MuRata
15	1	TERM BLOCK 2POS 45DEG 3.81 MM PCB	J1	691412320002	Würth Elektronik
16	5	CONN HEADER SMD 10POS 1.27 MM	P1_1, P1_2, P3, P4, P5	FTSH-105-01-F-DV-K	Samtec
17	2	CONN HEADER SMD 6POS 1.27 MM	P2A, P8A	FTSH-103-01-F-DV-TR	Samtec
18	2	MOSFET P-CH 25 V 460 MA SOT23	Q1_1, Q1_2	FDV304P	onsemi
19	2	100 K, 0.1 W, 1%, 0603	R1_1, R1_2	RC0603FR-07100KL	Yageo
20	10	100 R, 0.1 W, 1%, 0603	R2_1, R2_2, R3_1, R3_2, R4_1, R4_2, R5_1, R5_2, R13_1, R13_2	RC0603FR-07100RL	Yageo
21	4	1 K, 0.125 W, 1%, 0603	R6, R7, R10, R11	RK73H1JTTD1001F	KOA Speer Electronics Inc.
22	2	10 K, 0.5 W, 10%, THT	R8, R9	3386F-1-103TLF	Bourns
23	2	200 R, 0.1 W, 0.1%, 0603	R12_1, R12_2	RT0603BRD07200RL	Yageo
24	2	100 R, 0.063 W, 1%, 0402	R14, R15	RC0402FR-07100RL	Yageo
25	1	10 K, 0.1 W, 1% , 0603	R16	RC0603FR-0710KL	Yageo
26	4	47 R, 0.063 W, 1% , 0402	R17, R18, R38, R39	CRCW040247R0FKEDC	Vishay
27	14	1K, 0.063 W, 1%, 0402	R19, R24, R25, R26, R27, R28, R29, R30, R34,	CRCW04021K00FKED	Vishay

## Bill of materials

Item	Qt	Description	Designator	Part Number	Manufacturer
			R35, R36, R37, R40, R42		
28	1	33 R, 0.1 W, 1%, 0603	R20	CRCW060333R0FKEAC	Vishay
29	2	60.4 R, 0.063 W, 1%, 0402	R21, R22	CRCW040260R4FKED	Vishay
30	1	4.87 K, 0.063 W, 1%, 0402	R23	CRCW04024K87FKTD	Vishay
31	3	680R, 0.1 W, 1%, 0603	R31, R32, R33	AC0603FR-07680RL	Yageo
32	1	0 Ohm, 0.1 W, 0402	R41	ERJ2GE0R00X	Panasonic
33	2	SENSOR ANALOG, - 40C-125C ,SOT23-3	RT1_1, RT1_2	MCP9700T-E/TT	Microchip Technology
34	2	SWITCH SLIDE, SPDT, 200 MA, 12 V	SW1, SW2	CL-SB-12B-02T	Nidec Components Corporation
35	2	SENSOR ANGLE 360DEG SMD	U1_1, U1_2	TLI5012B E1000	Infineon Technologies
36	1	PSOC C3 Main line, Cortex-M33, 180 MHz, 64 kB SRAM, 256 KB Flash, E-LQFP-80	U2	PSC3M5FDS2AFQ1	Infineon Technologies
37	1	IC TRANSCEIVER 1/1 DSO-8	U3	TLE9250VSJXUMA1	Infineon Technologies
38	1	16 Mhz crystal oscillator	Y1	STDCQS1-16M	NDK

# REF\_48V\_2X1KW\_ASFOC dual-motor drive for robotics applications

## Hardware functional description

### 6 Hardware functional description

The main hardware elements of the evaluation system are:

- PSOC Control C3 MCU
- Two 6EDL7151 smart gate drivers
- 1EDL8011 high-side disconnect switch
- TLI4971 coreless current sensor

This combination of components facilitates high-frequency motor control while maintaining a high safety factor. The board is divided into two main sections:

- **Control card:** Carries the MCU, UART port, CAN terminals, position sensor connectors, and SWDIO
- **Power board:** Houses the two power stages, 48 V DC input, bulk capacitors, and the OCP battery disconnect switch

The modularity of this solution enables you to interchangeably use any configuration of the control card and power board based on your unique application needs.

#### 6.1 Key MCU Information: PSOC Control C3

Specific PN used in design: PSC3M5FDS2AFQ1

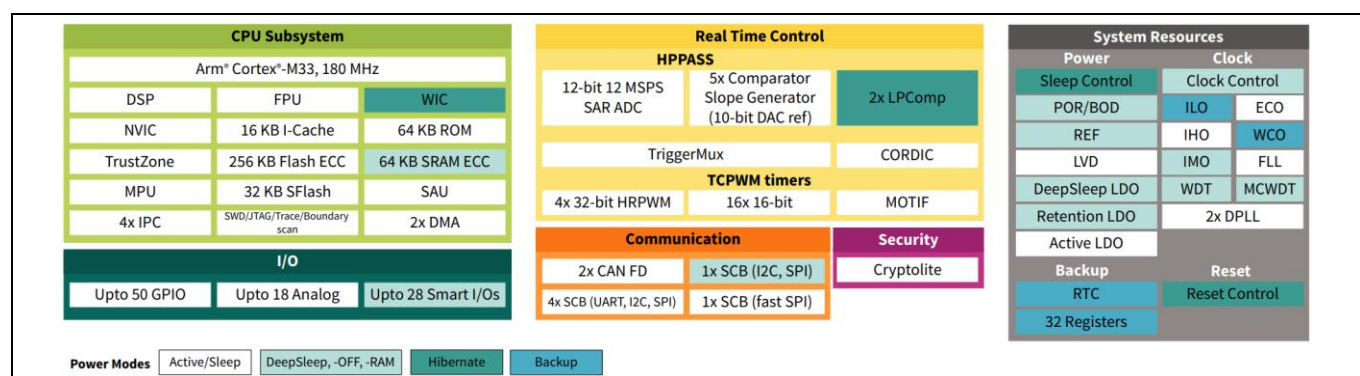


Figure 27 PSOC Control C3 – key features



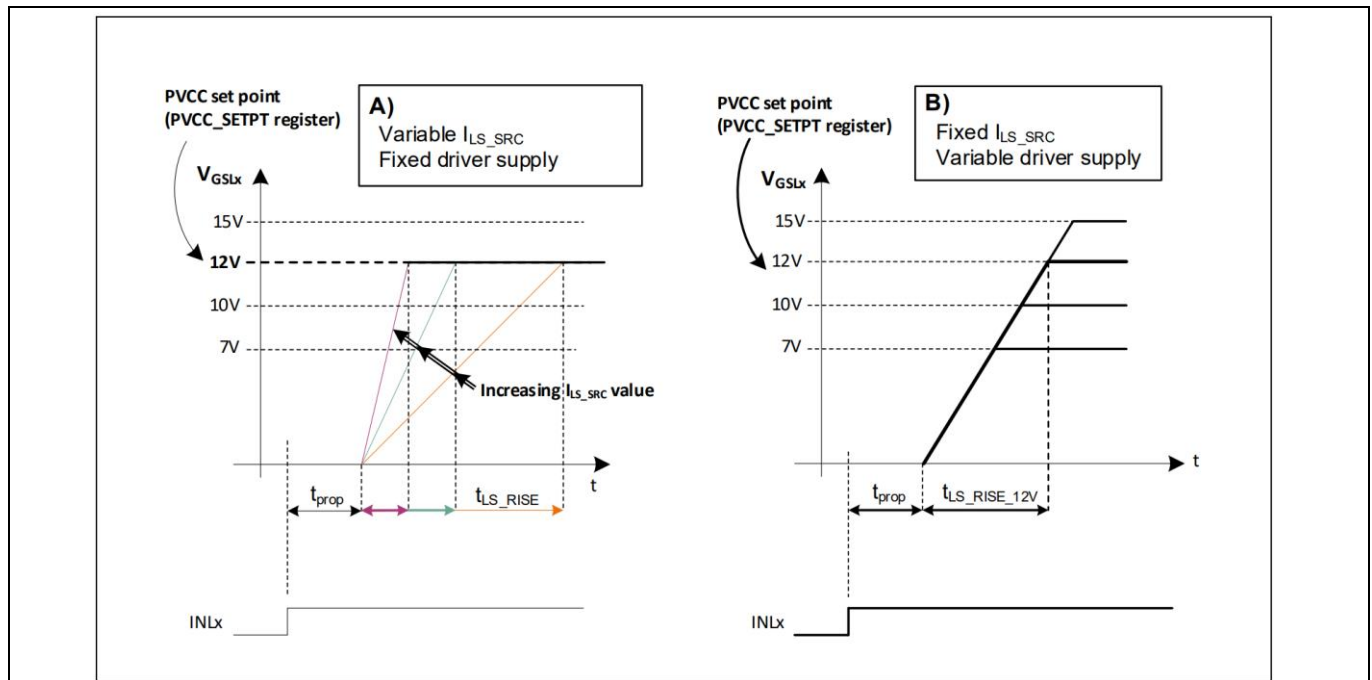
## Hardware functional description

**Table 4 Available pins for IO reconfiguration**

Available I/O		Details
Pin	Access	
P5.3	X1	
AN_B3	X28	
AN_B4	X29	
AN_B5	X30	

## 6.2 Key gate driver information: 6EDL7151

Infineon's MOTIX™ 6EDL7151 smart gate driver provides optimized gate drive pulses to the high- and low-side MOSFETs. These gate drivers allow operation over the full duty cycle range up to 100%. You can set the gate drive voltages to different levels, including 7 V, 10 V, 12 V, 15 V, and 20 V. One benefit of the charge pumps is that voltage levels can be maintained even if the battery voltage drops to a lower level, letting standard gate-level MOSFETs be used.



**Figure 28 Variable-switching behaviors and PVCC\_SETPT options**

Control of the drain-source rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors such as:

- Switching losses
- Dead time optimization

## Hardware functional description

- Drain voltage ringing

These factors lead to possible MOSFET avalanching. Correct configuration of the gate drive also helps you minimize EMI emissions. 6EDL7151 can control the slew rate of the driving signal to control the rise and fall slew rates of the drain-to-source voltage by adjusting the gate drive sink and source currents during different time segments throughout the switch-on and switch-off processes. This permits you to eliminate diode-resistor networks commonly used in gate drive circuits.

In most cases, gate resistors can be removed altogether, reducing component count – while simplifying and enabling further optimization of the circuit layout. Further instructions on how to perform these customizations is provided in the [Firmware variable configurations](#) section.

**Table 5 Gate drive parameters (Si)**

Param	Description	Min	Config
PVDD <sub>SETPT</sub>	Setpoint voltage for gate-switching voltage	7 V	12 V
I <sub>HS_SRC</sub>	Source current value for switching on high-side MOSFETs	10 mA	500 mA
I <sub>HS_SINK</sub>	Sink current value for switching off high-side MOSFETs	10 mA	500 mA
I <sub>LS_SRC</sub>	Current value for switching on low-side MOSFETs	10 mA	500 mA
I <sub>LS_SINK</sub>	Current value for switching off low-side MOSFETs	10 mA	500 mA
I <sub>PRE_SRC</sub>	Pre-charge current value for switching on both high-side and low-side	10 mA	1.5 A
I <sub>PRE_SNK</sub>	Pre-charge current value for switching off both high-side and low-side	10 mA	1.5 A
T <sub>DRIVE1</sub>	Amount of time that I <sub>PRE_SRC</sub> is applied. Shared configuration between high and low	0 ns	2.59 μs
T <sub>DRIVE2</sub>	Amount of time I <sub>HS_SRC</sub> and I <sub>LS_SRC</sub> are applied. Shared configuration between high-side and low-side drivers	0 ns	2.55 μs
T <sub>DRIVE3</sub>	Amount of time I <sub>PRE_SNK</sub> is applied. Shared configuration between high-side and low-side drivers	0 ns	2.59 μs
T <sub>DRIVE4</sub>	Amount of time I <sub>HS_SINK</sub> and I <sub>LS_SINK</sub> are applied. Shared configuration between high-side and low-side drivers	0 ns	2.55 μs

**Table 6 Gate drive parametersy (GaN)**

Param	Description	Min	Config
PVDD <sub>SETPT</sub>	Setpoint voltage for gate switching voltage	7 V	7 V
I <sub>HS_SRC</sub>	Source current value for switching on high-side MOSFETs	10 mA	500 mA
I <sub>HS_SINK</sub>	Sink current value for switching off high-side MOSFETs	10 mA	500 mA
I <sub>LS_SRC</sub>	Current value for switching on low-side MOSFETs	10 mA	500 mA
I <sub>LS_SINK</sub>	Current value for switching off low-side MOSFETs	10 mA	500 mA
I <sub>PRE_SRC</sub>	Pre-charge current value for switching on both high-side and low-side	10 mA	1.5 A
I <sub>PRE_SNK</sub>	Pre-charge current value for switching off both high-side and low-side	10 mA	1.5 A
T <sub>DRIVE1</sub>	Amount of time that I <sub>PRE_SRC</sub> is applied. Shared configuration between high and low	0 ns	2.59 μs
T <sub>DRIVE2</sub>	Amount of time that I <sub>HS_SRC</sub> and I <sub>LS_SRC</sub> are applied. Shared configuration between high-side and low-side drivers	0 ns	2.55 μs

## Hardware functional description

Param	Description	Min	Config
T <sub>DRIVE3</sub>	Amount of time that I <sub>PRE_SNK</sub> is applied. Shared configuration between high-side and low-side drivers	0 ns	2.59 μs
T <sub>DRIVE4</sub>	Amount of time that I <sub>HS_SINK</sub> and I <sub>LS_SINK</sub> are applied. Shared configuration between high-side and low-side drivers	0 ns	2.55 μs

*Note:* Important to configure any GaN devices with a 7 V switching voltage + diode clamping circuit. GaN should only be switched at 5 V.

The context of this application requires you to pay close attention to the configuration of the switching behaviors in the smart gate driver. During customized production of this reference guide, other important parameters you may need to configure are:

- Buck and linear regulators
- Charge pumps
- Current sense amplifiers

## 6.3 Overview of setup

This section talks about:

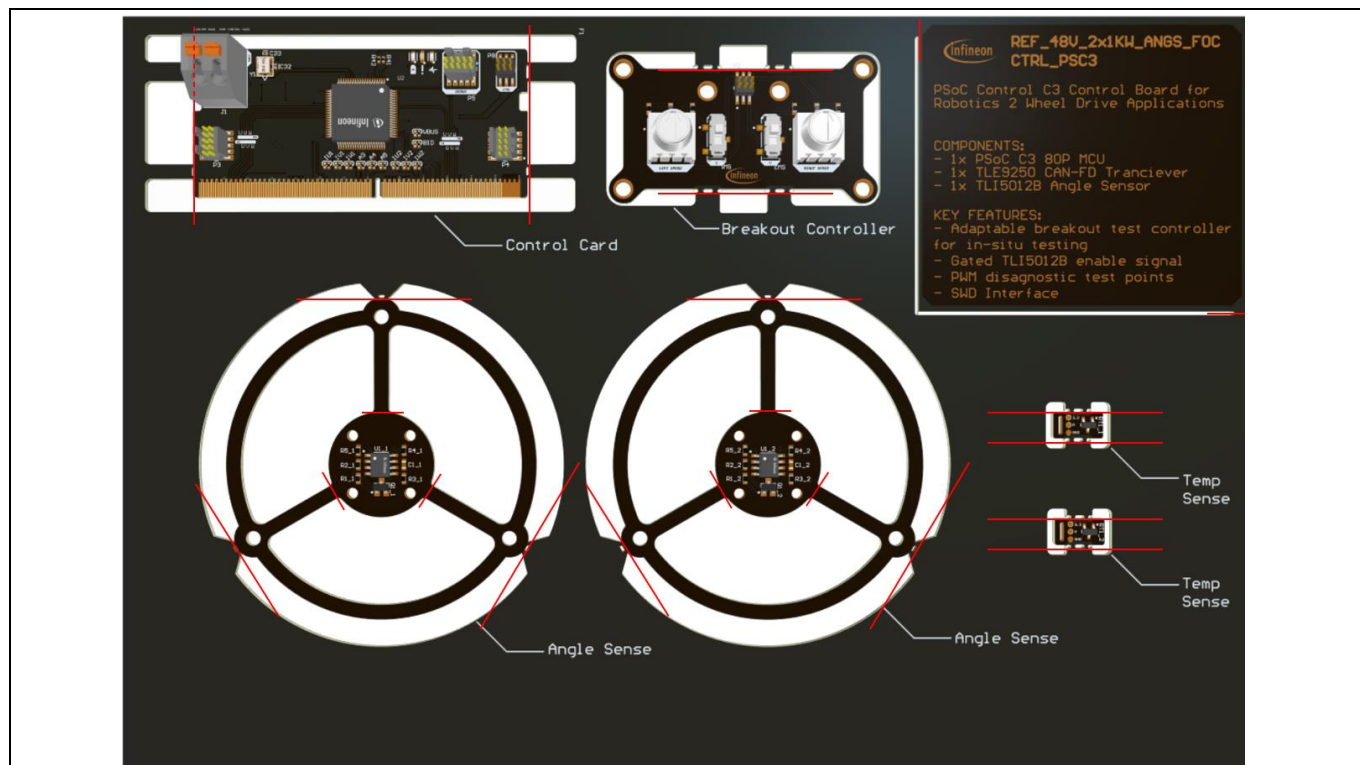
- The materials required for setup
- Important tools required for setting up the reference board
- Where to find the software needed for running this setup
- What you can expect for the general setup process

## 6.4 Hardware preparation

**Table 7** Hardware preparation checklist

Steps	Instruction	Details
1	Ensure the boards are properly depanelized	See the <b>Depanelization guide</b> below ( <a href="#">Figure 29</a> )
2	Slot control card into power board	See <b>how to insert SODIMM DDR4</b> if unclear
3	Ensure the connector cables fit into the debug and sensor connectors	See <a href="#">Figure 29</a> for how a fully assembled test system should look like

## Hardware functional description



**Figure 29 Depanelization guide (for the control card)**

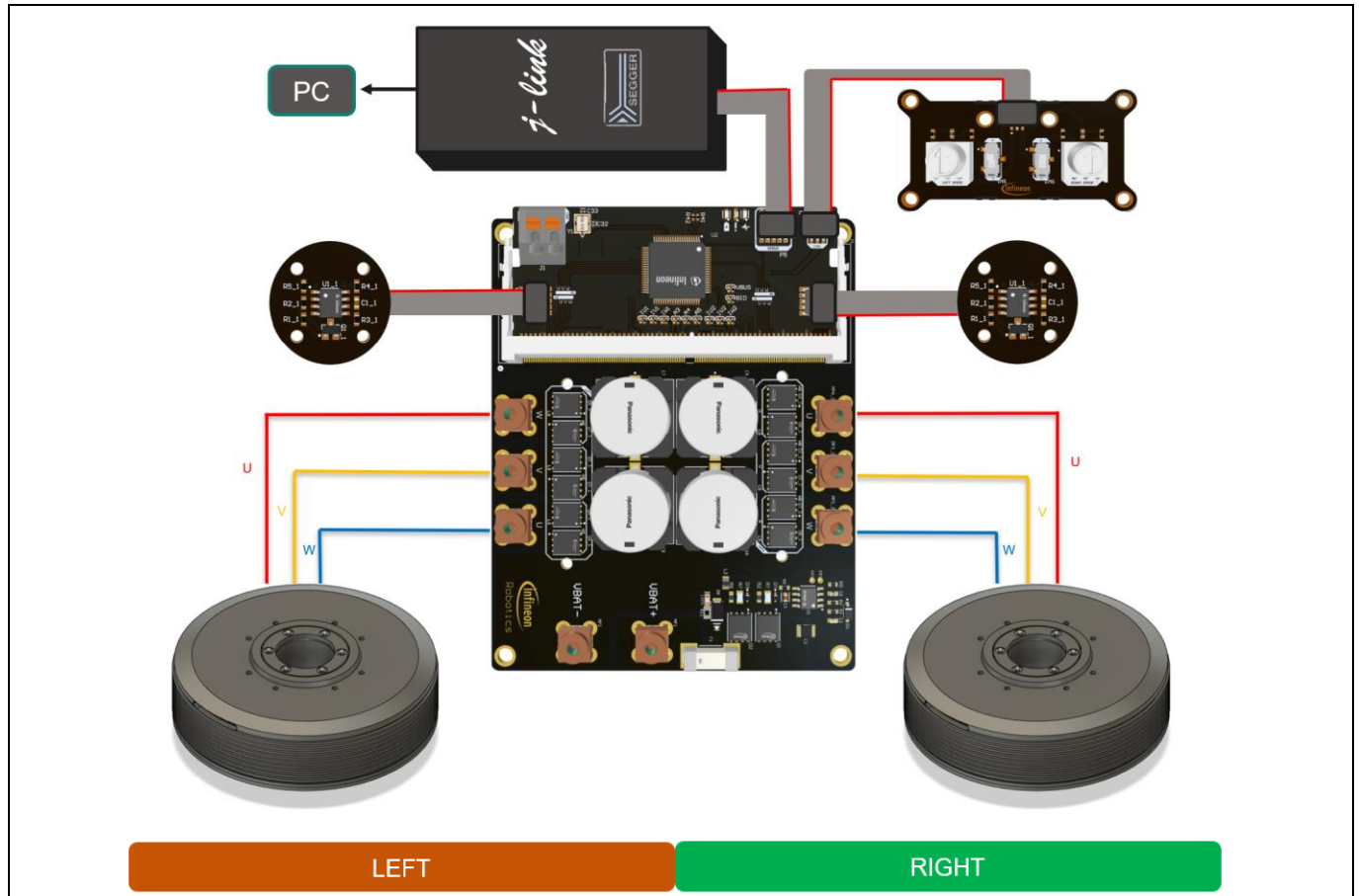
Depanelize the modules of the control card PCB by scoring along the red lines and snapping components off or snipping with a pair of sharp-tip flush wire cutters such as the one showed here:



**Figure 30 Sharp-tip flush wire cutters**

## Hardware functional description

### 6.4.1 Hardware connection



**Figure 31** System test connection diagram

Note:

1. Note the LEFT and RIGHT sides of this board. All orientations will reference this diagram.
2. The diametrical magnet will come preconfigured when testing under manufacturing verification purposes
3. If assembling from ground up, ensure to mark the placement and location of various components, such as:
  - The place where the diametrically-magnetized magnet is affixed relative to the rotor of the BLDC motor
  - The mounting position of the TLI5012B angle sensor board

## Hardware functional description

### 6.4.2 Firmware variable configurations

Firmware files necessary for changing motor configuration and behaviours are SPI\_6EDL Gateway *SGD.h* and *SGD.c*.

#### SGD.c

```

107 // Initialize the SPI
108 Cy_SCB_SPI_Init(SPI_SGD_HW, &SPI_SGD_config, &context);
109
110 #if defined(USING_MOTOR_L)
111 Cy_SCB_SPI_SetActiveSlaveSelect(SPI_SGD_HW, CY_SCB_SPI_SLAVE_SELECT0);
112 #elif defined(USING_MOTOR_R)
113 Cy_SCB_SPI_SetActiveSlaveSelect(SPI_SGD_HW, CY_SCB_SPI_SLAVE_SELECT1);
114 #endif
115 Cy_SCB_SPI_Enable(SPI_SGD_HW);
116
117 // Check the chip version
118 CY_ASSERT(SGD_ReadReg(ADDR_DEVICE_ID) == 0x0011);
119
120 // Write default configuration
121 // Dvdd oc threshold = 450mA
122 SGD_WriteReg(ADDR_SUPPLY_CFG, PVCC_SETPT_12V | CS_REF_CFG_1_2 | DVDD_OCP_THR_450 | DVDD_SFTSTRT_100us
123 | DVDD_SETPT_3_3 | BK_FREQ_1M | DVDD_TON_DELAY_200us | CP_PRECHARGE_DISABLE);
124
125 SGD_WriteReg(ADDR_ADC_CFG, ADC_OD_REQ_NO_ACTION | ADC_OD_IN_SEL_IDIGITAL | ADC_EN_FILT_ENABLE
126 | ADC_FILT_CFG_8_SAMPLES | ADC_FILT_CFG_PVDD_32_SAMPLES);
127
128 // HW brake mode set to high z
129 SGD_WriteReg(ADDR_PWM_CFG, PWM_MODE_6 | PWM_FREEW_CFG_ACTIVE | BRAKE_CFG_HIGH_Z | PWM_RECIRC_DISABLE);
130 // OT shut down enabled
131 const uint16_t Shunt_Amp_Timing_Mode = (params.sys.analog.shunt.type == Three_Shunt) ? CS_TMODE_GLxHIGH : CS_TMODE_ALWAYS;
132 //const uint16_t Shunt_Amp_Timing_Mode = CS_TMODE_ALWAYS;
133 SGD_WriteReg(ADDR_SENSOR_CFG, HALL DEGLITCH_640ns | OTS_DIS_PROTECTION_ENABLE | Shunt_Amp_Timing_Mode);
134 // WD fault disabled
135 SGD_WriteReg(ADDR_WD_CFG, WD_EN_DISABLE | WD_INSEL_EN_DRV | WD_FLTCFG_REGISTER | WD_TIMER_T_100us);
136 // WD brake disabled, locked rotor fault disabled
137 SGD_WriteReg(ADDR_WD_CFG2, WD_BRAKE_NORMAL | WD_EN_LATCH_DISABLE | WD_DVDD_RSTRT_ATT_0
138 | WD_DVDD_RSTRT_DLY_0ms5 | WD_RLOCK_EN_DISABLE | WD_RLOCK_T_1s | WD_BK_DIS_DISABLE);
139
140 SGD_WriteReg(ADDR_IDRIVE_CFG, IHS_SRC_500mA | IHS_SINK_500mA | ILS_SRC_500mA | ILS_SINK_500mA);
141 SGD_WriteReg(ADDR_IDRIVE_PRE_CFG, I_PRE_SRC_500mA | I_PRE_SINK_500mA | I_PRE_SRC_EN_ENABLED | I_PRE_SNK_EN_ENABLED);
142 SGD_WriteReg(ADDR_TDRIVE_SRC_CFG, TDRIVE1_80ns | TDRIVE2_100ns);
143 SGD_WriteReg(ADDR_TDRIVE_SINK_CFG, TDRIVE3_200ns | TDRIVE4_100ns);
144
145 SGD_WriteReg(ADDR_DT_CFG, DT_RISE_120ns | DT_FALL_120ns);
146
147 SGD_WriteReg(ADDR_CP_CFG, CP_CLK_CFG_781_25kHz | CP_CLK_SS_DIS_ENABLED);
148 // CS_OCP fault enabled, 8us deglitch time:
149 const uint16_t CS_Gain = (uint16_t)(params.sys.analog.shunt.opamp_gain) << 0U;
150 SGD_WriteReg(ADDR_CSAMP_CFG, CS_Gain | CS_EN_PHASE_A | CS_EN_PHASE_B | CS_EN_PHASE_C
151 | CS_BLANK_500ns | CS_EN_DCCAL_DISABLE | CS_OCP_DEGLITCH_8us | CS_OCPFLT_CFG_ALL); // set
152 // CS_OCP fault braking disabled, threshold = +/-300A, latched
153 SGD_WriteReg(ADDR_CSAMP_CFG2, CS_OCP_PTHR_300mV | CS_OCP_NTHR_300mV | CS_OCP_LATCH_ENABLE
154 | CS_MODE_SHUNT | CS_OCP_BRAKE_DISABLE | CS_TRUNC_DIS_DISABLE
155 | CS_NEG_OCP_DIS_ENABLE | CS_AZ_CFG_INTERNAL); // set, +/-300A fault threshold
156 SGD_WriteReg(ADDR_OTP_PROG, OTP_PROG_DISABLE);
157
158 // Disable brake and enable the now configured gate driver
159 // Nitin: disabled as there is no connection to nbrake pin from MCU
160 //Cy_GPIO_Set(N_BRK_SGD_PORT, N_BRK_SGD_NUM);
161 Cy_GPIO_Set(EN_DRV_SGD_PORT, EN_DRV_SGD_NUM);

```

- Line 122: PVCC\_SETPT\_12V can be set as various options, including 7 V, 10 V, 12 V, and 15 V
- You can find all these options within the SGD.h library file; changing them simply reconfigures the register values to control the switching gate voltage. If a GaN-based inverter is used, make sure to set the SUPPLY\_CFG to PVCC\_SETPT\_7V



## Hardware functional description

```

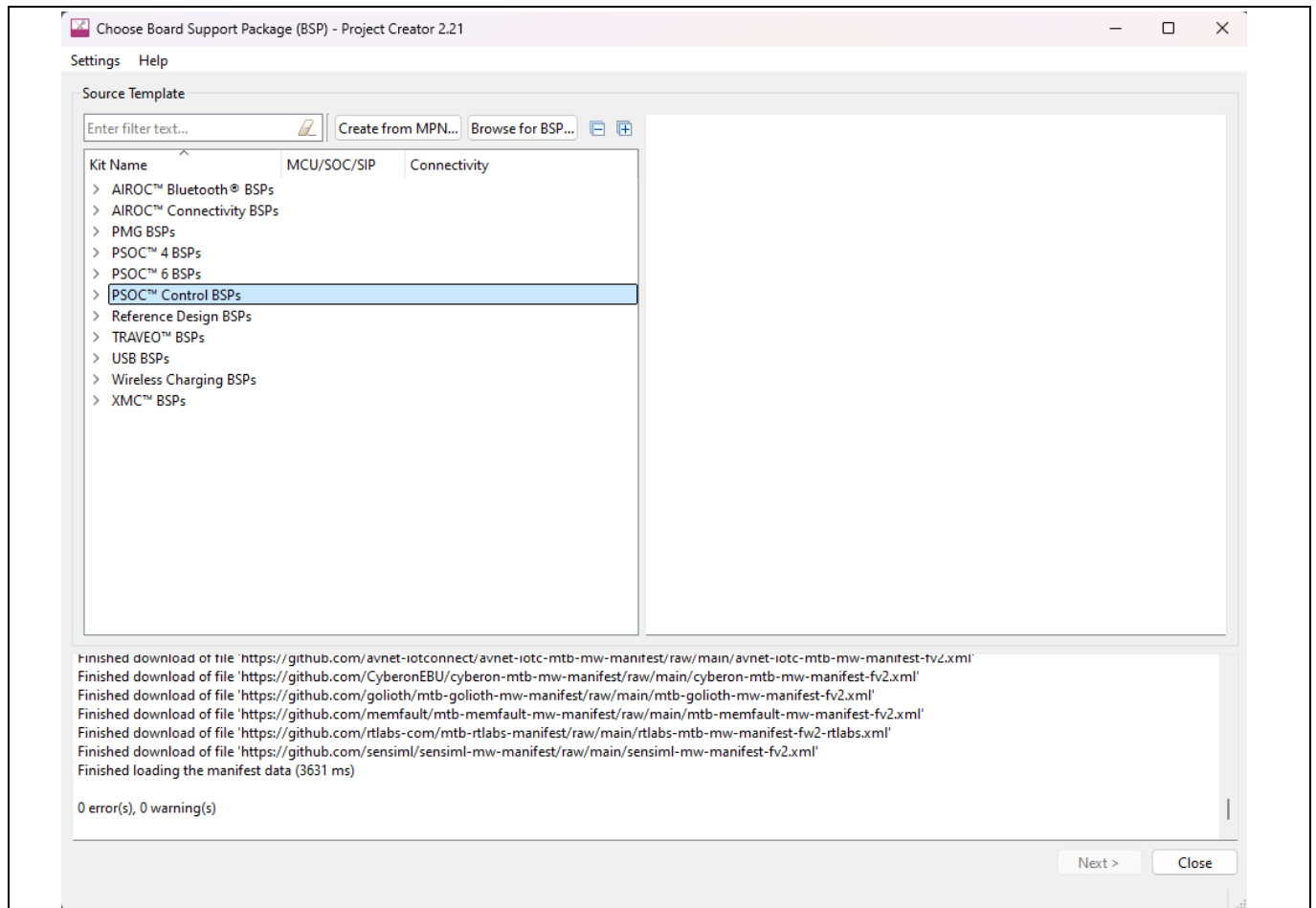
102 // SUPPLY_CFG
103 #define PVCC_SETPT_12V          (0x0000)
104 #define PVCC_SETPT_15V          (0x0001)
105 #define PVCC_SETPT_10V          (0x0002)
106 #define PVCC_SETPT_7V           (0x0003)
107 #define CS_REF_CFG_1_2          (0x0000)
108 #define CS_REF_CFG_5_12         (0x0004)
109 #define CS_REF_CFG_1_3          (0x0008)
110 #define CS_REF_CFG_1_4          (0x000C)
111 #define DVDD_OCP_THR_450        (0x0000)
112 #define DVDD_OCP_THR_300        (0x0010)
113 #define DVDD_OCP_THR_150        (0x0020)
114 #define DVDD_OCP_THR_50         (0x0030)
115 #define DVDD_SFTSTRT_100us      (0x0000)
116 #define DVDD_SFTSTRT_200us      (0x0040)
117 #define DVDD_SFTSTRT_300us      (0x0080)
118 #define DVDD_SFTSTRT_400us      (0x00C0)
119 #define DVDD_SFTSTRT_500us      (0x0100)
120 #define DVDD_SFTSTRT_600us      (0x0140)
121 #define DVDD_SFTSTRT_700us      (0x0180)
122 #define DVDD_SFTSTRT_800us      (0x01C0)
123 #define DVDD_SFTSTRT_900us      (0x0200)
124 #define DVDD_SFTSTRT_1000us     (0x0240)
125 #define DVDD_SFTSTRT_1100us     (0x0280)
126 #define DVDD_SFTSTRT_1200us     (0x02C0)
127 #define DVDD_SFTSTRT_1300us     (0x0300)
128 #define DVDD_SFTSTRT_1400us     (0x0340)
129 #define DVDD_SFTSTRT_1500us     (0x0380)
130 #define DVDD_SFTSTRT_1600us     (0x03C0)
131 #define DVDD_SETPT_VSENSE       (0x0000)
132 #define DVDD_SETPT_3_3          (0x0800)
133 #define DVDD_SETPT_5            (0x0C00)
134 #define BK_FREQ_500K            (0x0000)
135 #define BK_FREQ_1M              (0x1000)
136 #define DVDD_TON_DELAY_200us    (0x0000)
137 #define DVDD_TON_DELAY_400us    (0x2000)
138 #define DVDD_TON_DELAY_600us    (0x4000)
139 #define DVDD_TON_DELAY_800us    (0x6000)
140 #define CP_PRECHARGE_DISABLE     (0x0000)
141 #define CP_PRECHARGE_ENABLE     (0x8000)

```

**Figure 32 Gate driver supply configuration macros (6EDL7151)**

For all firmware documentation, see the ModusToolbox™ Application creator wizard. All new firmware releases for the PSOC C3 Control card can be found here:

## Hardware functional description



**Figure 33 Finding firmware documentation in ModusToolbox™ Application creator wizard**

Here you will find:

- Changelogs from version to version
- Instructions for tuning the motor driver to the motor being used
- Access to the ModusToolbox™ Motor Suite GUI for quick deployment and customization



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## References

## References

- [1] Infineon Technologies AG: *Application note - Gate drive for power MOSFETs in switching applications*;  
[Available online](#)

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## Revision history

### Revision history

Document version	Date of release	Description of changes
V 1.0	2025-03-05	Initial release

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