Customer Training Workshop

Traveo™ II Pulse Width Modulation (PWM) Interface

Q4 2020

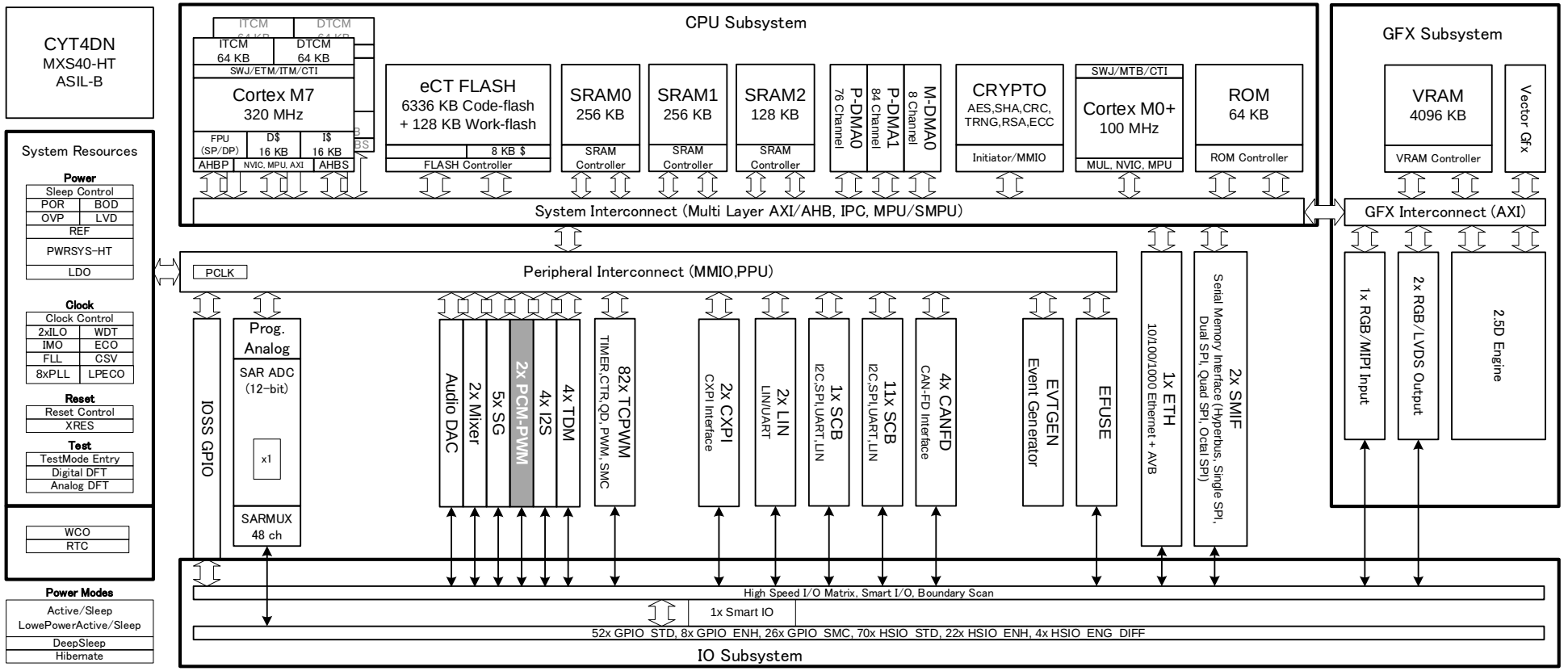
Target Products

- Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Cluster

› The PWM is part of Peripheral Blocks



Hint Bar

Review TRM chapter 33 for additional details

Pulse Width Modulation (PWM) Overview

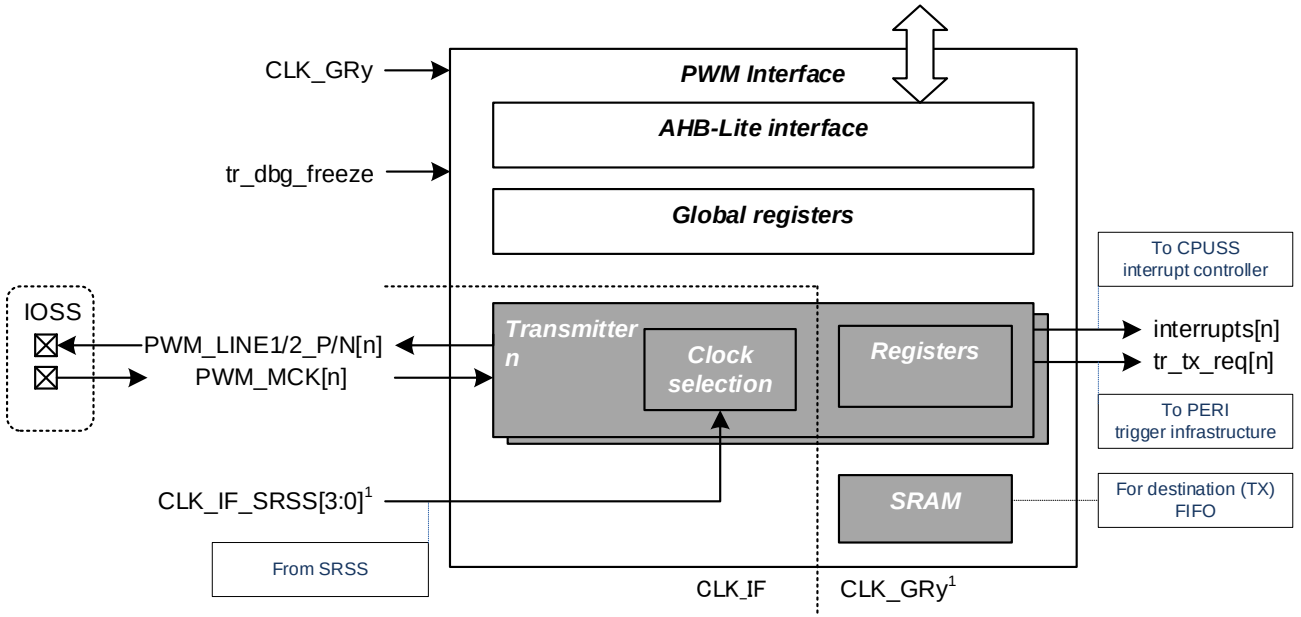
- Pulse Width Modulation (PWM)
  - PWM interface drives PWM output lines and their complementary output lines
  - PWM destinations are E-bridges or H-bridges, which drive low-cost speakers
  - PWM interface processes Pulse Code Modulated (PCM) input signals into PWM output signals
- Features
  - Programmable interface clock
  - Programmable doubling mode
  - Programmable gain
  - Programmable PWM
  - Programmable PCM sample formatting (8, 10, 12, 14, 16, 18, 20, 24, and 32 bits)
  - 64-entry TX FIFO with interrupt and trigger support

Hint Bar

Review TRM section 33.3 for additional details

PWM Block Diagram

- PWM components
  - PWM Interface
  - Clock
  - Transmitter
  - SRAM



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Review TRM section 33.3.2 for additional details

SRSS clock (CLK_IF_SRSS[3:0]) is dependent on the device

CLK_GR: Clock input to peripheral functions

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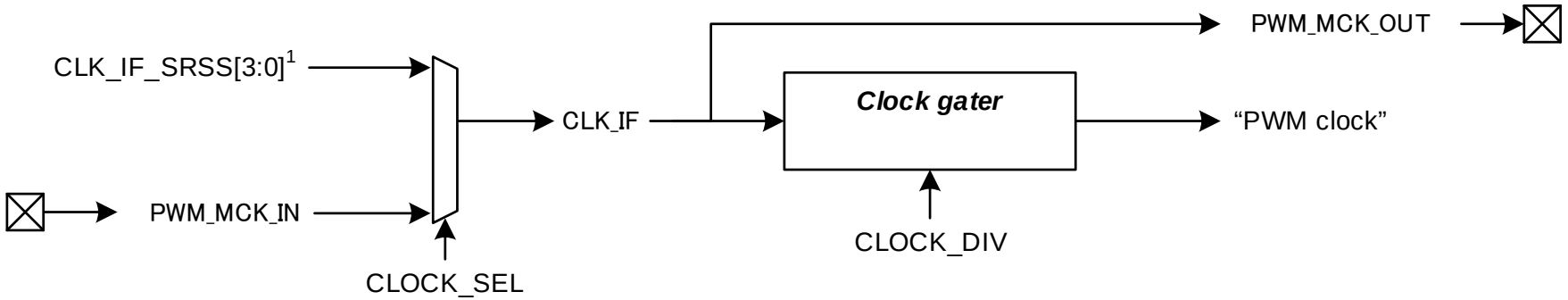
Clock

- PWM interface clock can be derived from either of these clock signals

Signal	Description
CLK_IF_SRSS[3:0][1]	SRSS clock.
PWM_MCK_IN	Master interface clock.

- An interface clock CLK_IF is derived and then gated to derive the PWM clock



Hint Bar

Review TRM section 33.3.3 for additional details

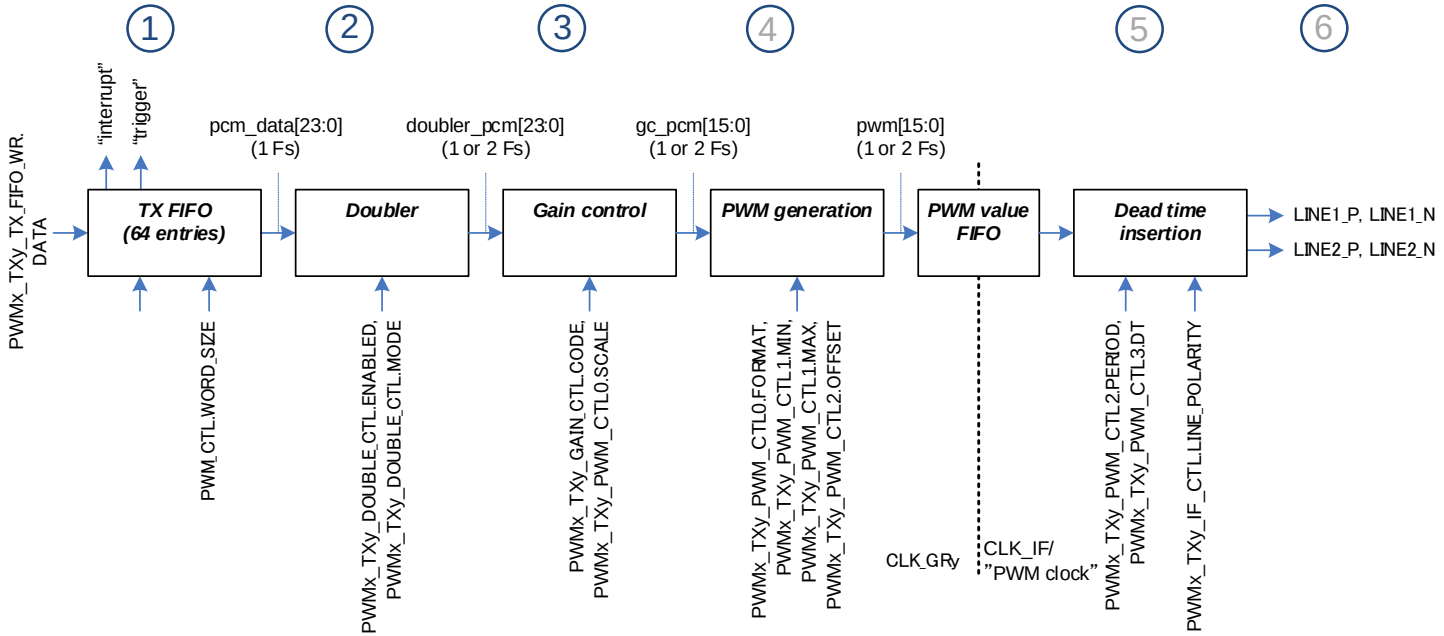
Review the Clock System Training section for additional details about high-frequency clocks

[1] Note: See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy.

PWM Output

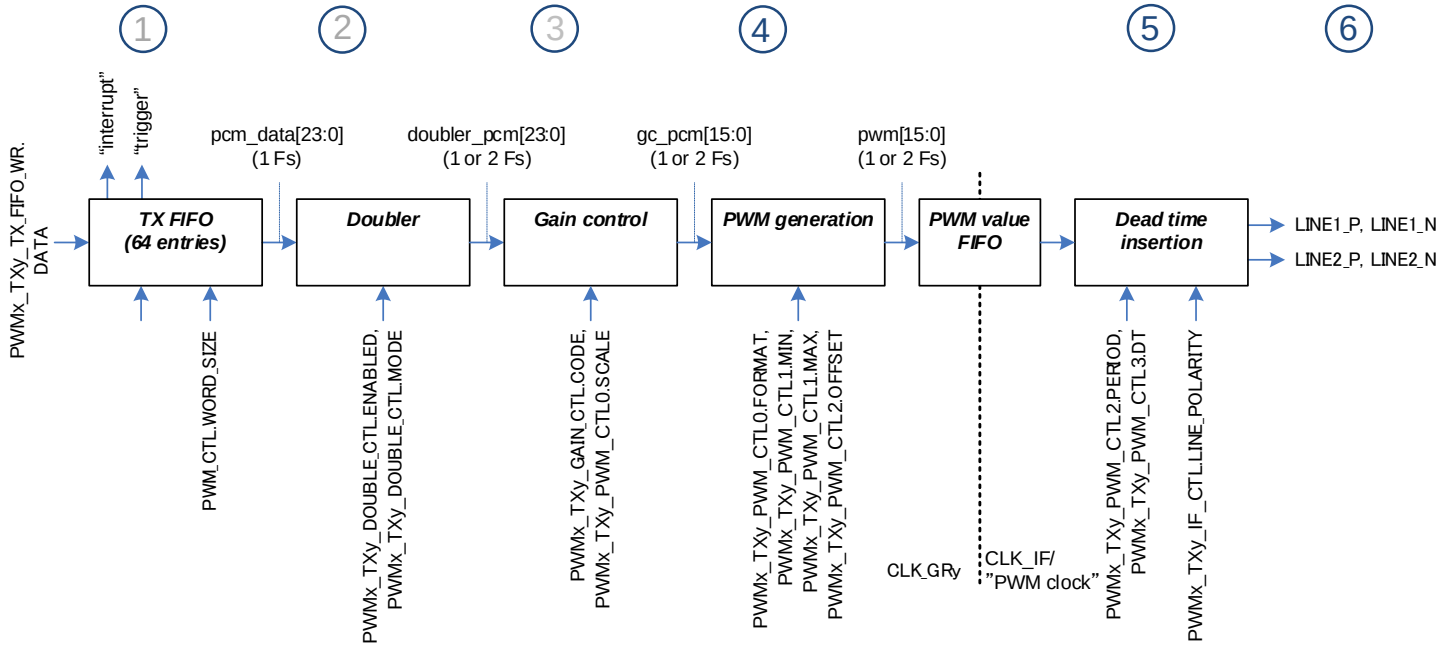
› PWM values pwm[15:0] are processed from the incoming TX FIFO PCM data in the following manner:

1. TX FIFO: Translates data into 24-bit PCM values, as specified by PWM_CTL.WORD_SIZE
2. Doubler: Doubles the PCM value frequency through either sample repetition or sample averaging, as specified by PWMx_TXy_DOUBLE_CTL
3. Gain control: Scales the PCM values by programmable multiplier value COEFF[13:0] and scale value SCALE[3:0]



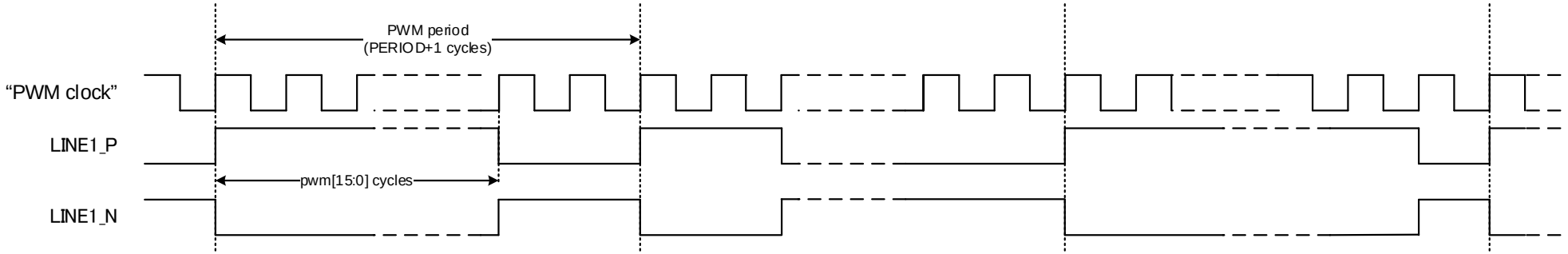
PWM Output

- PWM values pwm[15:0] are processed from the incoming TX FIFO PCM data
  4. PWM generation:
     - PWM format (E-bridge or H-bridge)
     - PWM period (PERIOD[15:0])
     - Offset value (OFFSET[15:0]) (only used in E-bridge mode)
  5. Dead time insertion
  6. PWM Output

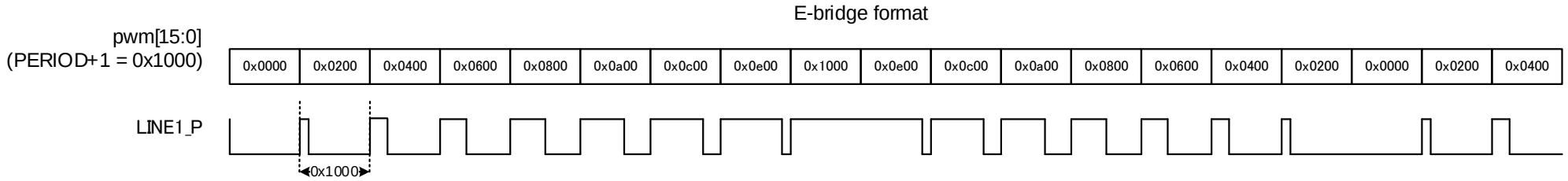


PWM Format

- E-bridge format
  - Used to drive the LINE1_P/N PWM output lines

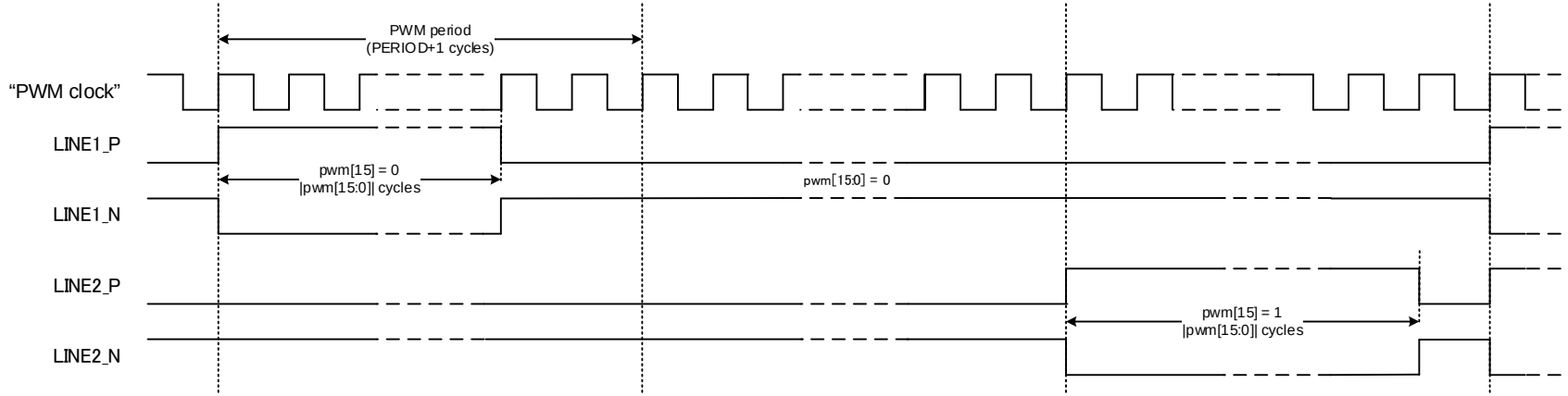


- PCM to PWM Modulation at a Coarser Grain (E-bridge Format)

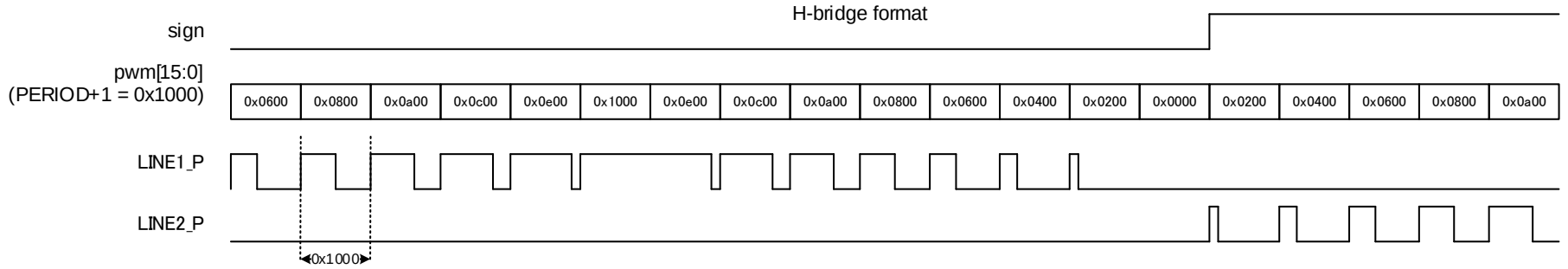


PWM Format

- H-bridge format
  - Used to drive the LINE1_P/N and LINE2_P/N PWM output lines

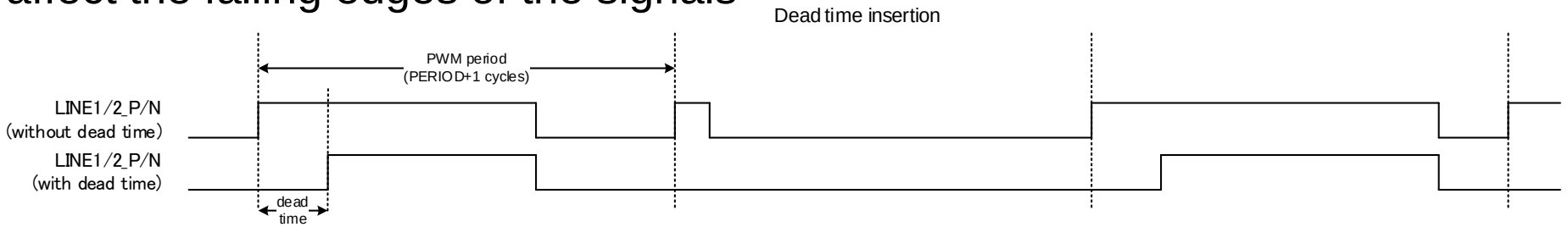


- PCM to PWM Modulation at a Coarser Grain (H-bridge Format)

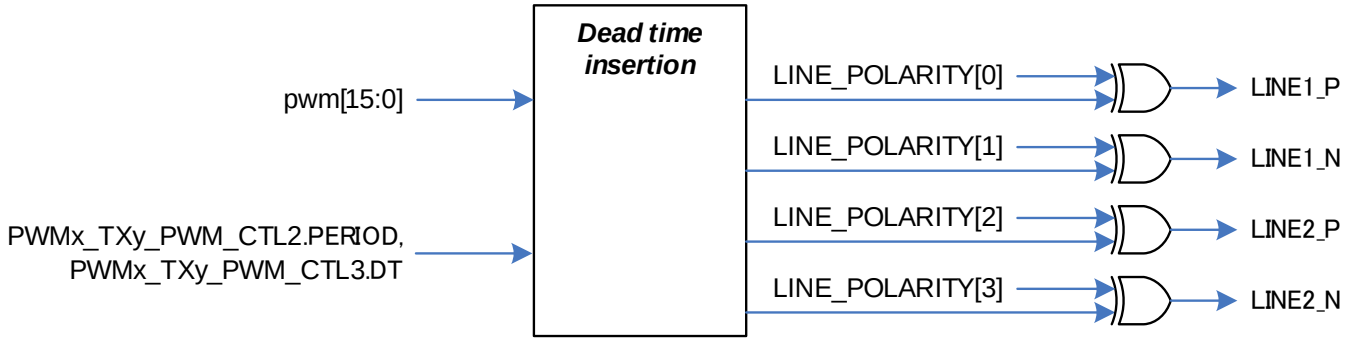


Dead Time

- Dead Time Insertion
  - Dead time insertion is deployed before polarity inversion of the PWM output lines
  - Dead time insertion effectively “delays” the rising edges of all PWM output signals, but does not affect the falling edges of the signals



- Polarity Control of PWM Output Lines
  - After dead time insertion, the polarity of all four PWM output lines can be inverted



Interrupt

- PWM interrupt can be triggered under any of the following events

TX Interrupt	Set condition
FIFO_TRIGGER	TX trigger is generated.
FIFO_OVERFLOW	Writing to a full TX FIFO (TX_FIFO_STATUS.USED is "64"). This is referred to as an underflow event.
FIFO_UNDERFLOW	Reading from an empty TX FIFO (TX_FIFO_STATUS.USED is "0").
IF_UNDERFLOW[1]	PCM samples are generated too fast by the interface logic. May indicate that the IP system frequency is too low with respect to the interface frequency (a SW configuration error).

Hint Bar

Review TRM section 33.3.6 and Register TRM for additional details

[1] This functionality is for debug purposes

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6676158	09/17/2019	Initial release
*A	6805471	02/12/2020	Added note descriptions in each slide
*B	7031887	11/26/2020	Updated pages 2, 5, and 6
*C	7065462	01/12/2021	Updated page 2