Customer Training Workshop Traveo™ II Program and Debug Interface

Q4 2020

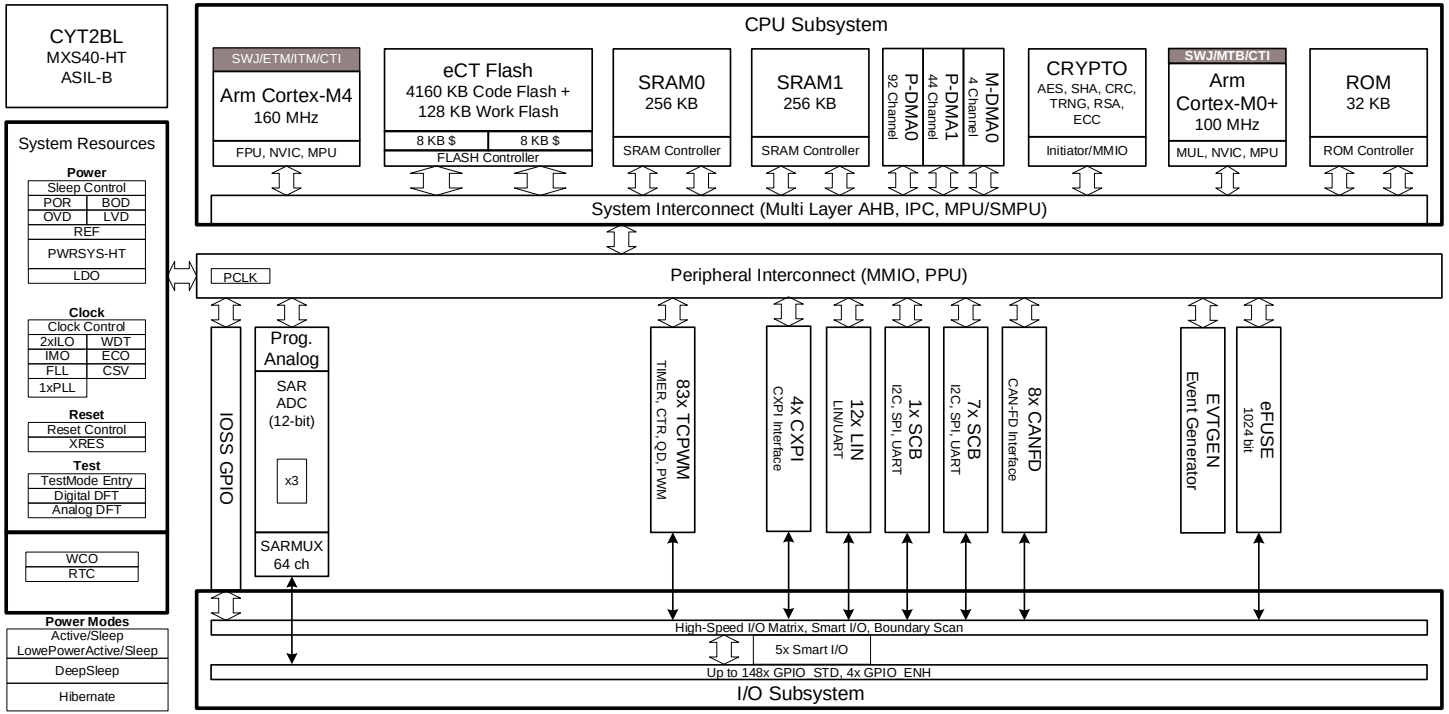
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160KB
Traveo II Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Body Controller Entry

› The program and debug interface is part of the CPU subsystem

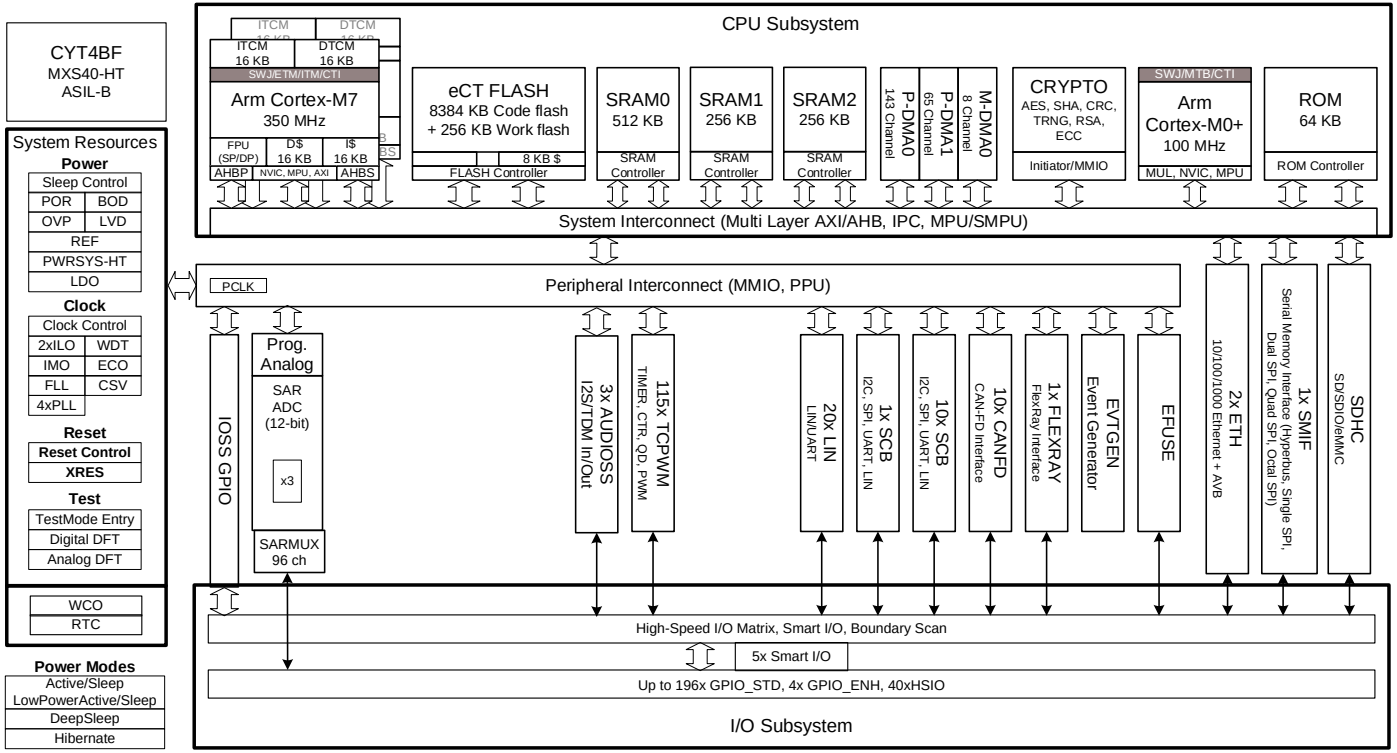


Hint Bar

Review TRM chapter 32 for additional details

Introduction to Traveo II Body Controller High

› The program and debug interface is part of the CPU subsystem

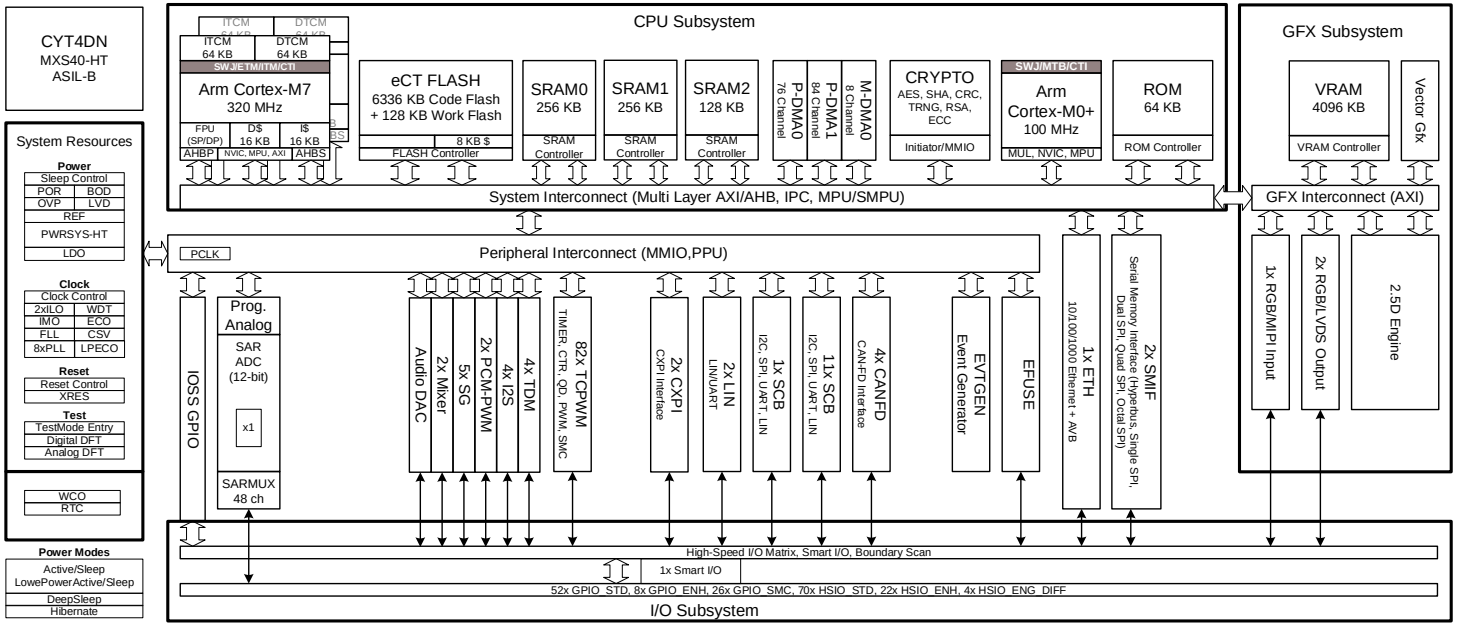


Hint Bar

Review TRM chapter 36 for additional details

Introduction to Traveo II Cluster

› The program and debug interface is part of the CPU subsystem



Hint Bar

Review TRM chapter 38 for additional details

Program and Debug Interface Overview

- The program and debug interface is a communication gateway for an external device to perform programming and debugging
- The external device includes a
  - Cypress-supplied programmer
  - Third-party programmer and debugger
- Communication protocol between the external device and Traveo II microcontroller is supplied by
  - Serial wire debug (SWD)
  - Joint Test Action Group (JTAG)

Hint Bar

Review the Program and Debug Interface TRM chapter for additional details

Multi-Core Debug for CYT2B6/B7/B9/BL

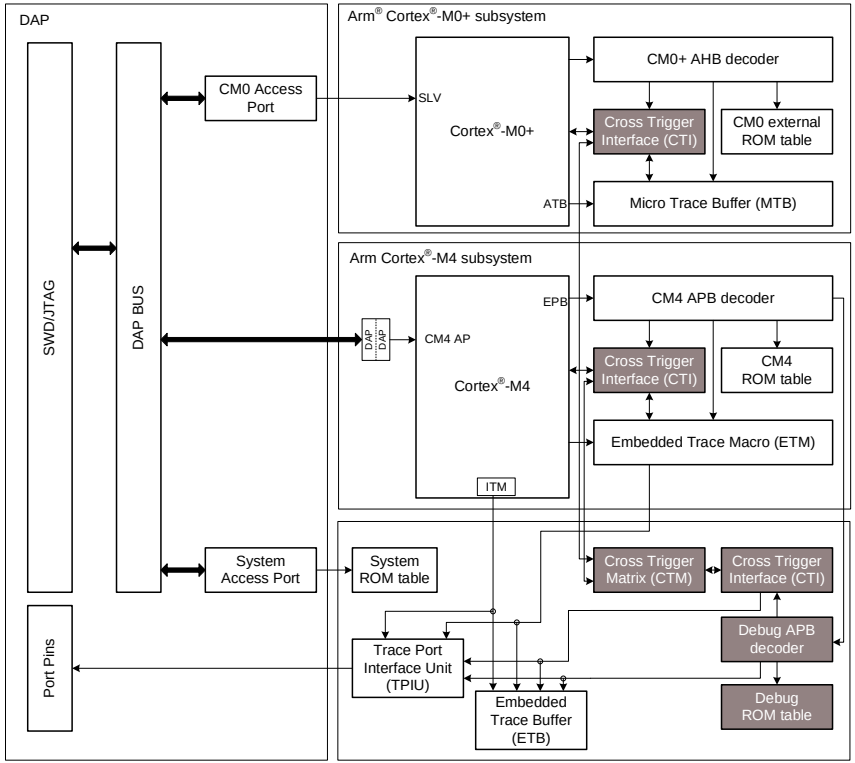
- Arm® Cortex®-M0+ Core debug components
  - Cross-triggering interface (CTI), four hardware breakpoints, and two watchpoints
- Arm Cortex-M4 Core debug components
  - CTI, six hardware breakpoints, and four watchpoints
- Enables multi-core debug
  - Three CTIs connected via cross-triggering matrix (CTM)
  - Start or stop CM0+/CM4 at the same time
  - Start or stop instruction tracing based on whether or not the trace buffer is full, or on the break
- Debug and access port (DAP) security
  - Three access ports (APs) each can be independently disabled
  - eFuse (permanent)
  - System AP is protected by MPU

Hint Bar

Review TRM chapter 31 and CoreSight documentation for additional details

Multi-Core Debug for CYT2B6/B7/B9/BL

Program and Debug Interface for Debug



Hint Bar

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Multi-Core Debug for CYT3BB/4BB/3DL/4DN

- Arm® Cortex®-M0+ Core debug components
  - Cross-triggering interface (CTI), four hardware breakpoints, and two watchpoints
- Arm Cortex-M7 Core debug components
  - CTI, six hardware breakpoints, and four watchpoints
- Enables multi-core debug
  - Three CTIs connected via cross-triggering matrix (CTM)
  - Start or stop CM0+/CM7 at the same time
  - Start or stop instruction tracing based on whether or not the trace buffer is full, or on the break
- Debug and access port (DAP) security
  - Four access ports (APs) each can be independently disabled
  - eFuse (permanent)
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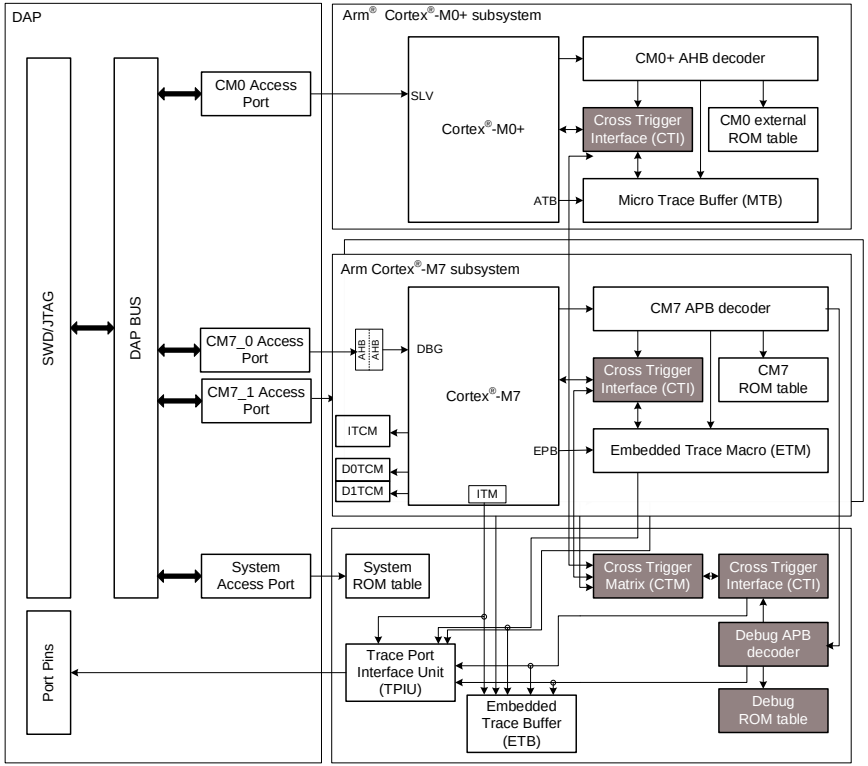
Multi-Core Debug for CYT3BB/4BB/3DL/4DN

Program and Debug Interface for Debug



Hint Bar

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Tracing for CYT2B6/B7/B9/BL

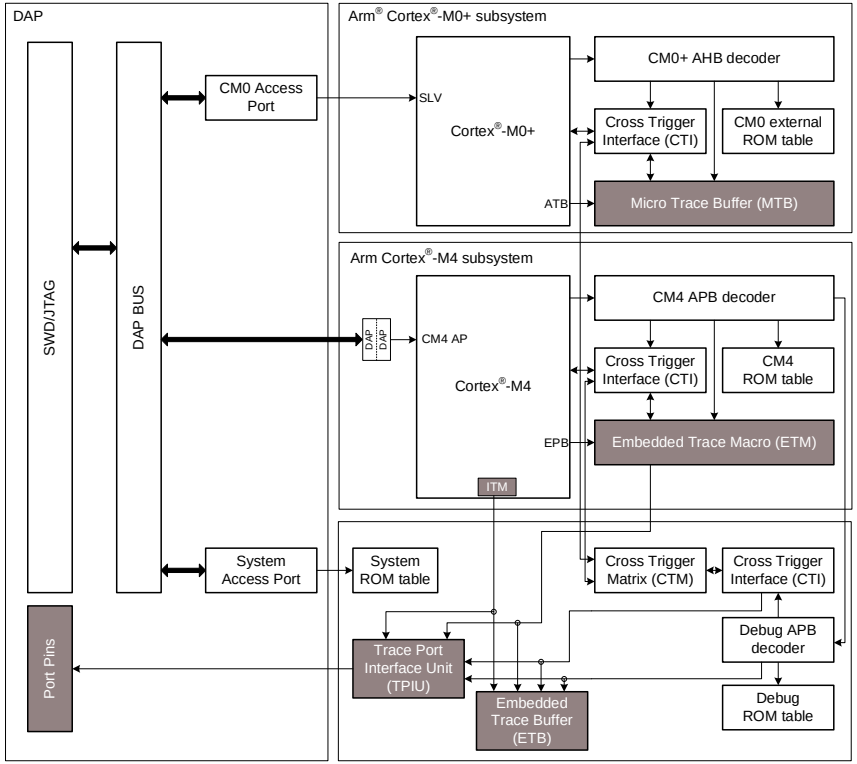
- Arm® Cortex®-M0+
  - Micro trace buffer (MTB) for tracing and storing instructions
- Arm Cortex-M4
  - Serial wire viewer (SWV) for output trace information with single pin at SWO
  - Embedded trace macrocell (ETM) for tracing instructions
  - Embedded trace buffer (ETB) for tracing instructions and storing them in a local SRAM
  - Instrumentation trace macrocell (ITM) for tracing output
  - Trace port interface unit (TPIU) for tracing information from the chip to an external trace port analyzer
    - Parallel (4 pins, multiplexed with GPIO and clock pin)
    - SWO (multiplexed on JTAG TDO)

Hint Bar

Review TRM chapter 31 and CoreSight Documentations for additional details

Tracing for CYT2B6/B7/B9/BL

Program and Debug Interface for Tracing



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Tracing for CYT3BB/4BB/3DL/4DN

- Arm® Cortex®-M0+
  - Micro trace buffer (MTB) for tracing and storing instructions
- Arm Cortex-M7
  - Embedded trace macrocell (ETM) for tracing instructions
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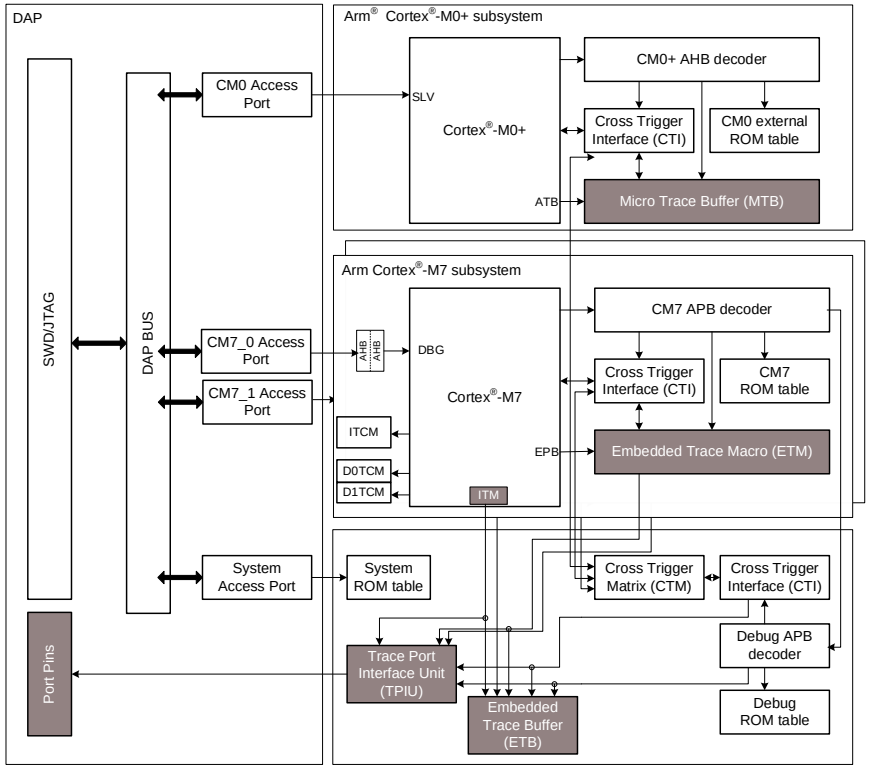
Tracing for CYT3BB/4BB/3DL/4DN

Program and Debug Interface for Tracing



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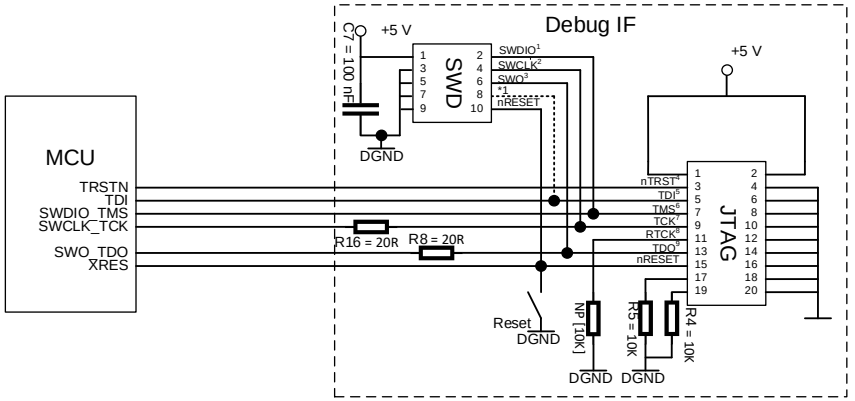
Serial Wire Debug (SWD) and JTAG Interface

- The SWD protocol is a packet-based serial transaction protocol
- JTAG controller and interface are compliant to IEEE-1149.1-2001
  - The test access port (TAP) interface is used to control the values in the boundary scan cells
  - Boundary scan test supported



*1: Only needed if SWD connector should also provide JTAG lines

[1] Serial wire data I/O
[2] Serial wire clock
[3] Serial wire output
[4] Test reset
[5] Test data in
[6] Test mode select
[7] Test clock
[8] Return test clock
[9] Test data out

Debug interface pin configuration on Boot ROM

After reset, the debug pins remain in high-impedance mode until Boot ROM initializes them as follows:

Pin Name	Input Enable	Drive Mode
swj_trstn	Yes	Internal Pull-up
swj_swo_tdo	No	Strong (output)
swj_swdoe_tdi	Yes	Internal Pull-up
swj_swdio_tms	Yes	Internal Pull-up
swj_swclk_tclk	Yes	Internal Pull-down

Hint Bar

Review the Program and Debug Interface TRM chapter for additional details

Programmer and IDEs for Traveo II

Flash Programmer

Vendor	Flash Programmer	Software	Notes
Infineon	MiniProg3	Cypress Programmer 1.0	Only for CYT2B7
	MiniProg4	Auto Flash Utility	
DTS Insight	NET IMPRESS AF430/AFX100	AZ490 Remote Controller	
Segger	J-Link	J-Flash	
	Flasher Arm (for mass production)		

Integrated Design Environment (IDE)

Vendor	Debugger	Compiler
GHS	GHS Probe (5.6.4/5.6.6)	MULTI V7 (ver2017.1.4)
IAR	I -JET	Embedded Workbench for Arm (8.42.1)
iSystem	i-TAG Family	–
Lauterbach	TRACE 32	–

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Revision History

Revision	ECN	Submission Data	Description of Change
**	6086858	04/17/2018	Initial release
*A	6400751	12/4/2018	Added the note descriptions. Updated the Block Diagram Updated SWD and JTAG I/F figures. Added CYT4BF information
*B	6661420	08/26/2019	Updated pages 2 and 13. Added CYT4DN information and added page 6.
*C	7052549	12/22/2020	Updated pages 2, 13, 16 Merged page 3 for Traveo II Body Controller Entry