Customer Training Workshop

Traveo™ II FlexRay

Q4 2020

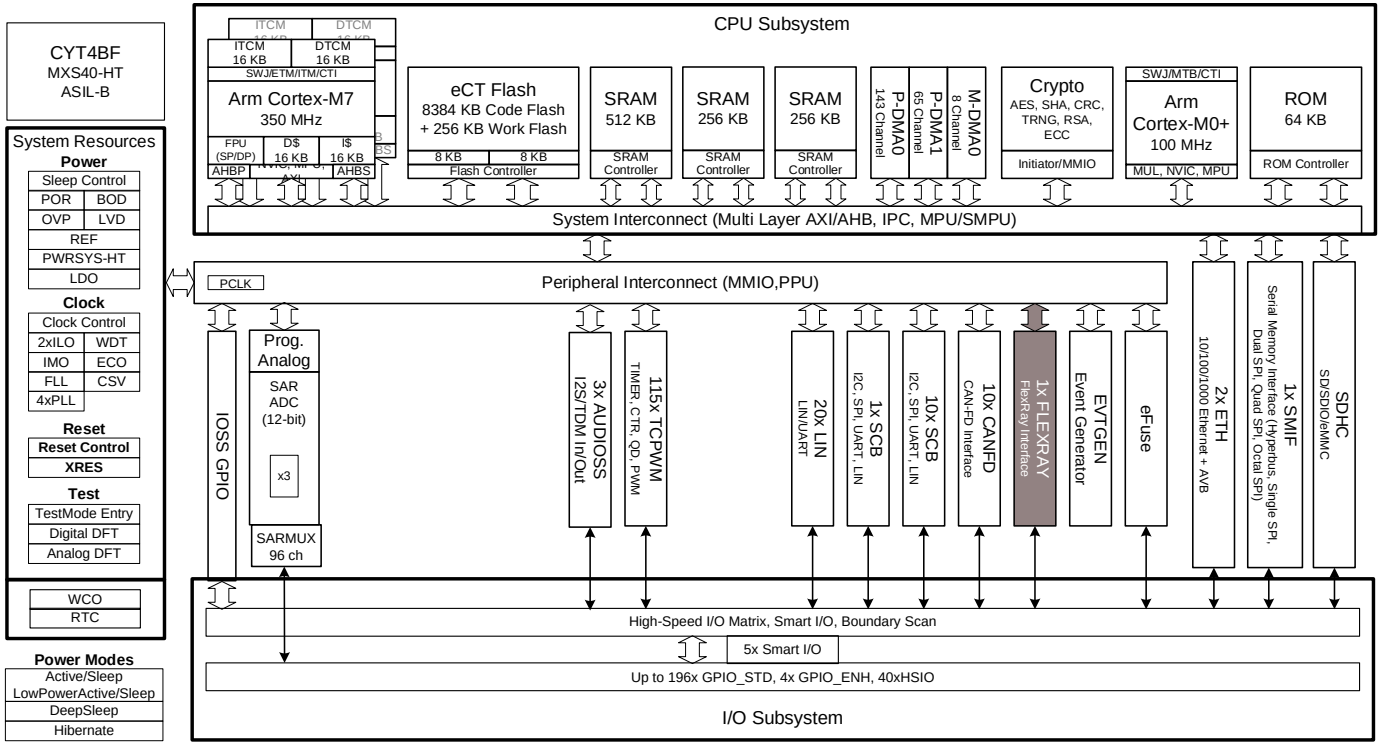
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller High	CYT4BF	Up to 8384KB

Introduction to Traveo II Body Controller High

- FlexRay is part of the Peripheral blocks



Hint Bar

Review TRM chapter 30 for additional details

FlexRay Overview

- FlexRay controller support is based on FlexRay protocol V2.1 Rev. A
- Features
  - Up to 10 Mbps per channel (supports A and B channels)
  - 8-KB total message buffer RAM
    - Up to 128 message buffers (approximately 16 bytes overhead per message)
    - Variable length data section, depending on number of buffers
    - Examples: 128 buffers with 48-bytes data; 30 buffers with 254-bytes data
    - Each message buffer is configurable as a reception buffer, transmission buffer, or as part of the reception FIFO
  - Host access to message buffers via input and output buffers
    - Input buffer: Holds messages to be transferred to the message RAM
    - Output buffer: Holds messages read from the message RAM
  - Filtering
  - Maskable interrupts

Hint Bar

Review the datasheet and TRM chapter 30 for additional details

Traveo II FlexRay Additional Features

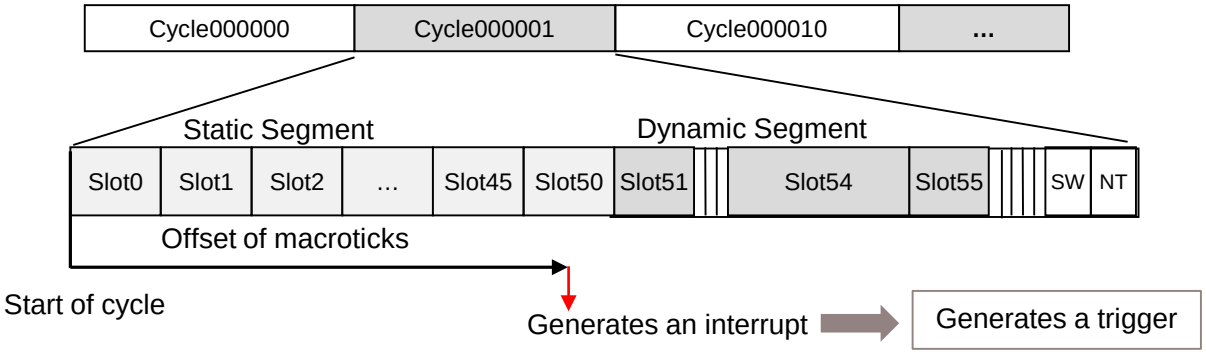
- Timer 0 Trigger
- Stop Watch Event Trigger
- DMA Trigger

Hint Bar

Review the Register TRM and TRM section 30.15 for additional details

Traveo II FlexRay Timer 0 Trigger

- Timer 0 Trigger Output
  - A pulse will be generated on tr_tint0_out when the timer 0 interrupt is asserted
- Timer 0
  - Timer 0 is an absolute timer in macroticks (MT)
  - Timer 0 setting
    - Start/stop setting
    - One execution/continuous execution setting
    - Cycle control to operate timer 0
    - Set number of offsets for MT

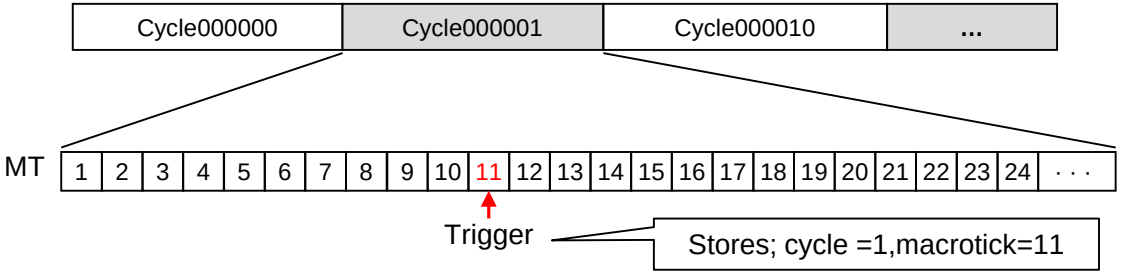


Hint Bar

Review TRM section 30.15 for additional details

Traveo II FlexRay Stop Watch Event Trigger

- Stop Watch Event Trigger Input
  - Stop watch trigger sources
    - Software Trigger
    - Interrupt Line 0 event (E-Ray INT0)
    - Interrupt Line 1 event (E-Ray INT1)
    - External Trigger (from Traveo II trigger mux)
  - Stop watch function
    - Stores the time that a specific event occurred
      - Cycle number
      - Macrotick (MT) value



Hint Bar

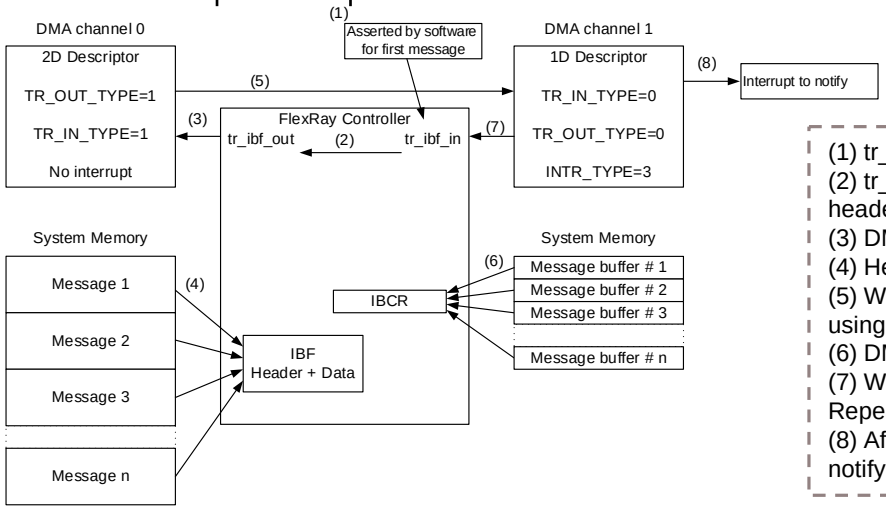
Review TRM section 30.15 for additional details

Traveo II FlexRay DMA Trigger

DMA Trigger Interface for Input Buffer Access

- Trigger input and output signals transfer data between the system memories and FlexRay controller message RAM via the input/output buffer using DMA controller

Signal	Direction	Description
tr_ibf_in	Input	Trigger input that indicates that the DMA transfer to write IBCR has completed.
tr_ibf_out	Output	Trigger output for triggering the DMA transfer from system memory to IBF.



(1) tr_ibf_in is asserted by software for first message
(2) tr_ibf_out requests DMA to transfer the message header/data from system memory to the IBF
(3) DMA ch.0 is triggered by tr_ibf_out
(4) Header and data sections of IBF are written
(5) When the transfer is complete, it triggers DMA ch.1 using the Traveo II trigger multiplexer
(6) DMA ch.1 is responsible for writing the IBCR
(7) When it is done, it asserts the tr_ibf_in trigger signal Repeat steps (2) to (7)
(8) After DMA ch.1 completes the write, interrupt to notify the application

Hint Bar

Review TRM section 30.15 for additional details

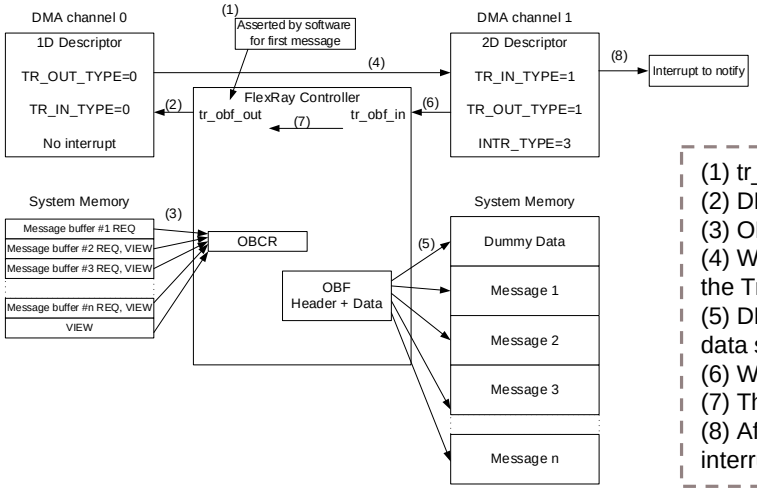
Input Buffer (IBF)

Input buffer command request (IBCR)

Traveo II FlexRay DMA Trigger

- DMA Trigger Interface for Output Buffer Access
  - Trigger input and output signals transfer data between the system memories and FlexRay controller message RAM via the input/output buffer using DMA controller

Signal	Direction	Description
tr_obf_in	Input	Trigger input that indicates that the DMA transfer from OBF to the system memory is complete.
tr_obf_out	Output	Trigger output for triggering the DMA transfer to write OBCR.



(1) tr_obf_out is asserted by software for first message
(2) DMA ch.0 triggered by tr_obf_out
(3) OBCR is written
(4) When the transfer is complete, it triggers DMA ch.1 using the Traveo II trigger multiplexer
(5) DMA ch.1 is responsible for transferring the header and data sections from the OBF to the system memory
(6) When it is done, it asserts the tr_obf_in trigger signal
(7) The tr_obf_out trigger signal is generated by the tr_obf_in
(8) After DMA ch.1 completes the transfer, it may raise an interrupt to notify the application

Hint Bar

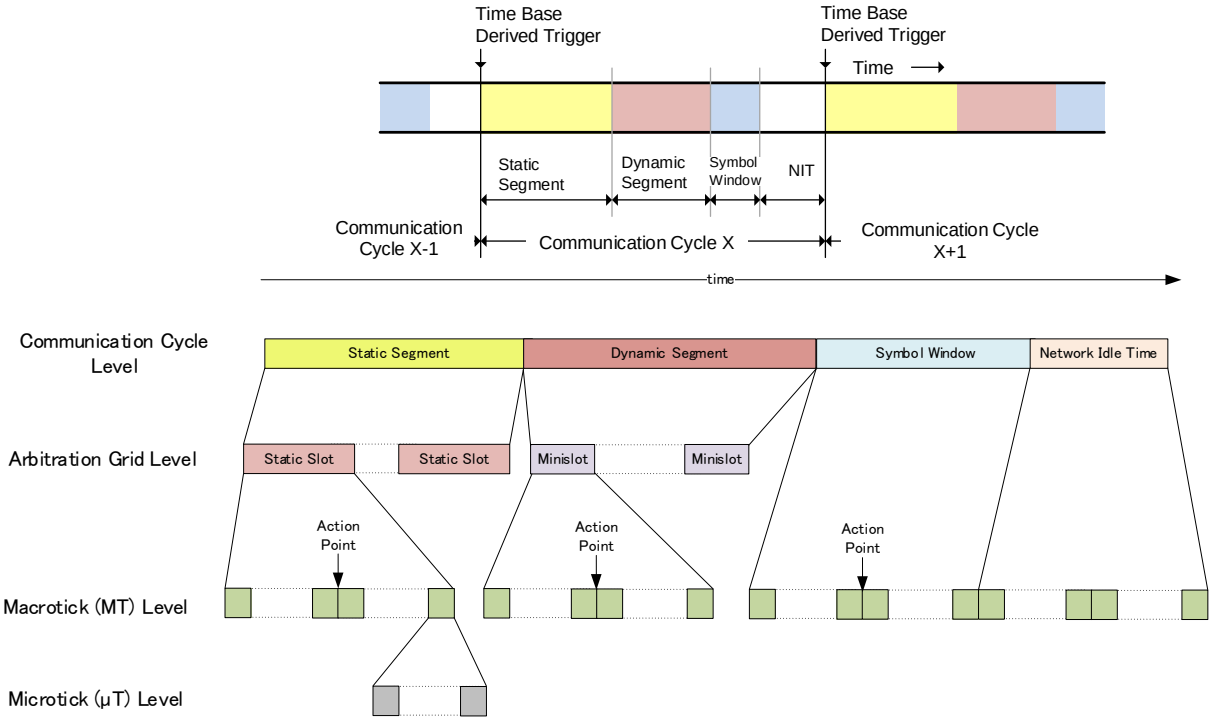
Review TRM section 30.15 for additional details

Output Buffer (OBF)

Output buffer command request (OBCR)

Appendix

Communication Cycle Structure

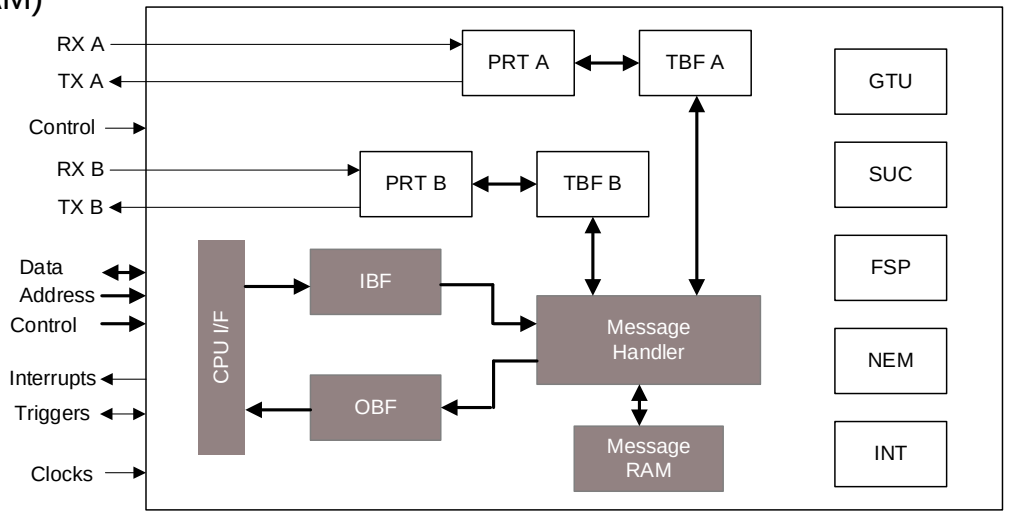


Hint Bar

Review the Register TRM and TRM section 30.15 for additional details

FlexRay Controller Block Diagram (1/3)

- FlexRay Controller Components
  - CPU I/F (CIF)
  - Input Buffer (IBF)
  - Output Buffer (OBF)
  - Message Handler (MHD)
  - Message RAM (MRAM)

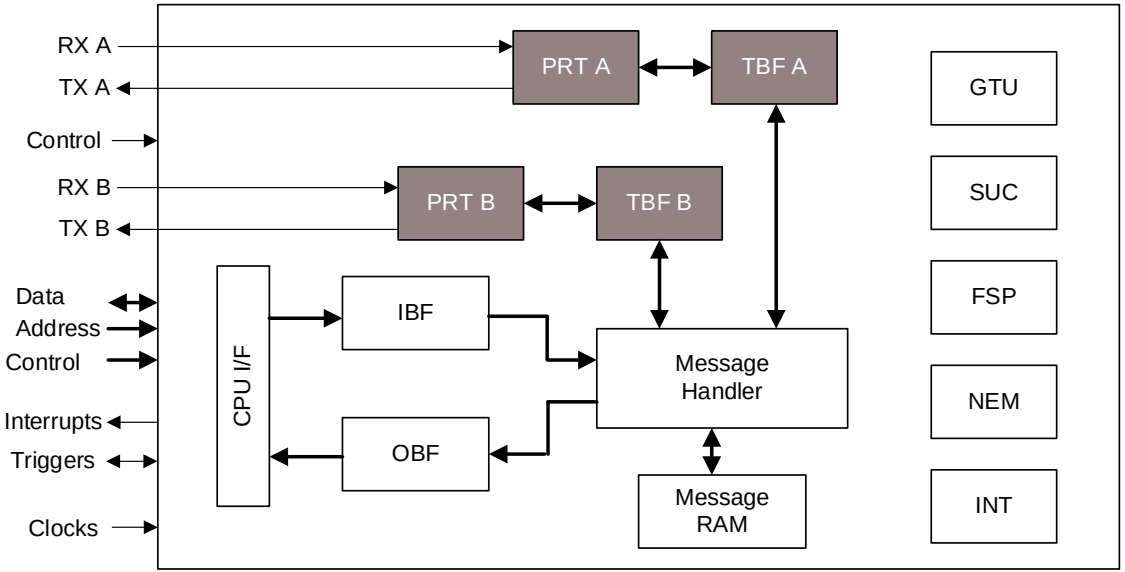


Hint Bar

Review TRM chapter 30 for additional details

FlexRay Controller Block Diagram (2/3)

- FlexRay Controller Components
  - Transient Buffer RAM (TBF A/B)
  - FlexRay Channel Protocol Controller (PRT A/B)

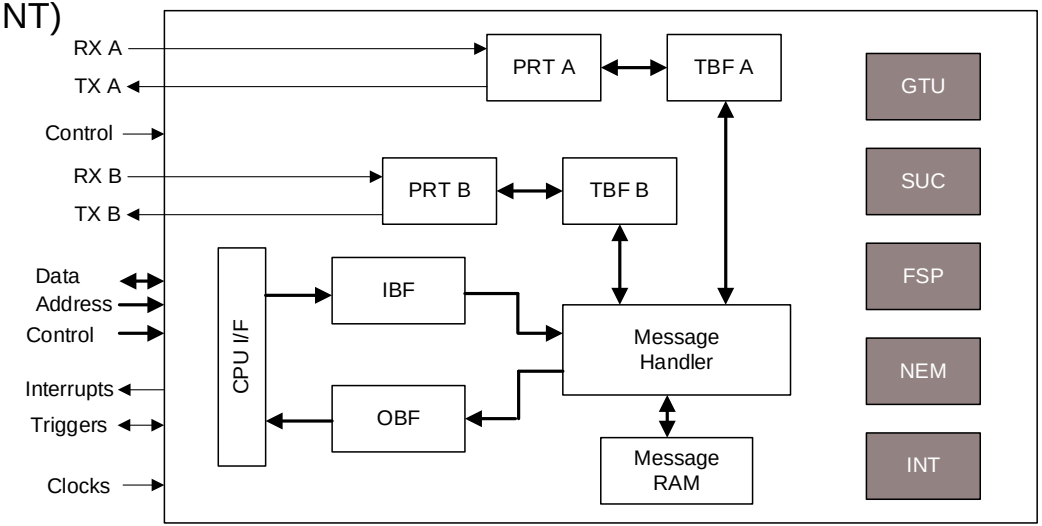


Hint Bar

Review TRM chapter 30 for additional details

FlexRay Controller Block Diagram (3/3)

- FlexRay Controller Components
  - Global Time Unit (GTU)
  - System Universal Control (SUC)
  - Frame and Symbol Processing (FSP)
  - Network Management (NEM)
  - Interrupt Control (INT)



Hint Bar

Review TRM chapter 30 for additional details

FlexRay Controller Components (1/4)

- FlexRay Controller Component Features:
  - CPU I/F (CIF): Connects the host CPU to the FlexRay controller
  - Input Buffer (IBF)
    - Used to write to the message buffers configured in the message RAM
    - Host CPU writes header and data sections for a specific message buffer to the input buffer
    - Message handler transfers data from the input buffer to the selected message buffer in the message RAM
  - Output Buffer (OBF)
    - Used to read the message buffers configured in the message RAM
    - Message handler transfers data from the selected message buffer to the output buffer
    - When the data transfer is complete, Host CPU can read the header and data sections of the transferred message buffer from the output buffer
  - Message Handler (MHD)
    - Acceptance filtering
    - Controls the data transfers between the following components:
      - Input/output buffer and message RAM
      - Transient buffer RAMs of the two FlexRay protocol controllers and message RAM
  - Message RAM (MRAM): Consists of a single-port RAM that stores configuration data (header and data) for up to 128 FlexRay message buffers

Hint Bar

Review TRM chapter 30 for additional details

FlexRay Controller Components (2/4)

- FlexRay Controller Component Features:
  - Transient Buffer RAM (TBF A/B)
    - Stores the data sections of two messages
  - FlexRay channel protocol controller (PRT A/B)
    - Consists of a shift register and FlexRay protocol finite state machine (FSM)
    - Functions:
      - Checks and controls bit timings
      - Receives and transmits FlexRay frames and symbols
      - Checks the header CRC
      - Generates and checks the frame CRC
      - Connects to the bus driver

Hint Bar

Review TRM chapter 30 for additional details

FlexRay Controller Components (3/4)

- FlexRay Controller Component Features
  - Global Time Unit (GTU)
    - Microtick generation
    - Macrotick generation
    - Fault-tolerant clock synchronization using the Fault Tolerant Midpoint (FTM) algorithm for rate correction and offset correction
    - Cycle counter
    - Static segment timing control
    - Dynamic segment (minislot) timing control
    - Support for external clock correction
  - System Universal Control (SUC)
    - Configuration
    - Wakeup
    - Startup
    - Normal operation
    - Passive operation
    - Monitor mode

Hint Bar

Review TRM chapter 30 for additional details

FlexRay Controller Components (4/4)

- FlexRay Controller Component Features
  - Frame and Symbol Processing (FSP)
    - Controls the following functions:
      - Ensuring that the timing of frames and symbols is correct
      - Testing the syntactic and semantic validity of received frames
      - Setting the slot status flags
  - Network Management (NEM)
    - Handles the network management vector
  - Interrupt control (INT)
    - Functions:
      - Providing error and status interrupt flags
      - Enabling and disabling interrupt factors
      - Controlling the allocation of interrupt factors to the two module interrupt lines
      - Enabling and disabling module interrupt lines
      - Managing two interrupt timers
      - Capturing the Stop Watch time

Hint Bar

Review TRM chapter 30 for additional details

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6410080	12/12/2018	Initial release
*A	7036601	12/01/2020	Updated to Infineon format