Customer training workshop

TRAVEO™ T2G Body Entry Clock System

Q4 2021

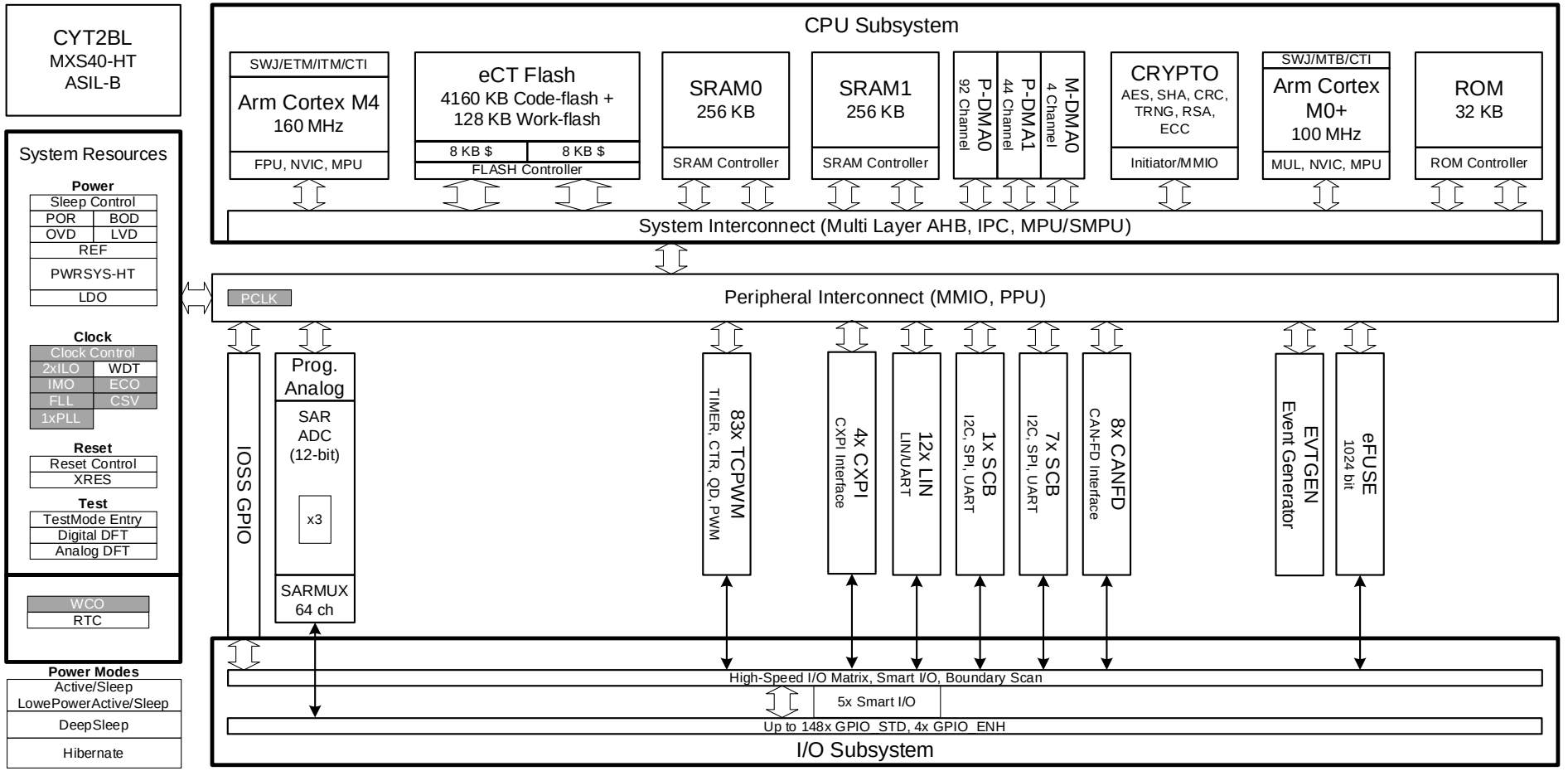
Target products

› Target product list for this training material:

Family category	Series	Code flash memory size
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B6	Up to 576 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2BL	Up to 4160 KB

Introduction to CYT2BL

› The clock system is part of the System Resources block



Hint Bar

Review Chapter 18 in the TRM for additional details

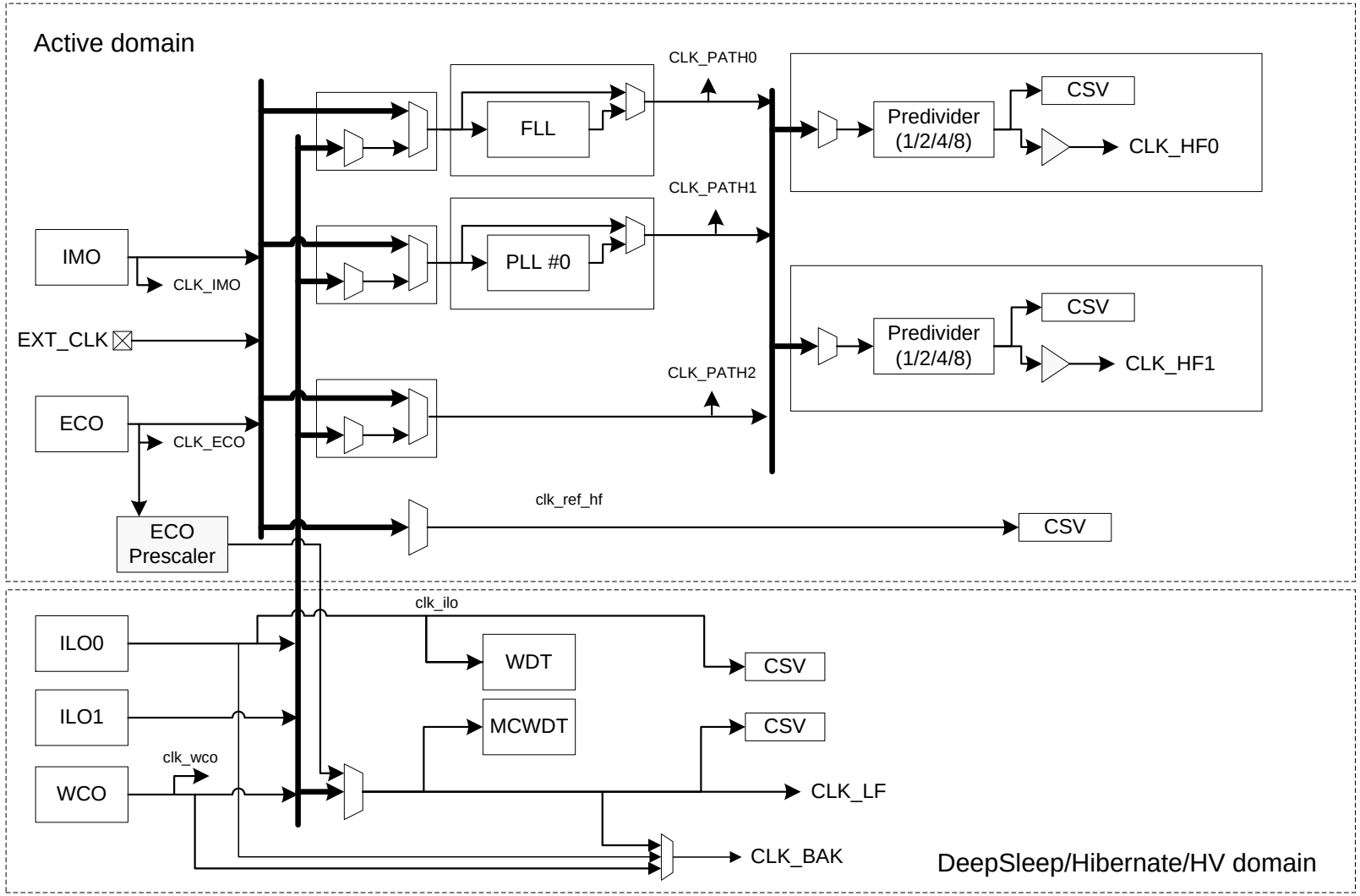
Clock system overview

- The clock system supplies clocks for MCU operation
- Features
  - Internal clock sources
    - 8-MHz IMO
    - 32.768-kHz ILO0/1
  - External clock sources
    - External crystal oscillator (ECO)
    - Watch crystal oscillator (WCO)
    - External clock (EXT_CLK) generated using a signal through I/O pin
      It is also possible to output the internal clock
  - Clock generation
    - Phase lock loop (PLL)
    - Frequency lock loop (FLL)
- Clock supervision (CSV) for detecting clock abnormality
- Clock calibration counter

Hint Bar

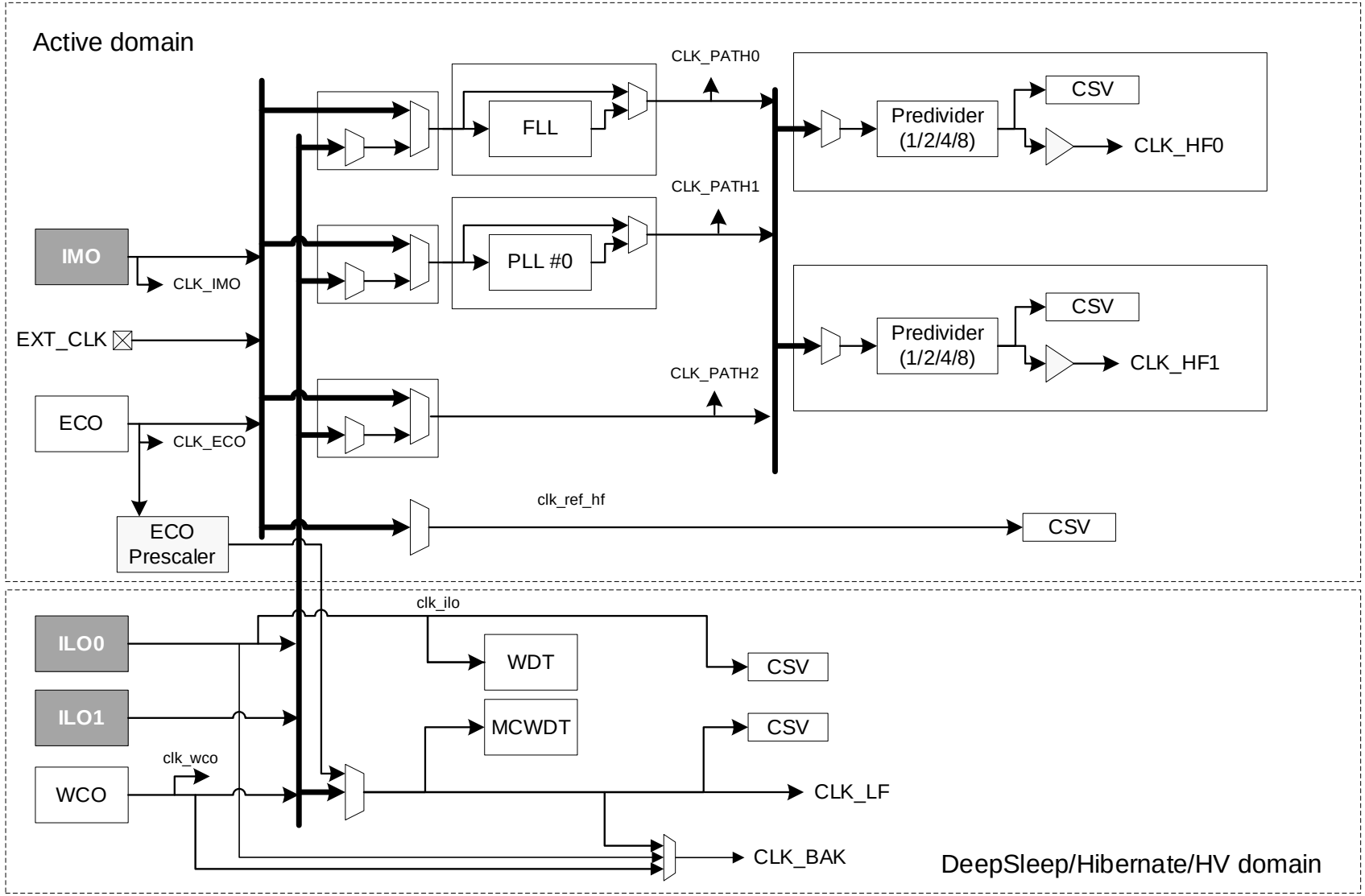
Review Chapter 18 in the TRM for additional details

Clock system block diagram



Internal clock sources

- Internal main oscillator (IMO)
- Internal low-speed oscillator 0/1 (ILO0/1)



IMO: Internal main oscillator

- Produces an 8-MHz fixed frequency
- An accurate, high-speed internal (crystal-less) oscillator
- Available in only Active and Sleep modes
- Default clock source after POR or any other reset
- Used by PLL0 to generate a wide range of high-frequency clocks
- Enabled and disabled by register[1]
  - Default is ENABLE[2]

Hint Bar

Review Section 18.2 in the TRM for additional details

Refer to the datasheet for additional details on AC specifications

[1] IMO should not be disabled if it is the source of the clock path to CLK_HF[0]
[2] Refer to the Register TRM (CLK_IMO_CONFIG) for additional details

ILO 0/1: Internal low-speed oscillators

- ILO0
  - Produces a 32.768-kHz nominal fixed frequency
  - Low power and low accuracy
  - Available in all power modes
  - Always the source of the Watchdog timer[1]
- ILO1
  - Used for ILO0 clock monitoring
  - Parameters for ILO1 are the same as ILO0

Hint Bar

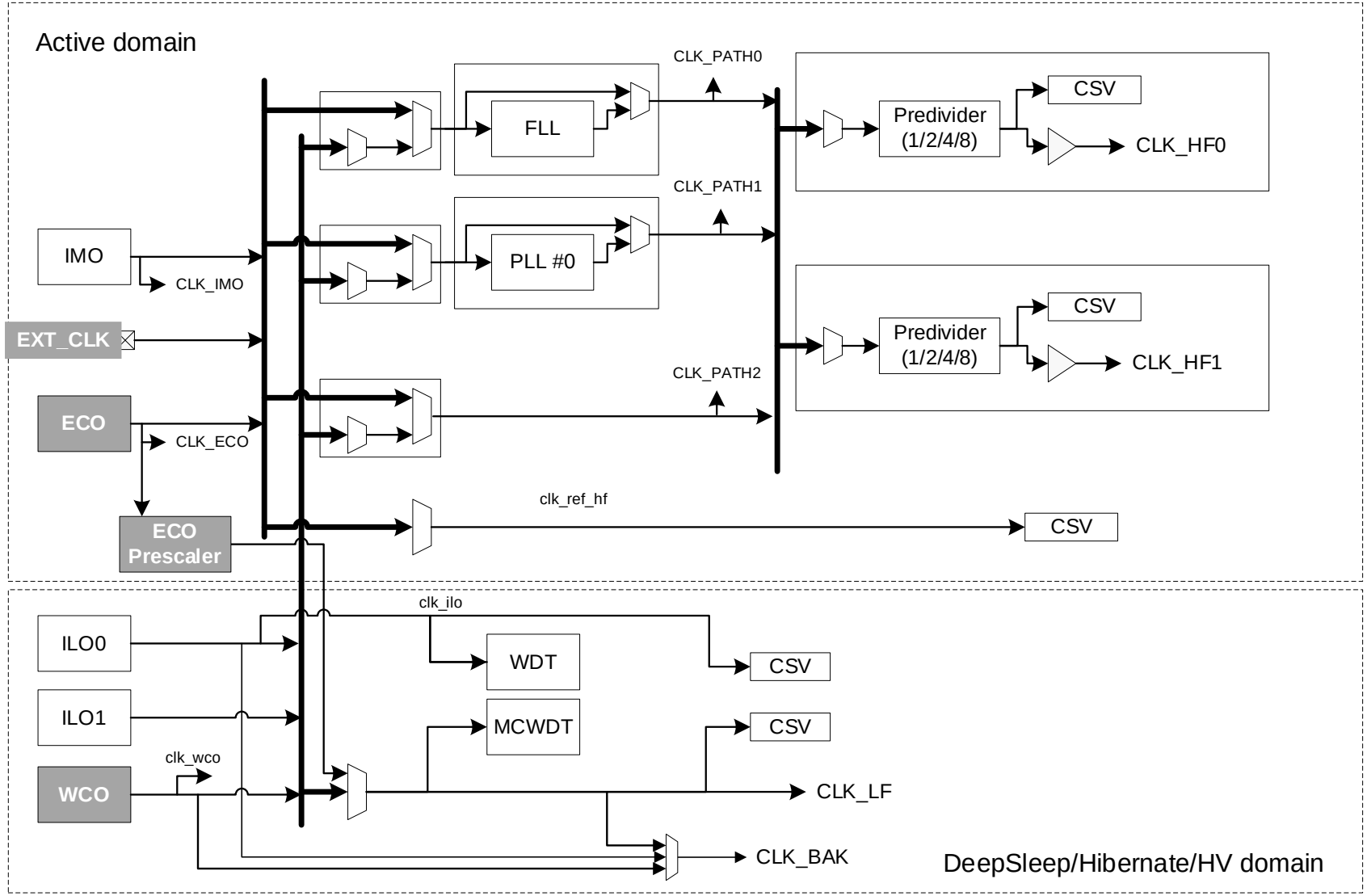
Review Section 18.2 in the TRM for additional details

Refer to the datasheet for additional details on AC specification

[1] Always leave the ILO enabled, as it is the source of the Watchdog timer

External clock sources

- ECO
- WCO
- EXT_CLK



External clock sources overview

- ECO
  - Contains an oscillator to drive an external 3.988 MHz to 33.34 MHz crystal
  - Used by PLL0 to generate a wide range of high-frequency clocks
  - ECO pre-scaler
  - ECO trimming
  - Enabled and disabled by register[1]
    - Default is DISABLE
- WCO
  - Highly accurate 32.768-kHz clock source
  - Primary clock source for the real-time clock (RTC)
  - Enabled and disabled by register[2]
    - Default is DISABLE
- EXT_CLK
  - 0.25 MHz to 80 MHz clock that can be sourced from a designated I/O pin
  - Can be used as the source clock for either the PLL or FLL
  - Can be used to output the internal clock (CLK_HF1 is available)
  - When using a pin as an input to EXT_CLK, I/O must be set appropriately[3]

Hint Bar

Review Section 18.2 in the TRM for additional details

Refer to the datasheet for additional details on AC specification

[1] Refer to the Register TRM (CLK_ECO_CONFIG) for additional details
[2] Refer to the Register TRM (CTL) for additional details
[3] Refer to the TRM section 18.2.3 and the datasheet for additional details

ECO trimming

- ECO supports a wide variety of crystals and ceramic resonators
- ECO can be configured by register[1]
  - The following trim bit fields can be configured to control the maximum peak oscillation voltage across the crystal (VP), the transconductance (gm), and the nominal frequency (f):
    - ATRIM (Amplitude Trim by AGC)
    - GTRIM (Gain Trim)
    - WDTRIM (Watchdog Trim)
    - FTRIM (Filter Trim)
    - RTRIM (Feedback Resistor Trim)

$$Max\ peak\ value:\ V_P = \frac{\sqrt{\frac{D_L}{2ESR}}}{\pi f (C_0 + C_L)}$$

f: Fundamental frequency of the crystal (XTAL)

D_L: Maximum drive level of XTAL

ESR: Equivalent series resistance

C_0: Shunt capacitance of XTAL

C_L: Parallel load capacitance of XTAL

$$Transconductance:\ g_m > 20 \times ESR \times (2\pi \times f)^2 \times (C_0 + C_L)^2$$

$$Negative\ resistance:\ |R_{neg}| = \frac{g_m \times 4 \times C_L^{\,2}}{(2\pi \times f)^2 \times (4 \times C_L^{\,2} + 4 \times C_L \times C_0)^2}$$

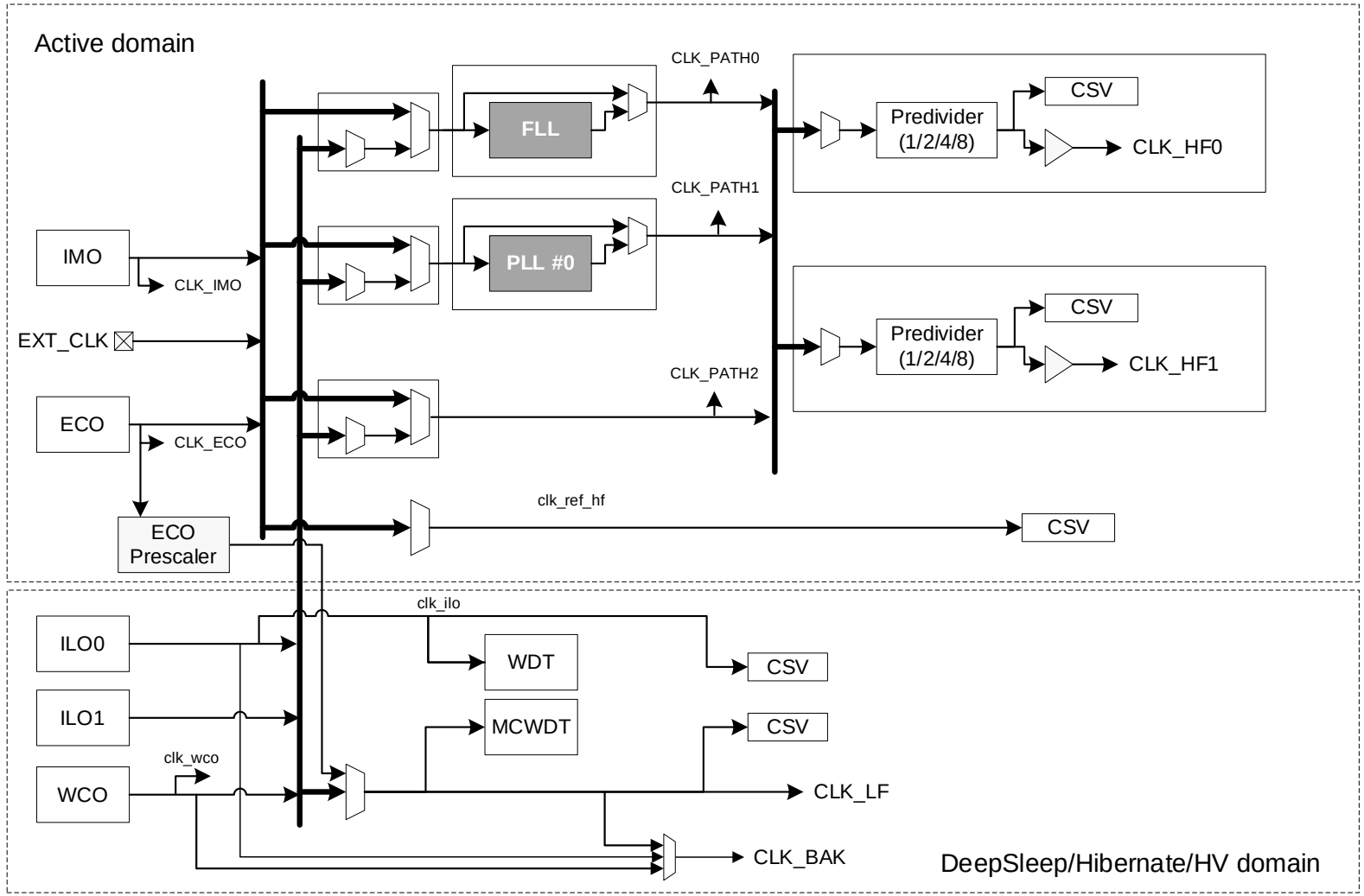
Hint Bar

Review TRM section 18.2 for additional details

[1] Refer to the Register TRM (CLK_ECO_CONFIG2) for additional details.

High-speed clock generation

- Phase lock loop (PLL)
- Frequency lock loop (FLL)



Clock generation: PLL and FLL

- PLL
  - Input clock can be IMO (8 MHz), ECO, or EXTCLK
  - PLL configuration parameters:
    - Input clock range: 3.988 to 33.34 MHz
    - Output clock range: 11 to 160 MHz (CYT2BL)[1]
- FLL
  - Input clock can be IMO (8 MHz), ECO, or EXTCLK
  - A counter with a current-controlled oscillator (CCO)
    - Starts up (locks) faster and uses lower power than the PLL
    - The lock tolerance is user adjustable
  - Parameters on the FLL configuration:
    - Input clock range: 0.25 MHz to 80 MHz
    - Output clock range: 24 MHz to 100 MHz (CYT2BL)[1]

Hint Bar

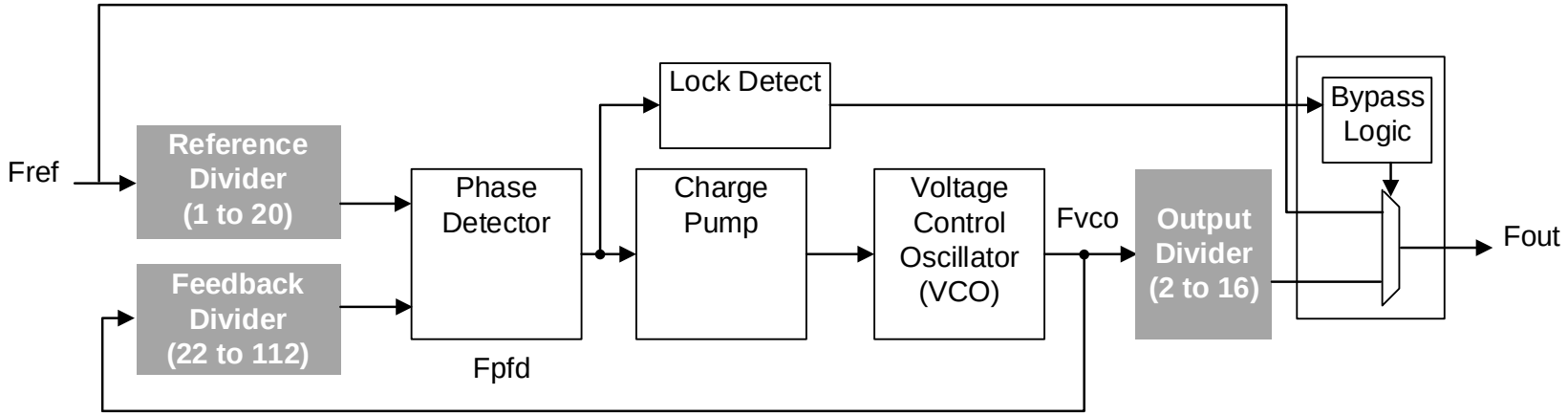
Review Section 18.3 in the TRM and Register TRM for additional details

Refer to the datasheet for additional details on AC specification

[1] Refer to the data sheet for target product.

PLL configuration example

- Parameters on PLL configuration:
- Fref: 3.988 MHz to 33.34 MHz
- Fout (Fvco/Output divider): 11 MHz to 160 MHz (CYT2BL)[1]
- Fpfd (Fref/Reference divider): 4 MHz to 8 MHz
- Fvco (Fpfd * Feedback divider): 170 MHz to 400 MHz



	Fref	Fout	Fpfd	Fvco
Frequency	8 MHz	160 MHz = Fvco/2	4 MHz = Fref/2	320 MHz = Fpfd x 80
Divider Setting	-	Output Divider: 2	Reference Divider: 2	Feedback Divider: 80

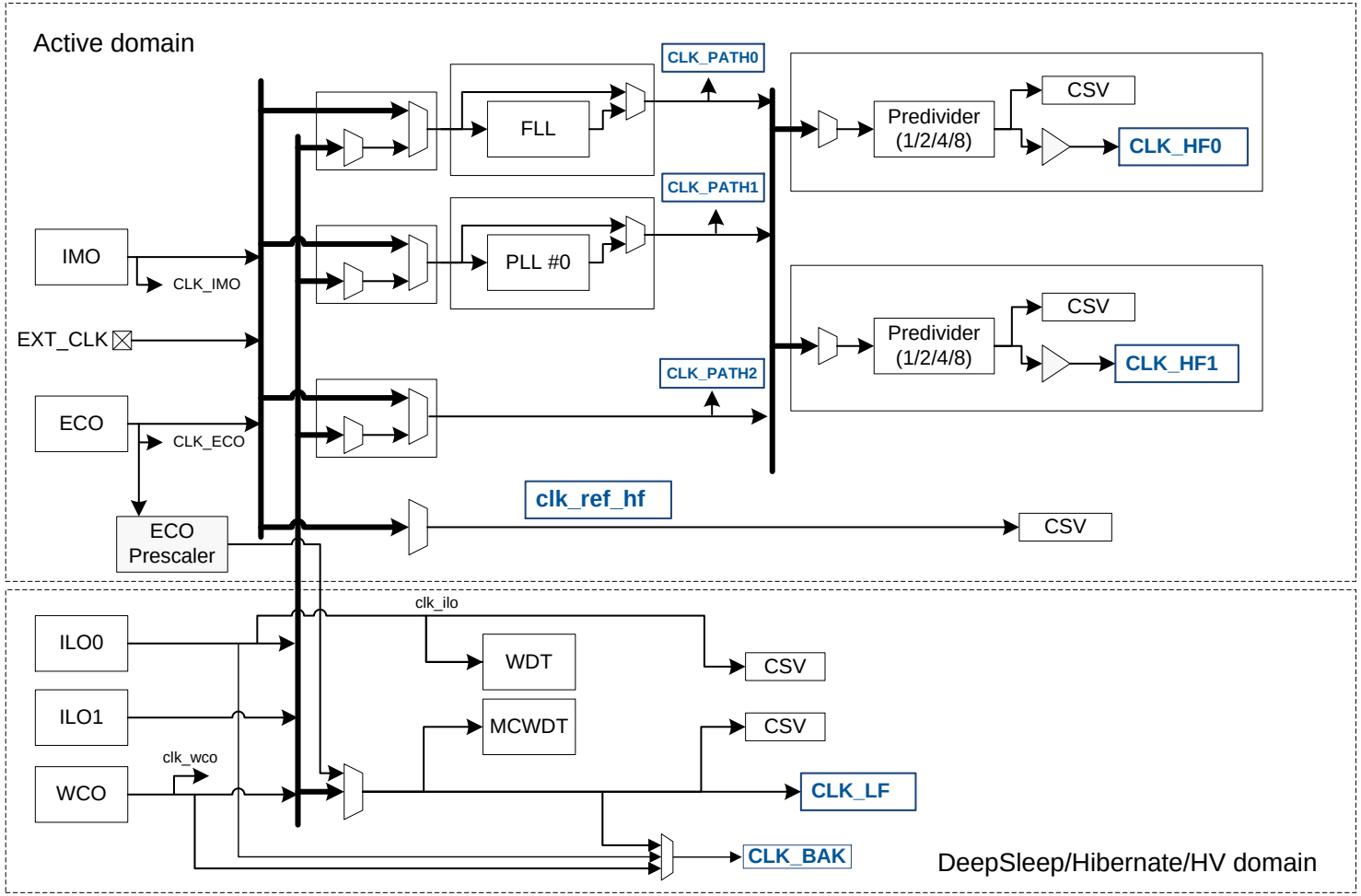
[1] Refer to the data sheet for target product.

Hint Bar

Review section 18.3.1 in the TRM and Register TRM for additional details

Clock trees

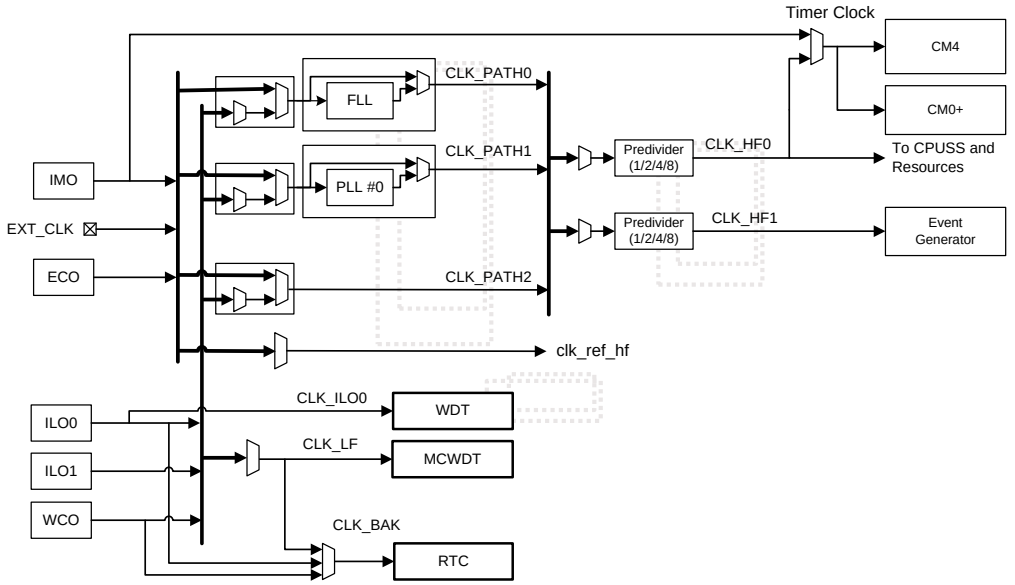
- CLK_PATH0/1/2
- CLK_HF0/1
- clk_ref_hf
- CLK_LF
- CLK_BAK
- CLK_HF0 distribution



Clock distribution

- CLK_PATHx
  - Input sources for the CLK_HF roots
  - CLK_PATH0 contains the FLL output
    Up to 100 MHz (using FLL)[1]
  - CLK_PATH1 contains the PLL output
    Up to 160 MHz (using PLL)[1]
  - CLK_PATH2 is a connection to root clocks
    Up to 33.34 MHz (using ECO)
- CLK_REF_HF
  - Selects IMO, ECO, EXTCLK
  - Typically selects the IMO (8 MHz)
  - Used as a reference clock for CLK_HF0/1 clock supervision

- CLK_HF0/1
  - Selects CLK_PATH0, 1, 2
  - CLK_HF0 is the input source for the CPUSS and resources such as Timer, SCB, and SAR ADC
  - CLK_HF1 is the input source for the event generator



Hint Bar

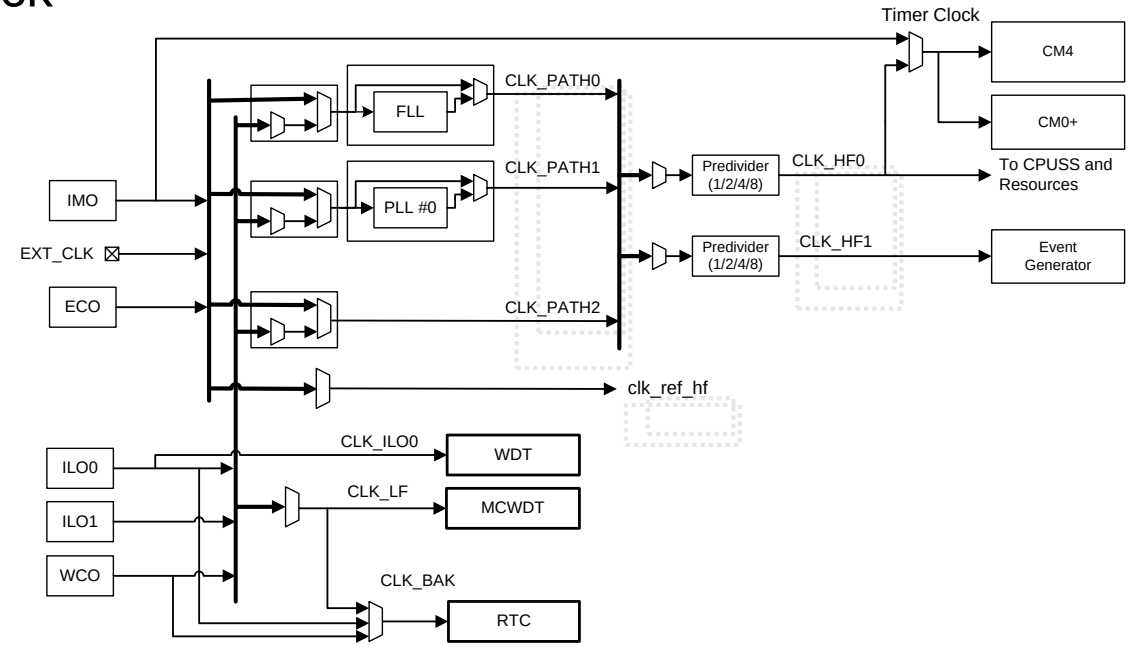
Training section reference:

- CPU Subsystem

[1] Refer to the data sheet for target product.

Clock distribution

- CLK_LF
  - ILO0, ILO1, or WCO (32.768 kHz) can be the input clock for CLK_LF
  - Input sources for the MCWDT clock
  - Uses reference clock for CLK_ILO0 Clock Supervision
- CLK_BAK
  - ILO0, ILO1, or WCO (32.768 kHz) can be the input clock for CLK_BAK
  - Input sources for RTC[1] clock



[1] Typically WCO is connected to RTC. CLK_LF also can connect to RTC.

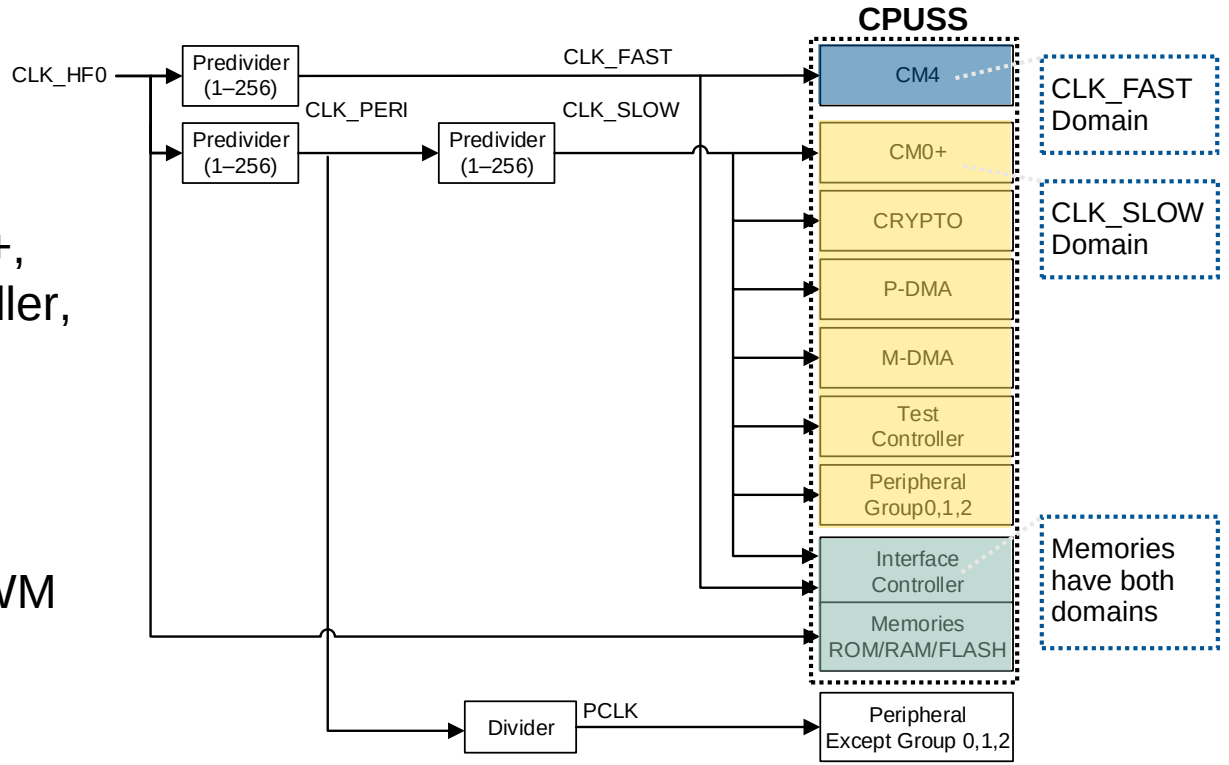
Hint Bar

Training section reference:

- CPU Subsystem

CLK_HF0[1] distribution

- The root clock for the CPUSS and the peripherals
- Distributed to CLK_FAST, CLK_SLOW, and CLK_PERI
- CPUSS has CLK_FAST and CLK_SLOW domains
- CLK_FAST
  - Source clock for CM4
  - Up to 160 MHz[2]
- CLK_SLOW
  - Source clock for the CM0+, Crypto, DMAs, test controller, some peripherals[3]
  - Up to 100 MHz[2]
- CLK_PERI
  - Source clock for all peripherals such as TCPWM and SCB, via divider
  - Up to 100 MHz[2]



Hint Bar

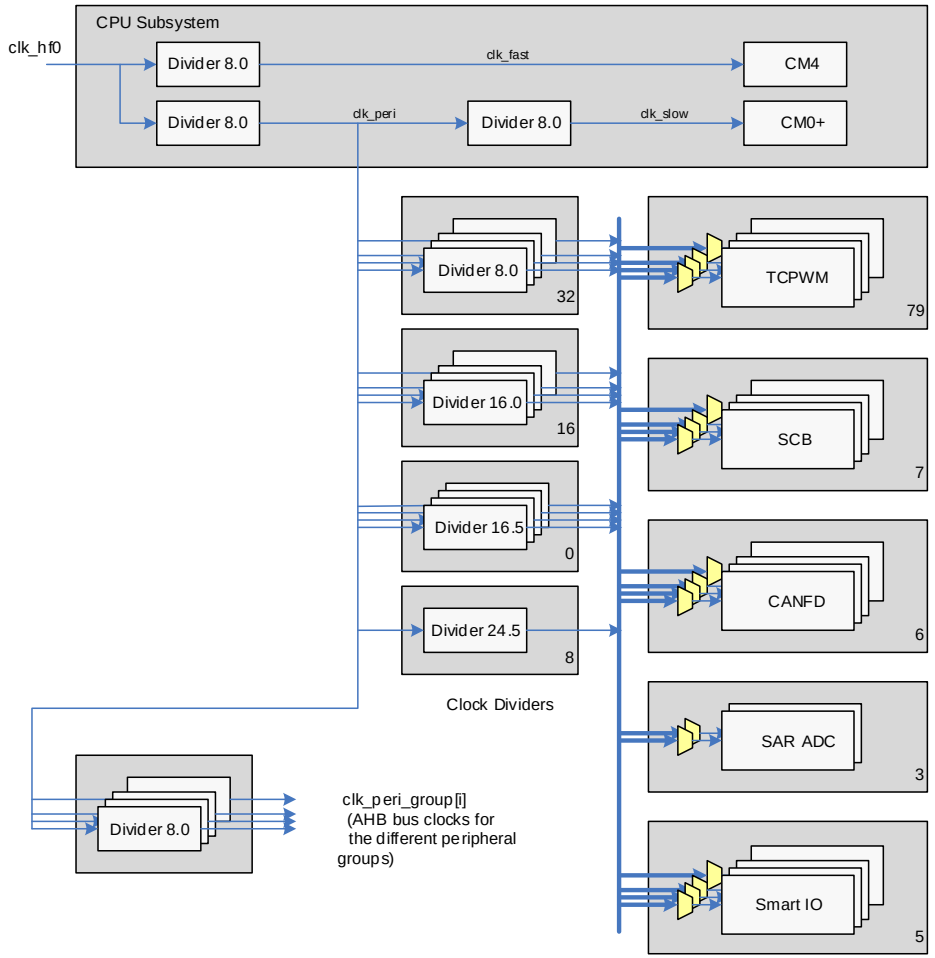
Training section references:

- CPU Subsystem

[1] CLK_HF0 can be enabled and disabled by register. CLK_HF0 is always enabled as the clock source of CPU.
[2] Refer to the data sheet for target product.
[3] CPUSS and PPU registers

Peri clock distribution

- PERI clock divider
  - Four types of dividers[1]
    - 8-bit divider
    - 16-bit divider
    - 16.5-bit divider
    - 24.5-bit divider
  - Fractional clock dividers supported
  - Output of dividers can be routed to any peripheral
  - Phase aligning
    - Can be phase-aligned with any of the other (enabled) clock dividers.



Hint Bar

Clock dividers can be configured through the following registers:

DIV_8_CTL

DIV_16_CTL

DIV_16_5_CTL

DIV_24_5_CTL

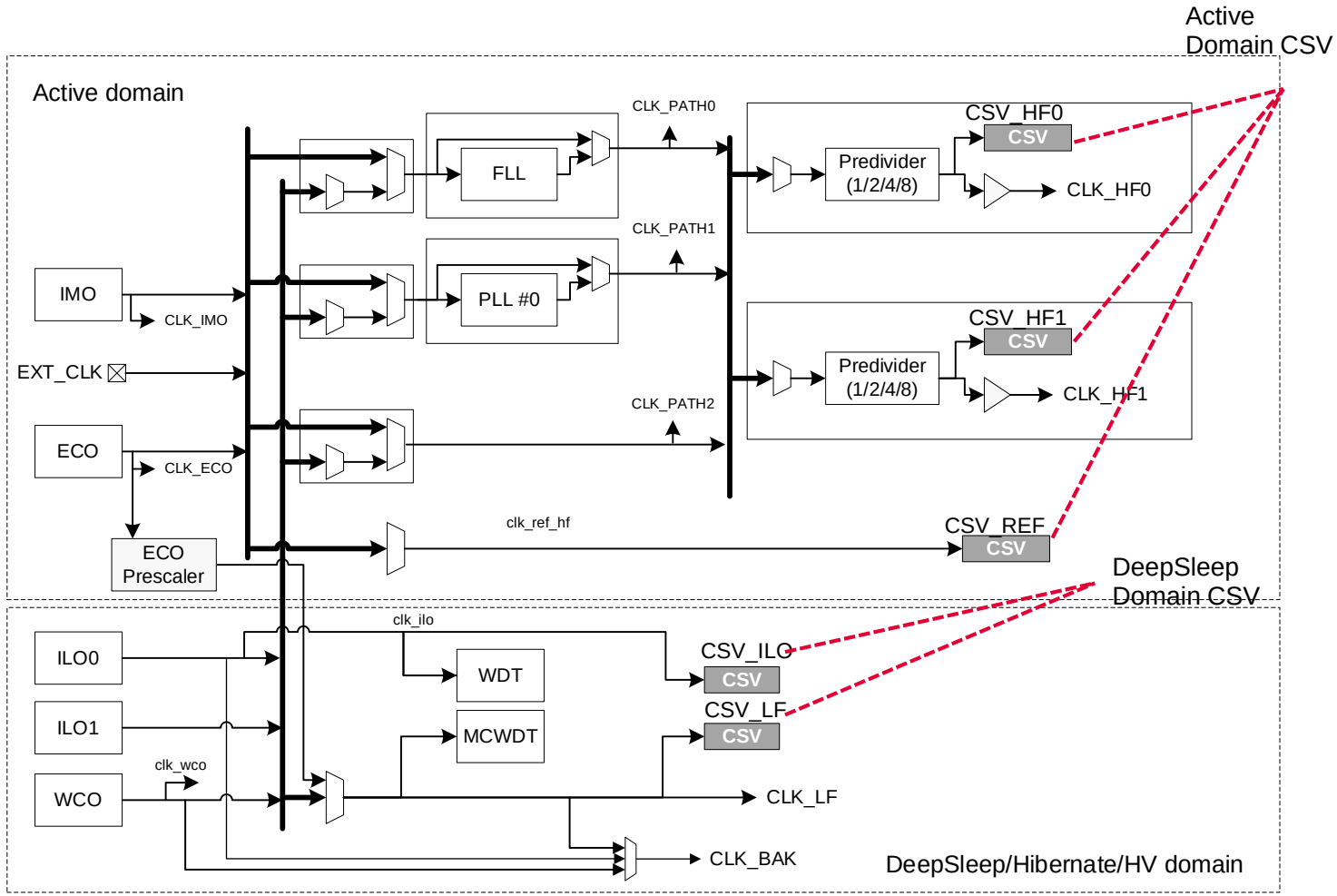
Clock Enable multiplexers can be configured through CLOCK_CTL registers, which are assigned for each peripheral

Review Section 18.7 in the TRM for additional details on clock numbers, which are assigned for each peripheral

[1] Not all dividers are supported

Clock supervision (CSV)

- Clock supervision (CSV) allows one clock to be monitored with another clock (reference clock)
- Monitored clock sources:
  - CLK_HF0
  - CLK_HF1
  - CLK_REF_HF
  - ILO0
  - CLK_LF
- CSV power domains:
  - Active domain CSV
  - DeepSleep domain CSV

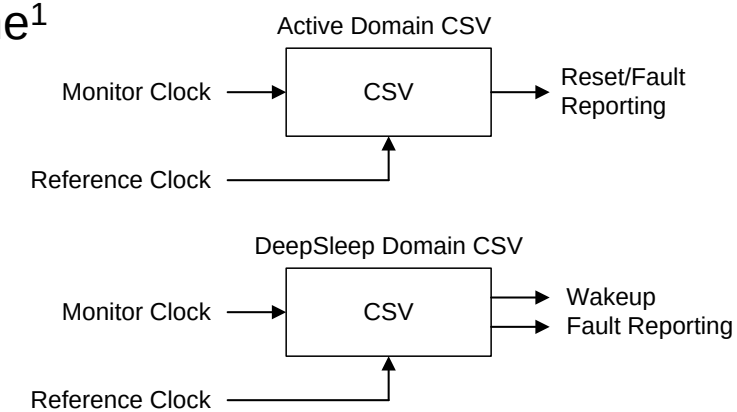


Clock supervision features

- Checks that the frequency of the monitored clock is within the allowed frequency window
  - Uses a reference clock to supervise the behavior of the monitor clock

CSV Components	Monitor Clock	Reference Clock	Note
CSV_HF0/1	CLK_HF0/1	clk_ref_hf	clk_ref_hf is typically selected the IMO (default)
CSV_REF	clk_ref_hf	ILO0	–
CSV_ILO	ILO0	CLK_LF	CLK_LF is selected WCO or ILO1
CSV_LF	CLK_LF	ILO0	–

  - Active domain CSV: CSV_HF0/1, CSV_REF
    - Automatically stops during DeepSleep, and restarts by wakeup
    - Wait function of monitoring start for startup time[1]
    - Possible to generate a Reset or a Fault report
  - DeepSleep domain CSV: CSV_ILO, CSV_LF
    - Operates during Active and DeepSleep
    - Generates Wakeup and Fault reports
  - All CSVs are initially OFF



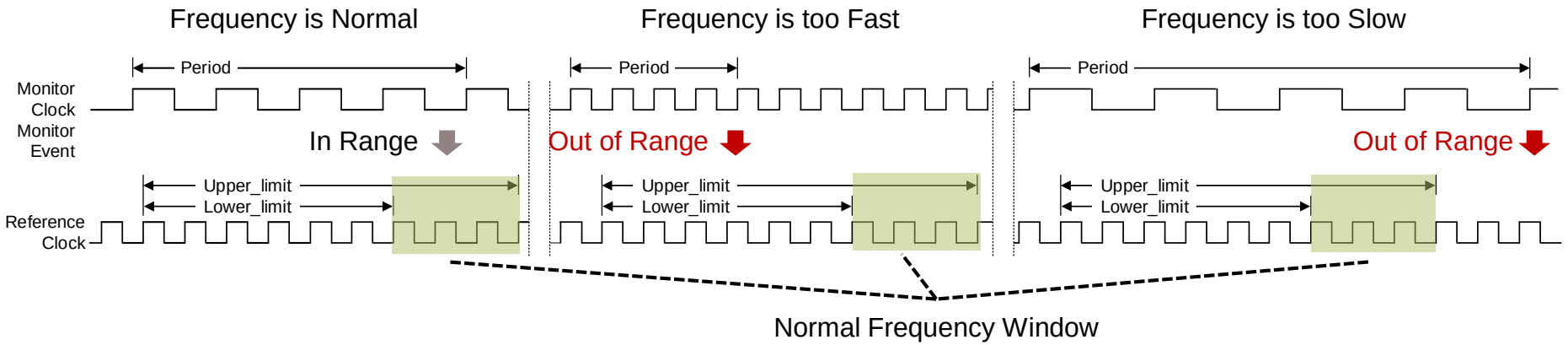
[1] Need to prevent a false error detection at startup

Hint Bar

See the Register TRM for additional details

CSV operation

- The monitored clock generates a monitor event (Period), and the reference clock generates a lower and upper limit
- The monitor event is compared against a lower limit/upper limit
- An error is reported if the monitor event ≤ lower limit, or if the monitor event > upper limit



- Advantages
  - Detects whether the clock stops, runs too fast or runs too slow, and if the period is not within the frequency window
  - Monitors clock in each power mode such as Active, Sleep, and DeepSleep with Active domain CSV and DeepSleep domain CSV
  - Can achieve ASIL-B

Hint Bar

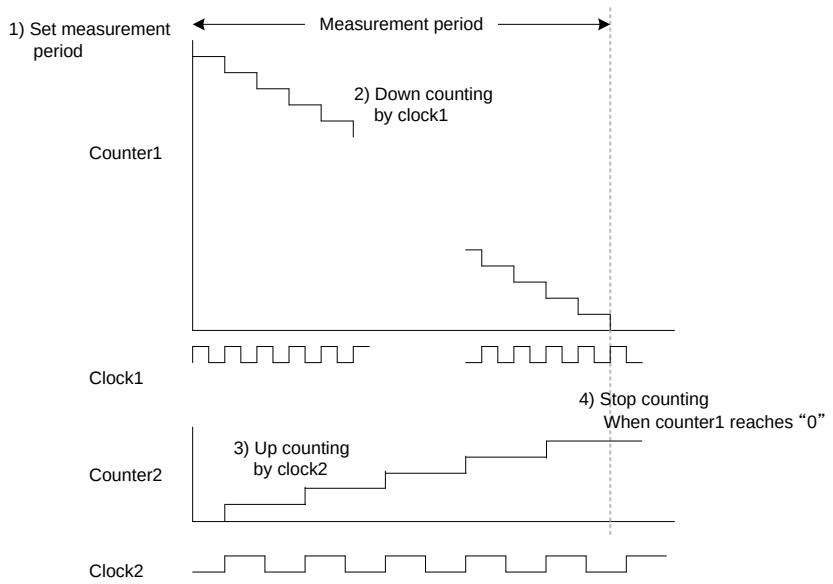
The monitor clock and the reference clock are asynchronous (typical). Therefore, the frequency window needs to account for maximum clock tolerance.

Clock calibration counter

- Clock calibration counter operation
  - Two counters: Counter1 and Counter2
    - Counter1 is clocked by clock1: reference clock
    - Counter2 is clocked by clock2: measurement clock.
  - Counter1 sets the measurement period by the count number of clock1
  - Counter2 indicates the count number of clock2 during the measurement period
  - Clock2 frequency can be calculated from the following formula using two count numbers:

$$\text{clock2frequency} = \frac{\text{Counter2value}}{\text{Counter1value}} \times \text{clock1frequency}$$

  - All clock sources are available as a source for these two clocks.
- Use case
  - Measure a lower-accuracy clock, such as the ILO, using a higher-accuracy clock such as the ECO



Hint Bar

Review Section 18.8 in the TRM for additional details

Count Clock1, 2 can be selected through registers:

CLK_OUTPUT_FAST

Appendix

Comparison Between CYT2BL, CYT4BF, and CYT4DN (1/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
IMO		Supported			
ECO		Supported			
ILO 0		Supported			
ILO 1		Supported			
WCO		Supported			
LPECO		Not implemented		Supported	
FLL	Number of FLL	1			
	Input Range	0.25 to 80 MHz		0.25 to 100 MHz	
	Output Range	24 to 100 MHz			
PLL	Number of PLL	1	2	3	
	Input Range	3.988 to 33.34 MHz			
	Output Range	11 to 160 MHz	11 to 200 MHz		
PLL400	Number of PLL	Not implemented	2	5	
	Input Range	Not implemented	3.988 to 33.34 MHz		
	Output Range	Not implemented	25 to 350 MHz (*)	25 to 400 MHz	(*) Spreading off
	SSCG	Not implemented	Yes		
	Fractional Operation	Not implemented	Yes		

Comparison Between CYT2BL, CYT4BF, and CYT4DN (2/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
CLK Trees Source Clock	CLK_PATH 0	FLL			
	CLK_PATH 1	PLL	PLL400		
	CLK_PATH 2	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL400		
	CLK_PATH 3	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL	PLL400	
	CLK_PATH 4	Not implemented	PLL	PLL400	
	CLK_PATH 5	Not implemented	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL400	
	CLK_PATH 6	Not implemented		PLL	
	CLK_PATH 7	Not implemented		PLL	
	CLK_PATH 8	Not implemented		PLL	
	CLK_PATH 9	Not implemented		ECO,IMO,EXT_CLK,WCO, ILO0/1,LPECO	
	CLK_REF_HF	ECO,IMO,EXT_CLK		ECO,IMO,EXT_CLK ,LPECO	
	CLK_TIMER	CLK_HF0, IMO	IMO		
	CLK_LF	ILO0/1, WCO, ECO		ILO0/1, WCO, ECO ,LPECO	
	CLK_BAK	CLK_LF, ILO0, WCO		CLK_LF, ILO0, WCO ,LPECO	

Comparison between CYT2BL, CYT4BF, and CYT4DN (3/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
CLK Distribution	CLK_HF0	CPUSS clocks, PERI, and AHB infrastructure	CPUSS (Memories, CLK_SLOW, Peripherals)	CPUSS (Memories, CLK_SLOW, Peripherals)	
	CLK_HF1	Event Generator	CPUSS (Cortex-M7 CPU 0, 1)	CPUSS (Cortex-M7 CPU 0, 1)	
	CLK_HF2	Not connect	CAN FD, FlexRay, LIN, TCPWM, SCB, SAR	CAN FD, CXPI, LIN, SCB, SAR	
	CLK_HF3	Not implemented	Event Generator	Event Generator	
	CLK_HF4	Not implemented	Ethernet	Ethernet	
	CLK_HF5	Not implemented	Audio subsystem	Sound Subsystem #0	
	CLK_HF6	Not implemented	SDHC Interface, SMIF	Sound Subsystem #1	
	CLK_HF7	Not implemented	Not connect	Sound Subsystem #2	
	CLK_HF8	Not implemented	Not implemented	SMIF #0	
	CLK_HF9	Not implemented	Not implemented	SMIF #1	
	CLK_HF10	Not implemented	Not implemented	Video Subsystem	
	CLK_HF11	Not implemented	Not implemented	Video Display #0	
	CLK_HF12	Not implemented	Not implemented	Video Display #1	
	CLK_HF13	Not implemented	Not implemented	Not connect	

Comparison between CYT2BL, CYT4BF, and CYT4DN (4/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
Clock Divider	Number of Dividers	1	2		
	Fractional Clock Divider	24.5-bit dividers		16.5-bit dividers, 24.5-bit dividers	
	Phase Aligning	Supported			
Clock Supervision		Supported			
Calibration Counter		Supported			

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002-22204 *C, 2021-11-15

Revision History

Revision	ECN	Submission Date	Description of Change
**	6157641	04/29/2018	Initial release
*A	6364397	10/25/2018	Added slide 2 and the note descriptions of all pages. Updated slides 3-6, 9, 11, 14, 19. Added Clock Calibration Counter slide Updated the figures
*B	7060645	01/06/2021	Updated slide 2 - 4, 8, 10, 13, 16, 17, 18, 25-28 Deleted slide 4 Added slide 11
*C	7450141	11/16/2021	Updated slide 1, 2, 14