

Watchdog_1

for KIT_AURIX_TC334_LK

Watchdog configuration

AURIX™ TC3xx Microcontroller Training
V1.0.0



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Scope of work

The watchdog is serviced in order to prevent a reset.

This example is showing how to service the WatchDog Timer (WDT) periodically.

Introduction

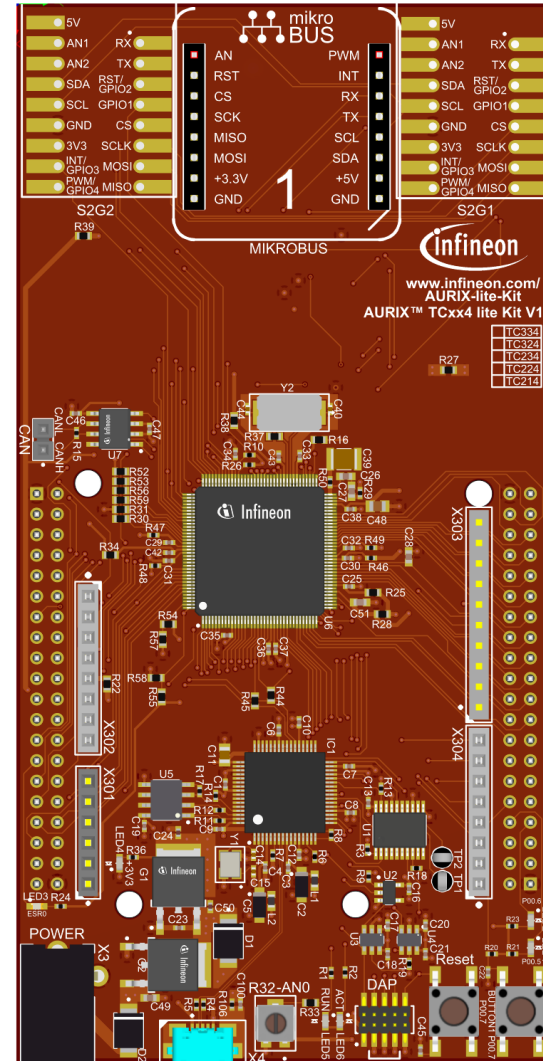
- › The watchdog (WD) provides on the one hand a highly reliable and secure way to detect and recover from software or hardware failure and on the other hand a protection against unintended register write accesses

- › There are two types of Watchdogs:
 - The Safety WD provides protection against unintended writes to critical system registers and memories. It consists of a timer that causes an SMU alarm request if it is not serviced within a certain time interval

 - The individual CPU WDs have similar functionalities as the safety watchdog. They provide protection to CPU registers as well as to particular system registers. The CPU individual timers, if activated, offer the ability to monitor separate CPU execution threads. They have to be serviced similar to the safety watchdog timer within a certain time interval, otherwise a device reset is triggered

Hardware setup

This code example has been developed for the board KIT_A2G_TC334_LITE.



Implementation

Configuring and servicing the CPU 0 watchdog timer

- › Comment out the instruction to disable the CPU watchdog (*IfxScuWdt_disableCpuWatchdog()*). Thus the CPU0 watchdog remains on and needs to be serviced
- › Configure the reload value (REL) that specifies the timeout of the WD timer using the function *IfxScuWdt_changeCpuWatchdogReload()*. The default value is 0xFFFC and the timer counts up. The time window for servicing the WD is very short, therefore it is extended by using 0xE000 as REL
- › The timeout can be calculated using this formula:
$$\text{timeout} \approx (0xFFFF - \text{REL}) / (f_{\text{SPB}} / \text{WDTSCON1.IRx}) = (0xFFFF - 0xE000) / (100 \text{ MHz} / 16384)$$
Note: The value 16384 is a constant, defined by IRx of register WDTSCON1.
- › A time variable is initialized to wait a fixed time inside the infinite loop
- › Call the *IfxScuWdt_serviceCpuWatchdog()* function in order to service the watchdog timer
- › The CPU0 watchdog is serviced periodically every second within the infinite while loop

Note: The above related **ScuWdt** functions need a password in order to write into the CPU0 related watchdog registers. The password is retrieved using the function *IfxScuWdt_getCpuWatchdogPassword()*. The **ScuWdt** functions are part of the library *IfxScuWdt.h*.

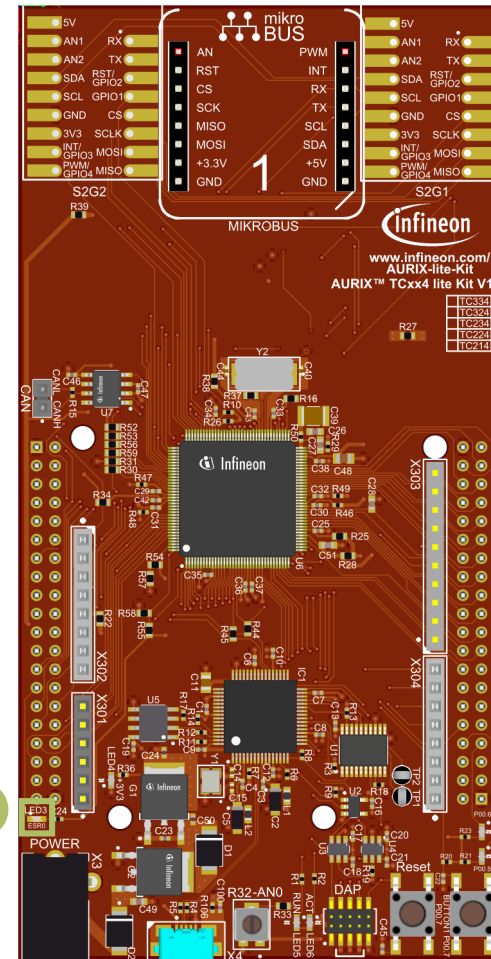
Run and Test

After code compilation and flashing the device, perform the following steps:

- › Terminate the debug session if it is open and restart the device. Check whether LED3 (1) is off - No reset is signaled. Thus the CPU0 watchdog is well serviced periodically
- › Comment out the instruction to service the CPU WD:
lfxScuWdt_serviceCpuWatchdog()
- › Compile, flash and run the code again
- › Terminate the debug session if it is open and restart the device. LED3 (1) turns on after some time signaling a reset. Thus the WDT is not serviced anymore

Note: in order to use the debugger, OCDS is enabled. Whenever the OCDS is enabled, all watchdogs are disabled by default.

Note: by default, if an SMU-induced Application Reset occurs twice (e.g. triggered by a watchdog), a severe system malfunction is assumed and the device is held in permanent Application Reset until a Power-On or System Reset occurs.



References



- › AURIX™ Development Studio is available online:
- › <https://www.infineon.com/aurixdevelopmentstudio>
- › Use the „*Import...*“ function to get access to more code examples.



- › More code examples can be found on the GIT repository:
- › https://github.com/Infineon/AURIX_code_examples



- › For additional trainings, visit our webpage:
- › <https://www.infineon.com/aurix-expert-training>



- › For questions and support, use the AURIX™ Forum:
- › <https://www.infineonforums.com/forums/13-Aurix-Forum>

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