AURIX™ - Autosar MCAL driver

Feature enhancement AURIX TC2xx vs. TC3xx

Device AUTOSAR		AURIX TC2xx	AURIX TC3xx	Safety claim at Production Release
AUTOSAR version		4.0.3	4.2.2	**TC3xx**
MCAL drivers	MC-ISAR Basic package	■ MCU ■ WDG ■ GPT ■ SPI ■ Port ■ DIO ■ ICU ■ PWM ■ ADC ■ CAN ■ CanTrcv ■ LIN ■ Fls ■ FEE ■ BFX ■ CRC	■ MCU ■ WDG ■ GPT ■ SPI ■ Port ■ DIO ■ ICU (supporting GTM, → **new CCU6 and GPT12)** ■ PWM (supporting **GTM → new CCU6)** ■ ADC (feature set 3) ■ CAN ■ CanTrcv ■ LIN ■ FLS ■ FEE (feature set 2) ■ **OCU – new** ■ BFX ■ CRC	■ **ASIL B functionality claim** ■ **Except for CAN, CanTrcv, LIN** ■ **ASIL D process to ensure freedom from interference in memory space**
	MC-ISAR COM Enhanced package	■ FlexRay (not for TC22x, 1x) ■ Ethernet (for ASRv4 only, not for TC23x, 2x, 1x)	■ FlexRay ■ Ethernet	■ **ASIL D process to ensure freedom from interference in memory space**
	MC-ISAR MCD MCAL Complex Drivers	■ UART, MSC (not for TC23x, 2x, 1x), DMA, FLSloader	■ CD: **new production release DS-ADC, SMU** ■ CD: DMA, FLSloader,, UART	■ **ASIL B functionality claim** ■ **Except for FLSloader** ■ **ASIL D process to ensure freedom from interference in memory space**
		■ Demo code only for: HSSL (not for TC23x, 2x, 1x) , SENT, I2C (not for TC23x, 2x, 1x), STM, DS-ADC (not for TC23x, 2x, 1x), SMU, IOM	■ DEMOCD (Demo code / App note – not released for production): HSSL , SENT, I2C, IOM, STM, IRQ	■ No safety claim
Configuration tool		Tresos	Tresos	
Compiler		- Tasking 4.2r2 - Windriver Diab 5.9.2.0+p - HighTec GNU 4.6.3.0	- migrate to TASKING 6.2r2 - HighTec GNU 4.9.2.0 - Wind River v5.9.6.4 or v5.9.6.6 (still tbd) - Greenhills (version to be defined) for TC38x, TC35x, TC36x; availability to be discussed on request	
Delivery package		Source code, Documentation	Source code, Documentation	

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New - AURIX2G ISAR MCAL Safety claim (TC3xx)

- The Productive MCAL drivers have an **ASIL B functionality claim** or QM functionality claim (module dependent, see below)
  - The modules CAN, LIN, FlexRay, Ethernet, CAN transceiver do **not** have an ASIL B claim, because it is assumed that End-to-End protection is used for a safe communication
  - The module FLSloader does **not** have an ASIL B claim

- Each Productive MCAL driver is developed according to **ASIL D process** ensuring Freedom from Interference in memory space, making it easier for the integrator to ensure coexistence with other SW outside MCAL SEooC, as required by ISO 26262 Part 9 Clause 6

- Additionally, the MCAL software development process is assessed at **ASPICE level 2** for the Productive drivers

- The DEMOCD modules HSSL, SENT, I2C, IOM, STM, IRQ will have **NO** safety claim and NO ASPICE level 2 process

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NEW SMU Driver: Additional Information

- To support customers to realise ASIL D, IFX:
  - Provides Smu_Init to initialize the SMU peripheral including its configuration ➔ ASIL B(D)
  - Provides Smu_InitCheck: safety mechanism to verify initialization is correct and complete ➔ ASIL B(D)
  - Performs DFA to confirm that Init and InitCheck are independent ➔ ensure no common cause failures between Init and InitCheck
  - Provides Smu_Lock service in SMU driver to prevent corruption by locking configuration data in SMU registers

- Customers should use ASIL decomposition at System level for satisfying SMU ASIL D configuration requirement

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Infineon Microcontroller: Software Quality

TC2xx (no ASPICE) → NEW: TC3xx (ASPICE L2)

- Standard and tailored development **process SDHB** established
- SDHB, as Infineon Development Standard, has been extended to support Safety **ISO26262**
- **NEW in TC3xxx:**
  - **ASPICE L2** aligned process for AURIX TC3x MCAL
    - 6 processes at L3
    - 4 processes at L2

KUGLER MAAG CIE

This is to demonstrate
that the project:

AURIX2G - TC39A_SW_MCAL

at Infineon Technologies India Pvt. Ltd, Bangalore, India and Munich, Germany

has provided evidences for the Capability Levels 2 and 3
in a project assessment performed on 22.-26. May 2017
and 19th October 2017
based on Automotive SPICE® V. 2.5

The Assessment conducted is a **Class 3, Type A** assessment according to ISO/IEC 33002.

Assessed Processes:	
Capability Level 3:	MAN.3, SUP.8, 9, 10, ENG.5 and ENG.6
Capability Level 2:	ENG.4*, ENG.7, ENG.8 and SUP.1
	*Scope: new project TC-3XX
Lead Assessor:	Markus Müller, ID: 4961-0600-11507-05
Co Assessor:	Bhaskar Vanamali, ID: 4961-0500-11625-05
Assessment Sponsor:	Narasimha Murthy

20. October 2017

Markus Müller
Lead Assessor

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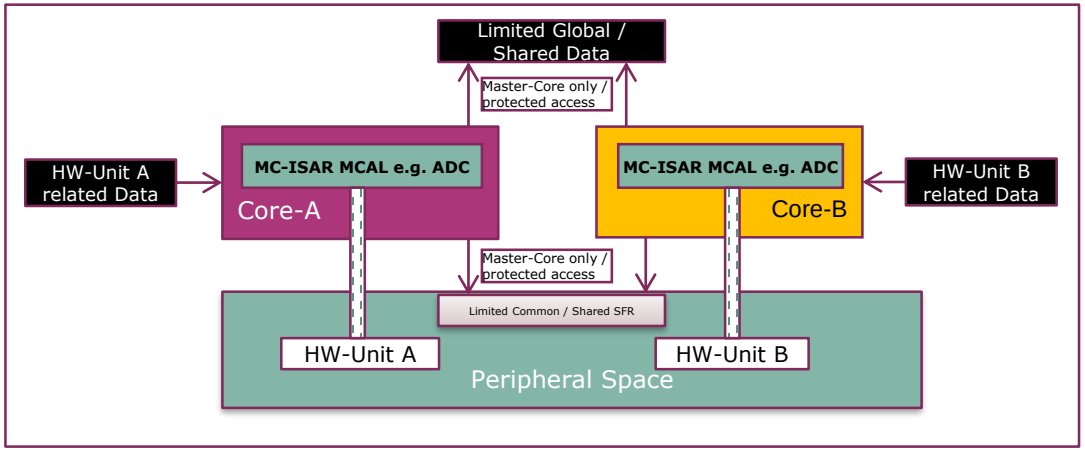
NEW - AURIX TC3xx New Multi Core Concept

MC-ISAR/MCAL with multicore support for TC3xx

- With TC3xx the number of cores are rising up to 6 cores (4 lockstep and 2 non lockstep cores)
- Assign MCAL instances to cores based on peripheral specific resource granularity (e.g. ADC HW kernel, SPI HW kernel, PWM channels, etc.)
  - Multi core partitioning supported for ADC, CAN, GPT, ICU, PWM, SPI, OCU, WDG drivers
- Multi core access without HW resource allocation for CRC, DIO, MCU and PORT



Main benefits with AURIX MCAL Multicore support:

- Possibility of seperation of multiple applications in one AURIX
- OEM, Tier1 applications can run isolated on separate core in one AURIX
- Simplify safety system partitioning. Enabling handling of peripherals for
  - Safety critical domain from lockstep core
  - Non safety critical tasks from non lockstep core
- Increased overal performace with limited power consumption increase

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