

24V Automotive Gateway-V1.0

For AURIX™ family

About this document

Scope and purpose

This document describes the features and hardware details of the 24V Automotive Gateway-V1.0 equipped with an TriCore AURIX™ Microcontroller from Infineon Technologies AG.

Intended audience

This document is intended for anyone who wants to develop software on the 24V Automotive Gateway-V1.0 or wants to use this kit for evaluating and demonstrating the capabilities of the AURIX microcontroller in combination with other Infineon Technologies products.

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1 Introduction of the 24V Automotive Gateway V1.0

The 24V Automotive Gateway-V1.0 offers a huge range of Application use cases. With the AURIX™ TC397XE B Step in combination with Realtek's RTL9047AA Switch future In Vehicle Networks can be addressed and evaluated. The TC397XE B Step is connected with a 1Gbps RGMII port to the Ethernet Switch for data transfer and a SPI channel for managing the Switch. The RTL9047AA provide five 100Base-T1 Ports together with the Rosenberger H-MTD® connector set provide the right feature set to connect the Automotive Gateway Board to an In Vehicle Network. 16 CAN-FD connections, 4 LIN and 4 FlexRay channels in total, half on each CPU allow bridging of different network topologies. CPU A offers in addition a PSI5-S connection with 4 channels. CPU B provides a raspberry pi like extension header to add extension Boards like pHAT. Both CPUs are connected with two high speed HSSL channels and one SPI channel.

AURIX™ TC3xx does not compromise on security. The second generation of the programmable Hardware Security Module (HSM) is available across the family for secure on-board communications and to prevent hardware manipulation such as tuning. Infineon's Trusted Platform Module (TPM) SLB9670 is the latest product featuring a fully TCG TPM 2.0 standard compliant module connected via SPI to the AURIX™.

1.1 Key features

- Dual AURIX™ 2 generation TC39 BA step device
- SBC TLE9278
- TLF30682
- CAN-FD
- FlexRay™
- LIN
- TPM
- Solenoid Relay
- Realtek automotive switch with 5 x 100 Base-T1 RTL4047AA VC
- Realtek Gb PHY RTL8211
- PSI5-S
- eMMC

24V Automotive Gateway-V1.0

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Introduction of the 24V Automotive Gateway V1.0

1.2 Block diagram

The block diagram in Figure 1 shows the main components of the 24V Automotive Gateway-V1.0 and interconnects between the used devices.

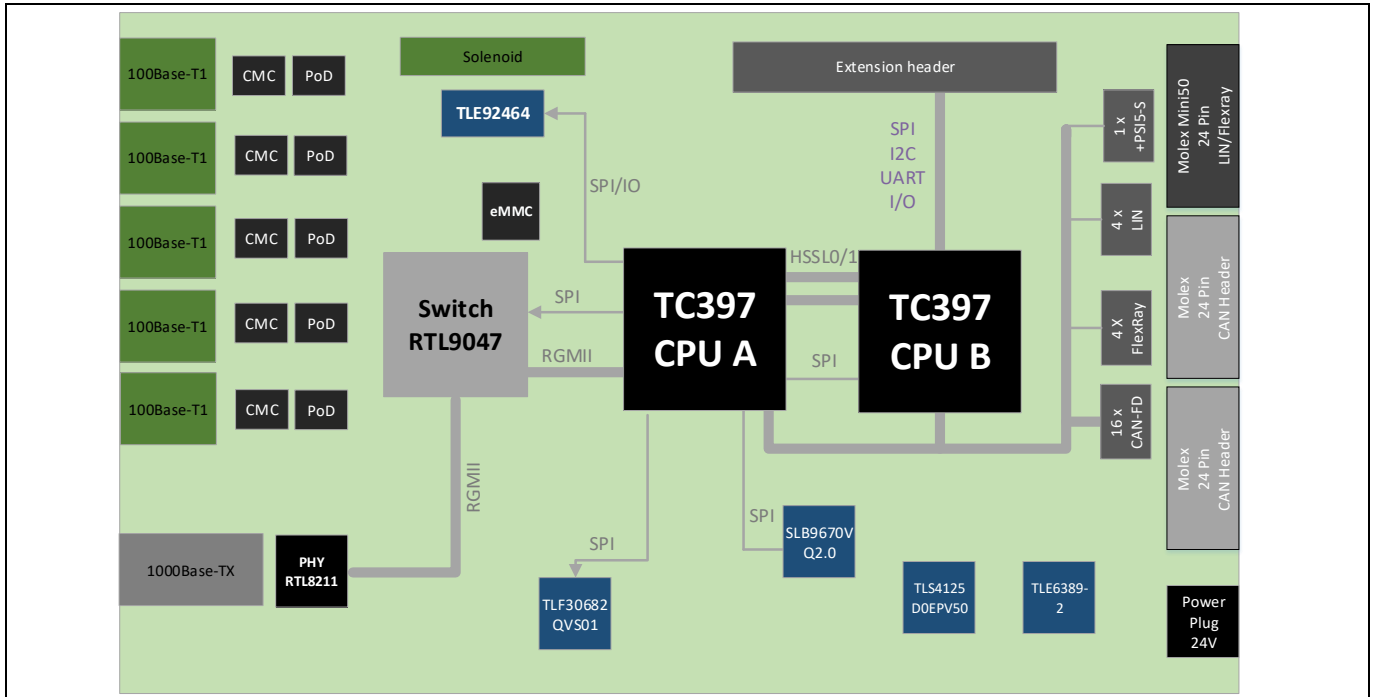


Figure 1 Block diagram of the Gateway Board

2 Hardware description

The following chapters provide a detailed description of the hardware and how it can be used.

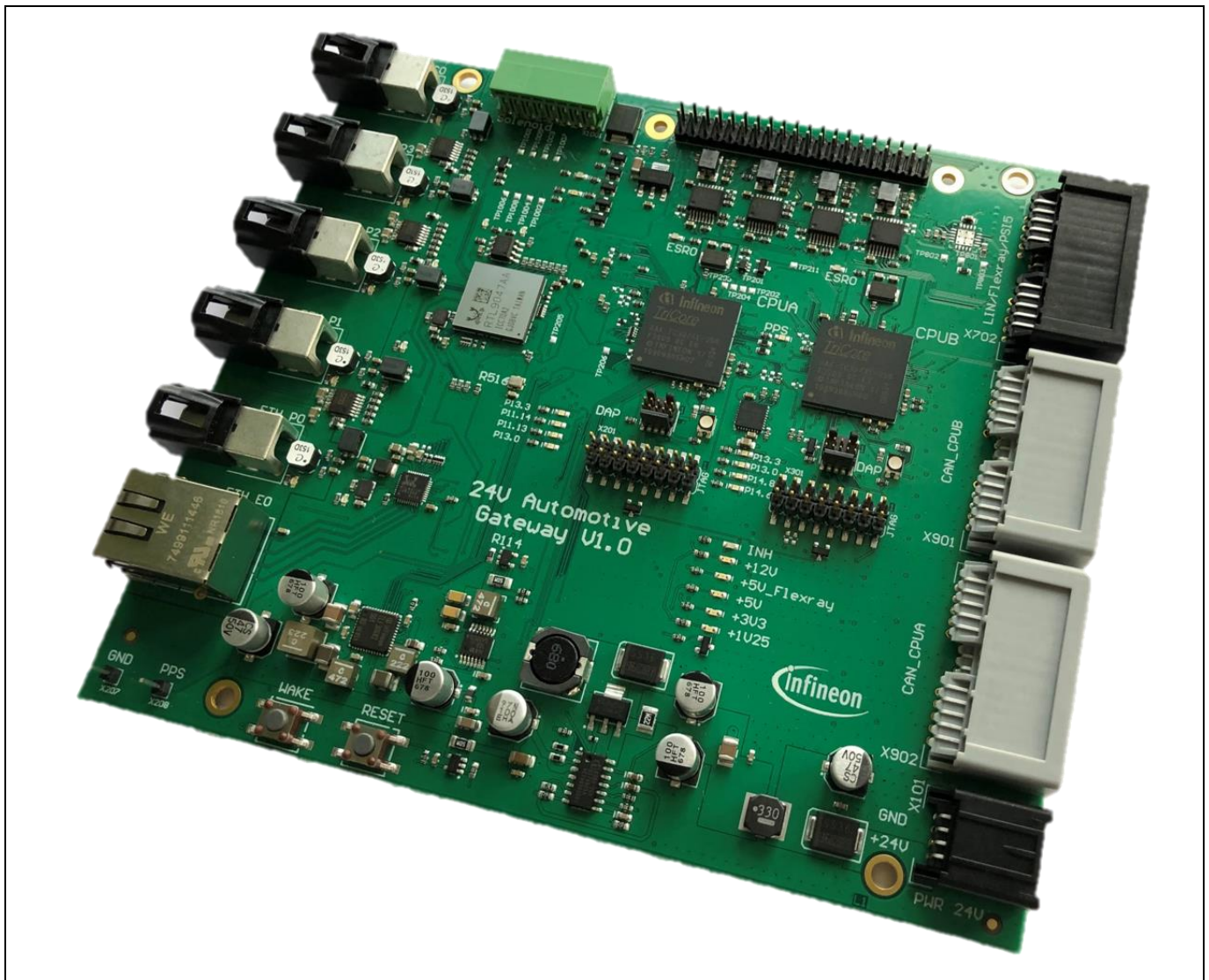


Figure 2 PCB of the 24V Automotive Gateway

24V Automotive Gateway-V1.0

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Hardware description

2.2 Power supply

The Power Supply concept must guarantee a stable supply of the Board. The standard Input voltage is 24V. Out of this the TLE6389 will generate 12V. Out of this 12V 3,3V and 5V will be generated. Figure 3 and Figure 4 visualize the power domains and used structure of Infineon's supply IC behind.

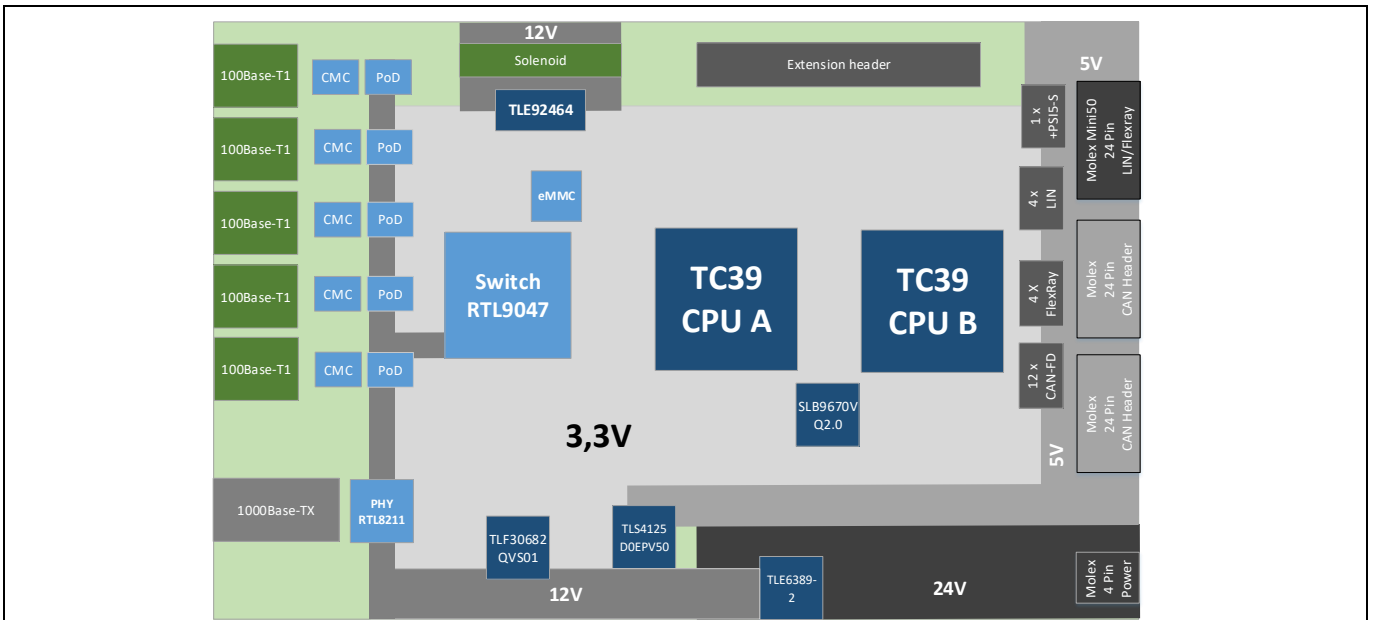


Figure 3 Power domains 24V Automotive Gateway Board

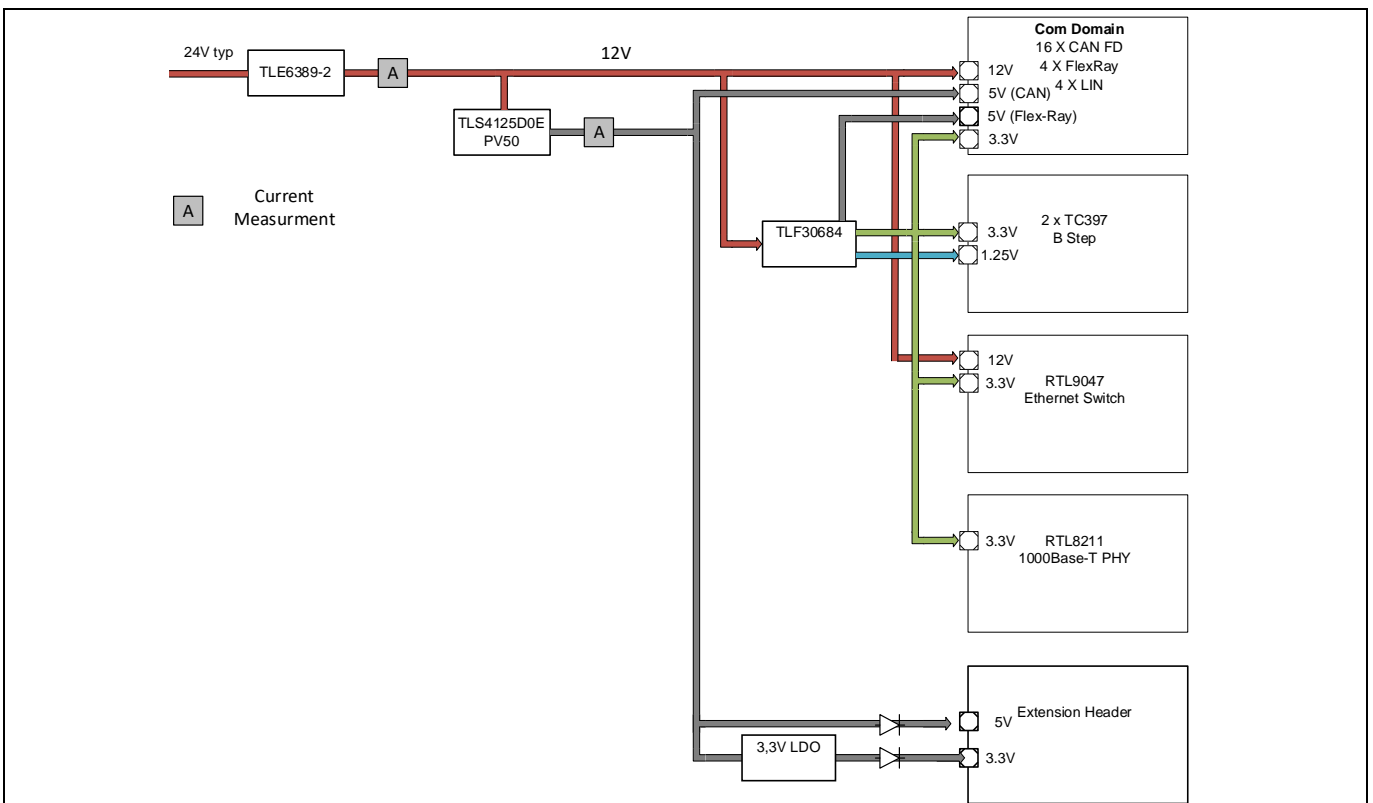


Figure 4 Supply structure

24V Automotive Gateway-V1.0

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Hardware description

2.2.1 TLF30682QVS01

The TLF30682QVS01, member of the OPTIREG™ PMIC-family, is a multi-rail supply for ADAS-applications like 76-79 GHz-Radar, multi-purpose Camera, or Display, Cluster, or Center Stack applications.

It's using an efficient and flexible pre-/post-regulator concept over a wide input voltage range. The high switching frequency range of the battery connected, synchronous buck (3V3/3.5A) with integrated switches allows optimization in usage of small filter components. An integrated synchronous SMPR-buck (Switch-Mode Post-Regulator) with high switching frequency enables supply for core or for memory (0V9-1V3/2.0A). Additionally, an asynchronous SMPR-boost (5V0/0.25A), running as well with high switching frequency, provides the 5V-domain for transceiver. Integrated switches, compensation and the high switching frequency is both minimizing the number and the value of external components required.

Additional features are under-/over-voltage monitoring (via independent reference) of all integrated and up to two external rails as well as a flexible watchdog concept to supervise the µC offers high flexibility for multiple applications.

The automotive qualified TLF30682QVS01 is coming in small, thermally enhanced VQFN-48 capable for automated optical inspection.

The TLF30682QVS01 is PRO-SIL™ ISO26262-Ready, functional safety documents are available on request (for more info visit www.infineon.com/PRO-SIL).

The device provides the following features:

- Step-down pre-regulator for wide input voltage range from 3.7 to 35 V (40 V limited time) with low overall power loss and fast transient performance. Suitable for operation with ceramic capacitors
- High-efficiency step-down post regulator for second output voltage generation
- Step-up post regulator with 5 V output voltage
- Voltage monitoring for two external voltage rails including enable signals
- 16-bit SPI interface to host CPU
- Configurable window watchdog

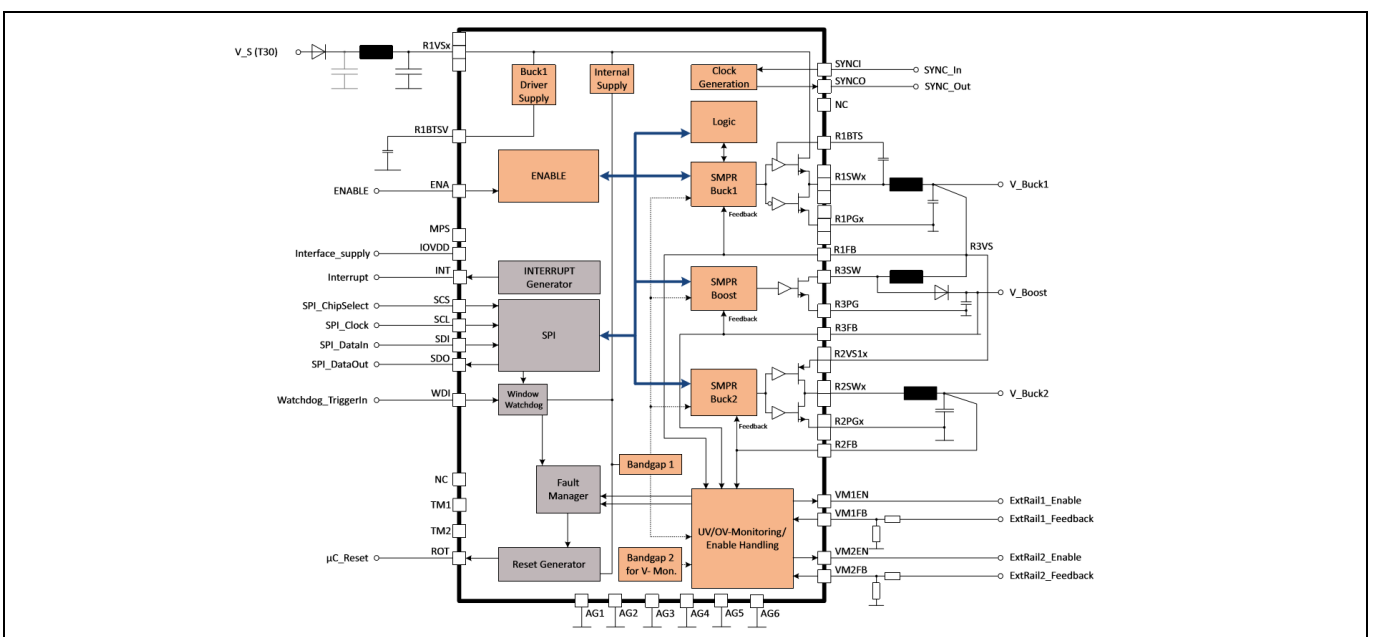


Figure 5 TLF30682QVS01 Block Diagram

Table 1 shows the signal connection list for the connection between CPU A and the TLF30682QV01.

Table 1 Connection between CPU A and TLF30682QVS01

CPU	Module	Signal	Pin	Comment
CPU A	QSPI2	CSN	P14.6	SLSO2
CPU A	QSPI2	SCK	P15.8	
CPU A	QSPI2	SI	P15.7	
CPU A	QSPI2	SO	P15.6	
CPU A	ESR	INT	/ESR1	
CPU A	Reset	/PORST	/PORST	
CPU A	I/O	WDI	P14.8	

2.2.2 Power supply sequencing and power down

The 24V Automotive Gateway-V1.0 input voltage is converted into several different voltage domains. Powering up the board will switch on the cascaded voltage ICs.

There is a global 12V INH signal which can switch off the +5V regulator and the TLF30682QVS01 for the main +3,3V. This signal is generated out of a logic AND from the INH signals coming from the Realtek Switch, the Flexray and LIN transceivers of CPU A.

The Automotive Ethernet network sleep and wake-up concept is designed to save maximum power of car ECUs. Open Alliance working group TC10 describes the concept used in 100/1000Base-T1.

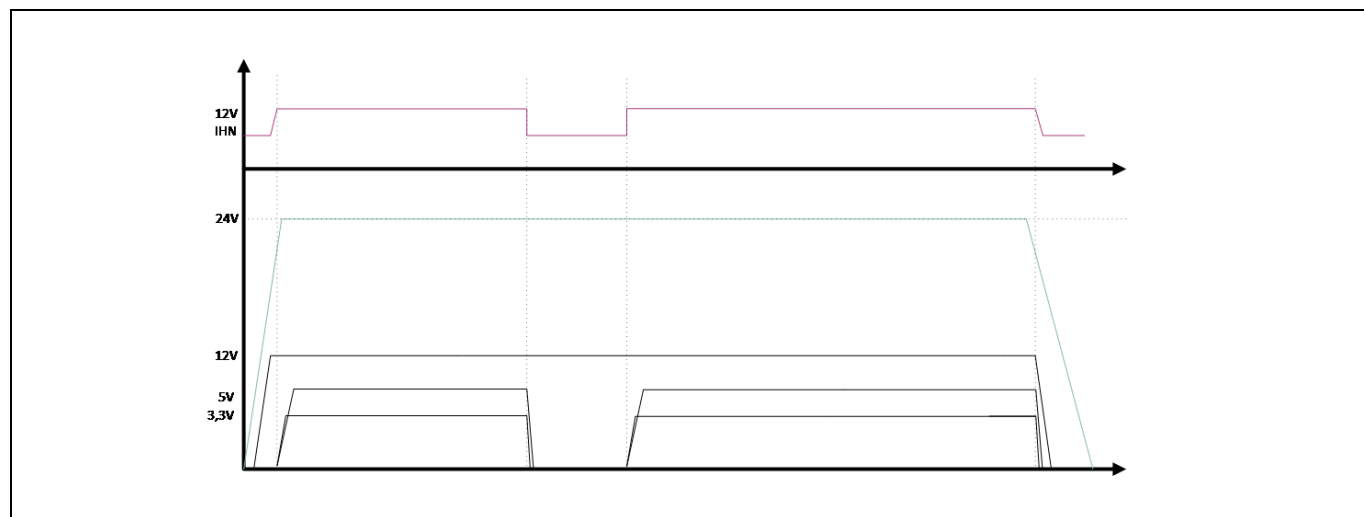


Figure 6 Board Power Sequence

2.2.3 Supply Monitoring functions

The 24V Automotive Gateway-V1.0 provide several monitoring functions to determine the correct voltage levels, acting according violations and provide these as meta data to higher management functions.

Figure 7 The following two tables list the signals connected to the VADC of CPU A and CPU B.

Table 2 Analog Signals to CPU A

CPU	Module	Signal	Pin	Comment
CPU A	VADC	AN2_A	P40.0	PoDL sense signal U601
CPU A	VADC	AN13_A	P40.5	+3,3V analog signal
CPU A	VADC	AN16_A	P40.6	+3,3V analog signal extension Header
CPU A	VADC	AN19_A	P40.8	+12V current feedback
CPU A	VADC	AN20_A	P40.9	+5V current feedback
CPU A	VADC	AN29_A	P41.3	+5V analog signal
CPU A	VADC	AN39_A	P41.7	+12/24V analog signal supply Solenoid
CPU A	VADC	AN40_A		+12V analog signal
CPU A	VADC	AN44_A	P41.8	PoDL sense signal U603
CPU A	VADC	AN46_A	P41.10	PoDL sense signal U602

Table 3 Analog Signals to CPU A

CPU	Module	Signal	Pin	Comment
CPU B	VADC	AN2_B	P40.0	CAN transceiver standby signal
CPU B	VADC	AN13_B	P40.5	+3,3V analog signal
CPU B	VADC	AN29_B	P41.3	+5V analog signal
CPU B	VADC	AN40_B		+12V analog signal

2.3 Board Resets

The 24V Automotive Gateway-V1.0 features several reset sources and groups depending on connected devices. The main reset source is the /PORST signal driven by the TLF30682QV01. This signal is connected to the CPU A, CPU B. CPU A as the system master can optionally issue a /PORST reset to CPU B via the signal P11.15_A.

The SLB9670VQ2.0 per default can be reset by P33.15 from CPU A. Optionally he can be reset by CPU A /ESR0 signal upon a software reset or PORST/ adapting the zero ohm bridges.

The eMMC per default gets reset by P15.2 of CPU A. Optionally he can be reset by CPU A /ESR0 signal upon a software reset adapting the zero ohm bridges.

The Solenoid Relay, TLE92464ED can be reset by P10.2 of CPU A.

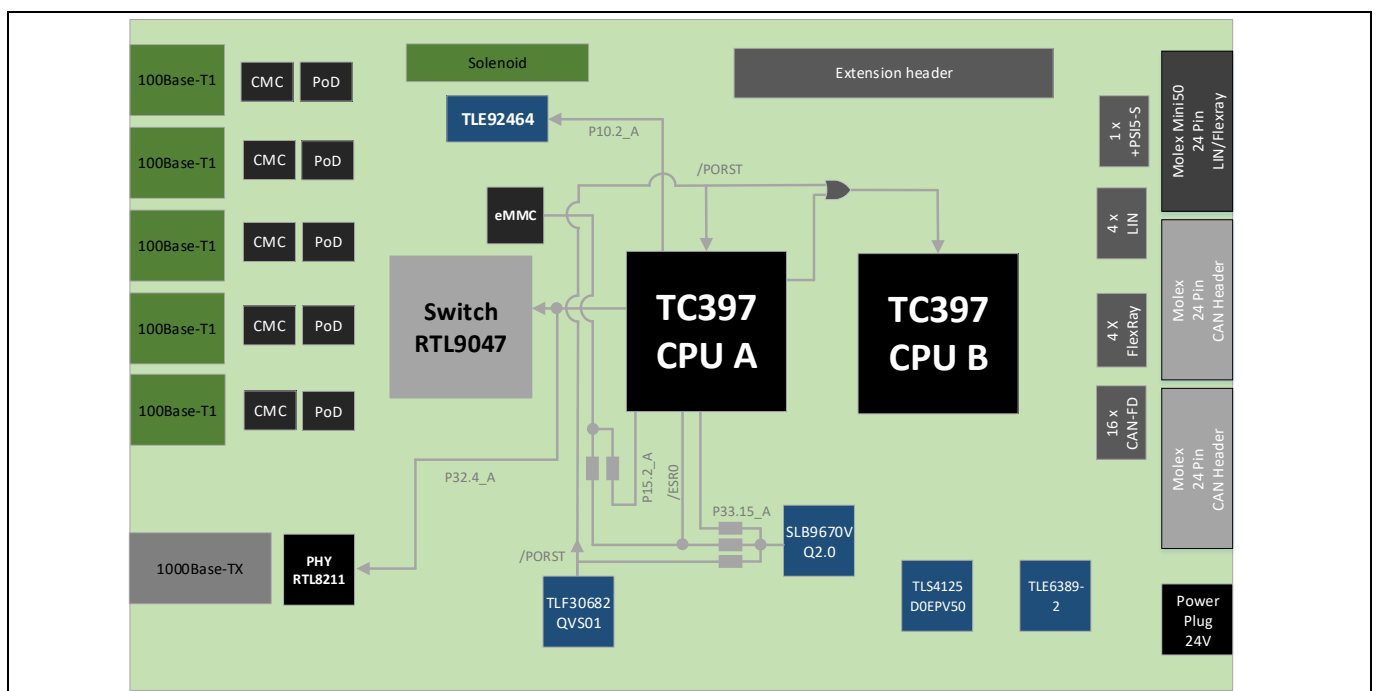


Figure 8 Reset connections

2.4 AURIX™ 2G CPU A to Switch connections

The AURIX™ 2G B Step provides a 1Gbit Ethernet MAC using RGMII to connect a Switch or PHY. On the 24V Automotive Gateway-V1.0 the AURIX™ device is connected via RGMII interface to Realtek's RTL9047AA switch on Port E1. As Switch Management interface a SPI channel is connected.

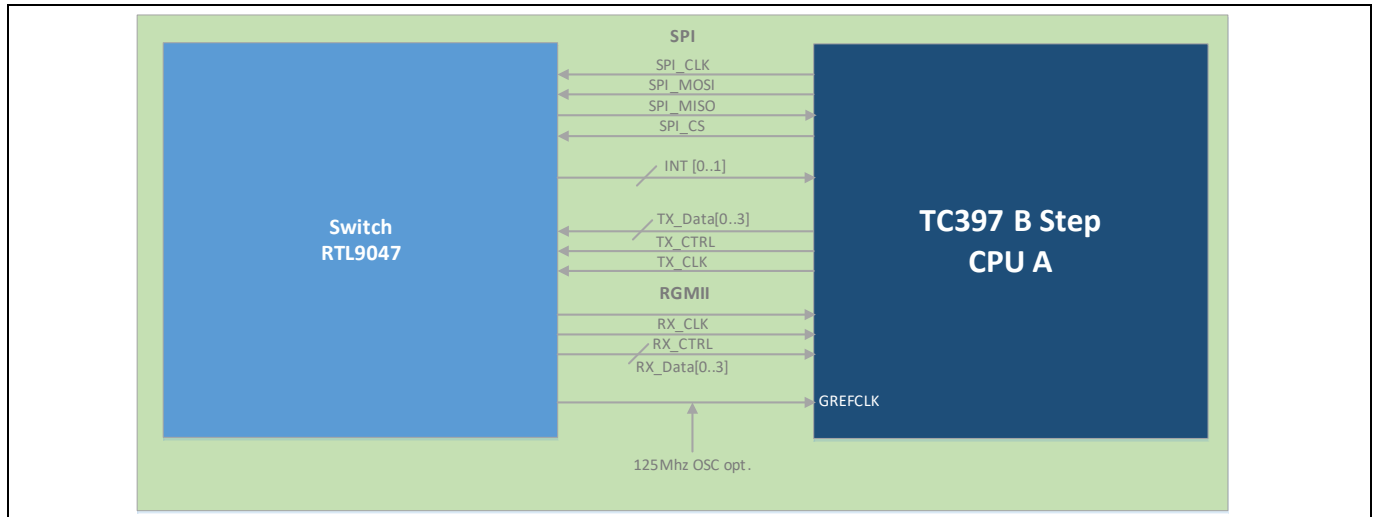


Figure 9 AURIX™ 2G CPU A to Switch connections

The AURIX™ marked as CPU A is connected via RGMII interface to the RTL9047 Ethernet Switch. Besides the standard RGMII signals the AURIX™ needs a 125MHz reference clock called GREFCLK for the Gb Ethernet Interface. By default this clock will be generated by the Ethernet Switch. Since not all Switches and PHYs provide such a clock, a crystal oscillator can be used. The 24V Automotive Gateway-V1.0 is prepared to use for example a NDK NZ2016SHA selectable by R512 and R538.

Attention: If the 125MHz GREFCLK is not present, the GMAC will not execute the DMA_MODE.SWR software reset.

In addition to the Gbit Ethernet Interface, a 25MHz SPI channel is used to manage the RTL9047 Ethernet Switch. The Ethernet Switch pins GPIOB_0 and GPIOB_1 are connected to the AURIX™ as well. GPIOB_0 is configurable as Interrupt Pin from Switch to AURIX™. GPIOB_1 can be configured for PTP TAI functionality.

Table 9 shows the signal connection list for the connection between CPU A and the Ethernet Switch.

Table 4 Connection between CPU A and the Ethernet Switch

CPU	Module	Signal	Pin	Comment
CPU A	GMAC	E1_RXD0	P11.3	GETH_TXD0
CPU A	GMAC	E1_RXD1	P11.2	GETH_TXD1
CPU A	GMAC	E1_RXD2	P11.1	GETH_TXD2
CPU A	GMAC	E1_RXD3	P11.0	GETH_TXD3
CPU A	GMAC	E1_RXDV	P11.6	GETH_TCTL
CPU A	GMAC	E1_RXC/E1_RXER	P11.4	GETH_TXCLK
CPU A	GMAC	E1_TXD0	P11.10	GETH_RXD0
CPU A	GMAC	E1_TXD1	P11.9	GETH_RXD1

CPU A	GMAC	E1_TXD2	P11.8	GETH_RXD2
CPU A	GMAC	E1_TXD3	P11.7	GETH_RXD3
CPU A	GMAC	E1_TXEN	P11.11	GETH_RXCTLA
CPU A	GMAC	E1_GTXC/E1_MTXC	P11.12	GETH_RXCLKA
CPU A	GMAC	CKDIG	P11.5	GETH_GREFCLK
CPU A	QSPI	GPIOA_0	P23.4	QSPI4_SLSO5
CPU A	QSPI	GPIOA_1	P33.11	QSPI4_SCLK
CPU A	QSPI	GPIOA_2	P22.0	QSPI4_MTSR
CPU A	QSPI	GPIOA_3	P22.1	QSPI4_MRSTB
CPU A	I/O - GTM	GPIOB_0	P10.4	Used for Interrupt generation
CPU A	I/O - GTM	GPIOB_1	P10.8	Used for Interrupt generation
CPU A	I/O	RESETB	P32.4	Reset

2.5 AURIX™ Ethernet MAC Address EEPROM

The 24V Automotive Gateway-V1.0 supports an EEPROM with a unique MAC address. Software can load these and use it to configure the Ethernet GMAC. Table 9

Table 5 Ethernet MAC Address EEPROM

CPU	Module	Signal	Pin	Comment
CPU A	I2C	SCL	P13.1	
CPU A	I2C	SDA	P13.2	

2.6 CPU A Ethernet PPS signal

Modern Ethernet systems provide a pulse per second (PPS or 1PPS) signal which is an electrical signal that has a width of less than one second and a sharply rising or abruptly falling edge that accurately repeats once per second. PPS signals are used for precise timekeeping and time measurement.

CPU A is providing the PPS signal via port pin P14.4_A. The signal itself can be measure by the signal header X208 and is connected to a logic buffer. CPU B can enable the output with port pin P23.0_B and gets forwarded to pin P15.0_B which provides timer inputs to the GTM core. P15.0_B is driving a blue LED.

2.7 Ethernet Switch RTL9047AA and RTL8211 PHY

To be able to connect the Board to a standard IT infrastructure, a Gbit Ethernet Interface is realized using RTL9047AA Port E0 via RGMII and Realtek Gbit PHY RTL8211 with an RJ45 connector. The PHY management interface MDIO will be connected to the AURIX™ MDIO interface.

To find out more about Realtek’s Switch and PHY please contact the listed contact partner in Appendix .

2.7.1 100Base-T1 CMC and PoDL

The 24V Automotive Gateway-V1.0 supports on all 5 100Base-T1 ports power over data line. The AURIX™ CPU A can select for each port switch 12 V to the port. It is recommended to not draw more than 0,22A out of one PoDL Link. This matches to a PoDL class 1 definition.

With the BTS7008 diagnostic features it is possible to do proportional load current sense, open Load in ON and OFF state or short circuit to ground and battery detection.

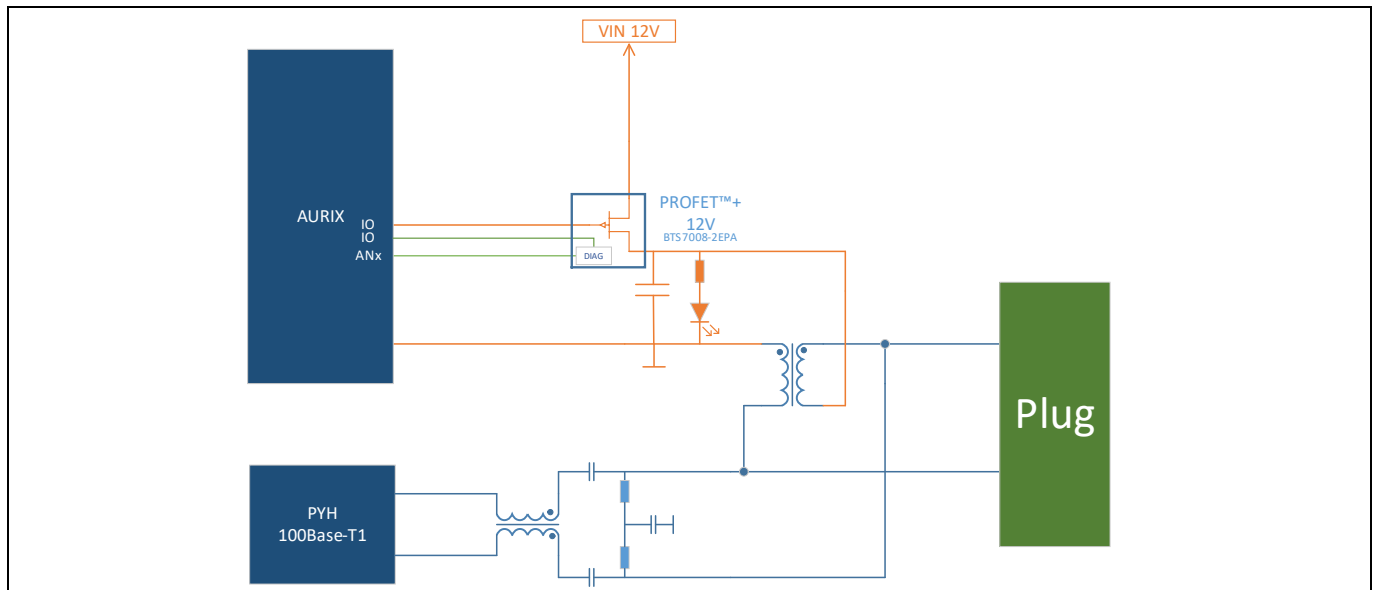


Figure 10 CMC and PoDL schematic

Table 6 shows the PoDL signal connection list.

Table 6 PoDL Signal List

CPU	Module	Signal	Pin	Comment
CPU A	I/O	IN0	P33.0	Port ETH_C0 power enable
CPU A	I/O	DEN	P33.1	Port ETH_C0 diagnose enable
CPU A	I/O	DSEL	P33.2	Port ETH_C0 diagnose channel select
CPU A	AN	IS	AN2	Diagnose feedback ETH_C0
CPU A	I/O	IN0	P01.3	Port ETH_P0 power enable
CPU A	I/O	IN1	P01.4	Port ETH_P1 power enable
CPU A	I/O	DEN	P01.5	Port ETH_P0 and ETH_P1 diagnose enable
CPU A	I/O	DSEL	P01.6	Port ETH_P0 and ETH_P1 channel select
CPU A	AN	IS	AN46	Diagnose feedback ETH_P0 and ETH_P1
CPU A	I/O	IN0	P00.10	Port ETH_P2 power enable
CPU A	I/O	IN1	P00.11	Port ETH_P3 power enable
CPU A	I/O	DEN	P01.7	Port ETH_P2 and ETH_P3 diagnose enable
CPU A	I/O	DSEL	P02.10	Port ETH_P2 and ETH_P3 channel select
CPU A	AN	IS	AN44	Diagnose feedback ETH_P2 and ETH_P3

24V Automotive Gateway-V1.0

For AURIX™ family

Hardware description

2.7.2 Standard 1000Base-T1 / 100Base-T1 connector

Rosenberger H-MTD® is a 360° fully shielded differential connector system. The new developed system combines high-performance data transmission up to 15 GHz or 20 Gbps and a small package size in a robust automotive grade housing. H-MTD® Cable and PCB connectors are available as single, double, quad for STP, UTP and SPP cables.

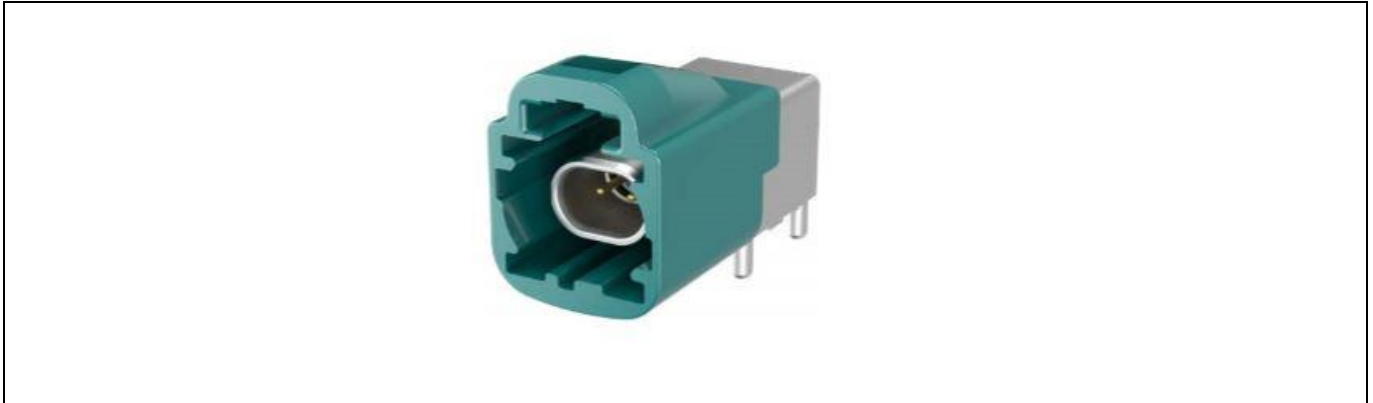


Figure 11 Rosenberger H-MTD

To find out more about Rosenberger H-MTD® please contact the listed contact partner in Appendix .

2.7.3 1000Base-TX Magnetics and RJ45 Jack

To connect the 24V Automotive Gateway-V1.0 to a standard IT infrastructure a RJ45 jack for CAT6/CAT7 cables is provided. This Gbit Ethernet port is connected as port E0 to the RTL9047 Switch



Figure 12 Magnetics and RJ45 Jack

2.8 Molex Mini50 CAN-FD

There are two Molex Mini50 connectors for CAN-FD connections on the 24V Automotive Gateway V1.0. In sum 16 Nodes capable for classic CAN and CAN-FD are available through these headers. Each of the CPU A and CPU B provide 8 CAN channel on a Molex connector. The Coding of CPU is explained in chapter CAN-FD Signals from CPU A, for CPU B in CAN-FD Signals from CPU B.

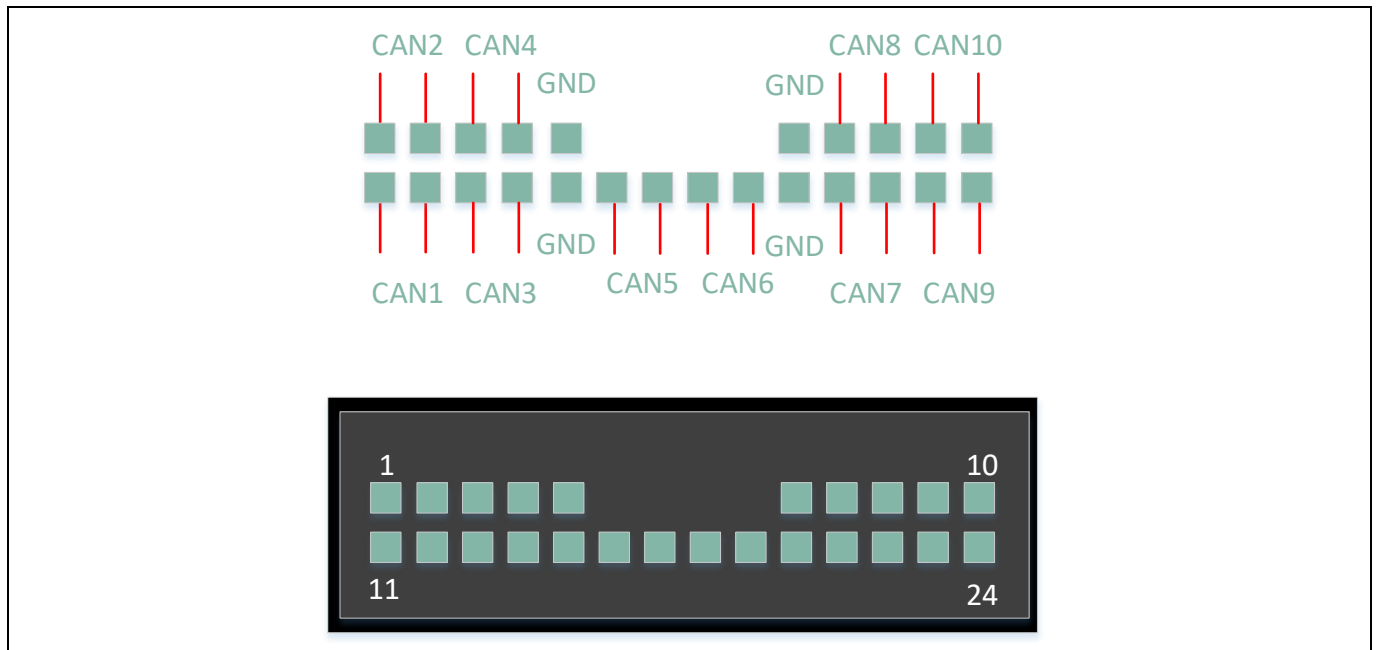


Figure 13 Molex Mini50 CAN-FD signal coding

2.8.1 CAN-FD Signals from CPU A

Table 9 shows the CAN-FD signal connection list.

Table 7 CAN-FD Signal List CPU A

CPU	Module	Signal	Pin	Header	Comment
CPU A	CAN1	CAN10_RXDA	P00.1		CAN 1 Node 0
CPU A	CAN1	CAN10_TXD	P00.0		CAN 1 Node 0
CPU A	CAN0/CAN2	CAN03_RXDA/CAN21_RXDA	P00.3		CAN 0 Node 3/ CAN 2 Node 1
CPU A	CAN0/CAN2	CAN03_TXD/CAN21_TXD	P00.2		CAN 0 Node 3/ CAN 2 Node 1
CPU A	CAN1	CAN11_RXDB	P00.5		CAN 1 Node 1
CPU A	CAN1	CAN11_TXD	P00.4		CAN 1 Node 1
CPU A	CAN0	CAN01_RXDB	P14.1		CAN 0 Node 1
CPU A	CAN0	CAN01_TXD	P14.0		CAN 0 Node 0
CPU A	CAN1/CAN2	CAN12_RXDC/CAN23_RXDB	P23.3		CAN 1 Node 2/ CAN 2 Node 3

CPU A	CAN1/CAN2	CAN12_TXD/CAN23_TXD	P23.2		CAN 1 Node 2/ CAN 2 Node 3
CPU A	CAN2	CAN22_RXDC	P23.6		CAN 2 Node 2
CPU A	CAN2	CAN22_TXD	P23.5		CAN 2 Node 2
CPU A	CAN1	CAN13_RXDC	P22.5		CAN 1 Node 3
CPU A	CAN1	CAN13_TXD	P22.4		CAN 1 Node 3
CPU A	CAN0/CAN2	CAN03_RXDB/CAN21_RXDD	P32.2		CAN 0 Node 3/ CAN 2 Node 1
CPU A	CAN0/CAN2	CAN03_TXD/CAN21_TXD	P32.3		CAN 0 Node 3/ CAN 2 Node 1

2.8.2 CAN-FD Signals from CPU B

All CAN transceivers are in standby per default. To be able to send CAN messages please use the P33.0 of CPU B to enable them. With the analog input AN2 of CPU B the current value of the CAN transceiver STB signal can be measured.

Table 8 CAN-FD Signal List CPU B

CPU	Module	Signal	Pin	Header	Comment
CPU B	CAN0	CAN01_RXDB	P14.1		CAN 0 Node 1
CPU B	CAN0	CAN01_TXD	P14.0		CAN 0 Node 1
CPU B	CAN0/CAN2	CAN03_RXDA/CAN21_RXDA	P00.3		CAN 0 Node 3/ CAN 2 Node 1
CPU B	CAN0/CAN2	CAN003_TXD/CAN21_TXD	P00.2		CAN 0 Node 3/ CAN 2 Node 1
CPU B	CAN1	CAN10_RXDA	P00.1		CAN 1 Node 0
CPU B	CAN1	CAN10_TXD	P00.0		CAN 1 Node 0
CPU B	CAN2	CAN23_RXDA	P14.10		CAN 2 Node 3
CPU B	CAN2	CAN23_TXD	P14.9		CAN 2 Node 3
CPU B	CAN1	CAN11_RXDB	P00.5		CAN 1 Node 1
CPU B	CAN1	CAN11_TXD	P00.4		CAN 1 Node 1
CPU B	CAN1	CAN13_RXDC	P22.5		CAN 1 Node 3
CPU B	CAN1	CAN 13_TXD	P22.4		CAN 1 Node 3
CPU B	CAN1/CAN2	CAN12_RXDC/CAN23_RXDB	P23.3		CAN 1 Node 2/ CAN 2 Node 3
CPU B	CAN1/CAN2	CAN12_TXD/CAN23_TXD	P23.2		CAN 1 Node 2/ CAN 2 Node 3
CPU B	CAN2	CAN22_RXDC	P23.6		CAN 2 Node 2
CPU B	CAN2	CAN22_TXD	P23.5		CAN 2 Node 2

2.9 Molex Mini50 FlexRay™ LIN PSI5S

The Molex Mini 50 connector X702 combines Flexray, LIN and PSI5S signal connections. Figure 14 show the connection scheme of that connector.

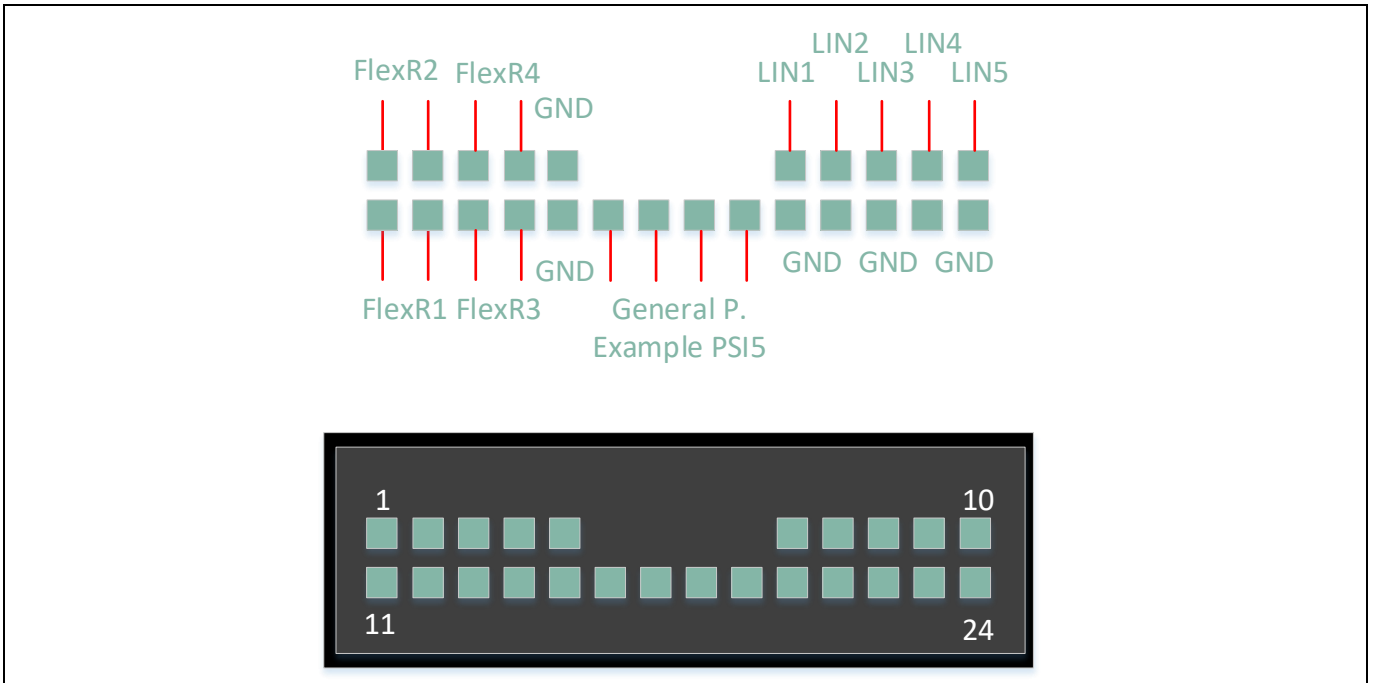


Figure 14 Molex Mini50 FlexRay™ LIN PSI5S signal coding

2.9.1 FlexRay™

There are 4 FlexRay™ connectors available on the 24V Automotive Gateway-V1.0. Two of them connected on each CPU. In addition to the standard FlexRay™ signals, several control signals are added.

Table 9 shows the FlexRay™ signal connection list.

Table 9 FlexRay™ Signal List

CPU	Module	Signal	Pin	Header	Comment
CPU A	ERAY0	RXD	P02.1	ERAY-A_A	ERAY0_RXDA2
CPU A	ERAY0	TXD	P02.0	ERAY-A_A	ERAY0_TXDA
CPU A	ERAY0	TXDEN	P14.9	N.C	ERAY0_TXENA
CPU A	I/O	STBN	P02.8	N.C	Zero Ohm R262 resistor (assembled)
CPU A	I/O	ERRN	P00.6	N.C	
CPU A	I/O	EN	P02.6	N.C	
CPU A	ERAY0	RXD	P02.3	ERAY-B_A	ERAY0_RXDB2
CPU A	ERAY0	TXD	P02.2	ERAY-B_A	ERAY0_TXDB
CPU A	ERAY0	TXDEN	P02.5	N.C	ERAY0_TXENB
CPU A	I/O	STBN	P02.9	N.C	Zero Ohm R263 resistor (assembled)

CPU A	I/O	ERRN	P00.7	N.C	
CPU A	I/O	EN	P02.7	N.C	
CPU B	ERAY0	RXD	P02.1	ERAY-A_B	ERAY0_RXDA2
CPU B	ERAY0	TXD	P02.0	ERAY-A_B	ERAY0_TXDA
CPU B	ERAY0	TXDEN	P02.4	N.C	ERAY0_TXENA
CPU B	I/O	ERRN	P00.6	N.C	
CPU B	I/O	EN	P02.6	N.C	
CPU B	ERAY0	RXD	P02.3	ERAY-B_B	ERAY0_RXDB2
CPU B	ERAY0	TXD	P02.2	ERAY-B_B	ERAY0_TXDB
CPU B	ERAY0	TXDEN	P02.5	N.C	ERAY0_TXENB
CPU B	I/O	ERRN	P00.7	N.C	
CPU B	I/O	EN	P02.7	N.C	

2.9.2 LIN

There are 4 LIN connectors available on the 24V Automotive Gateway-V1.0, two of them connected on each CPU.

Table 10 shows the LIN signal connection list.

Table 10 LIN Signal List

CPU	Module	Signal	Pin	Header	Comment
CPU A	ASCLIN0	RXD	P15.3	LIN0_A	ASCLIN0_ARXB
CPU A	ASCLIN0	TXD	P15.2		ASCLIN0_ATX
CPU A	I/O	EN	P32.5		Zero Ohm R264 resistor (assembled)
CPU A	ASCLIN1	RXD	P15.5	LIN1_A	ASCLIN1_ARXB
CPU A	ASCLIN1	TXD	P15.4		ASCLIN1_ATX
CPU A	I/O	EN	P32.6		Zero Ohm R265 resistor (assembled)
CPU B	ASCLIN0	RXD	P33.10	LIN0_B	ASCLIN0_ARXD
CPU B	ASCLIN0	TXD	P33.9		ASCLIN0_ATX
CPU B	ASCLIN1	RXD	P15.5	LIN1_B	ASCLIN1_ARXB
CPU B	ASCLIN1	TXD	P15.4		ASCLIN1_ATX

2.9.3 PSI5-S

CPU A provides one PSI5-S channel to an elmos E521.41 4 Channel Multi-Mode PSI5 transceiver. This transceiver is compliant with PSI5 standard v1.3 and v2.1. More information can be found in the datasheet of the transceiver.

Table 11 shows the PSI5-S signal connection list.

Table 11 PSI5-S Signal List

CPU	Module	Signal	Pin	Comment
CPU A	PSI5-S	SCLK	P33.10	
CPU A	PSI5-S	SDI_RXD	P33.6	
CPU A	PSI5-S	SDO_TXD	P33.5	
CPU A	I/O	TRIG	P33.9	
CPU A	Reset	/NRES	/PORST	Reset input

2.10 Inter-processor communication – HSSL0/1

Table 9 shows the HSSL signal connection list.

Table 12 HSSL Signal List

CPU	Module	Pin	Signal	Pin	Module	CPU
CPU A	HSCT0	P20.0	SYCLK	P20.0	HSCT0	CPU B
CPU A	HSCT1	P21.0	TXB1-RXA1_N	P22.2	HSCT1	CPU B
CPU A	HSCT1	P21.1	TXB1-RXA1_P	P22.3	HSCT1	CPU B
CPU A	HSCT0	P21.4	TXA-RXB_N	P21.2	HSCT0	CPU B
CPU A	HSCT0	P21.5	TXA-RXB_P	P21.3	HSCT0	CPU B
CPU A	HSCT1	P22.2	TXA1-RXB1_N	P21.0	HSCT1	CPU B
CPU A	HSCT1	P22.3	TXA1-RXB1_P	P21.1	HSCT1	CPU B
CPU A	HSCT0	P21.2	TXB-RXA_N	P21.4	HSCT0	CPU B
CPU A	HSCT0	P21.3	TXB-RXA_P	P21.5	HSCT0	CPU B

2.11 SPI between CPU A and CPU B

In addition to the two HSSL high speed connections between CPU A and B there is a SPI channel.

Table 13 shows the SPI signal connection list.

Table 13 SPI Signal List

CPU	Module	Comment	Pin	Signal	Pin	Comment	Module	CPU
CPU A	QSPIO	MTSR	P22.10	QSPIO0_SDI	P15.6	MTSRB	QSPIO2	CPU B
CPU A	QSPIO	MRSTC	P22.6	QSPIO0_SDO	P15.7	MRST	QSPIO2	CPU B
CPU A	QSPIO	SCLK	P22.7	QSPIO0_CLK	P15.8	SCLKC	QSPIO2	CPU B
CPU A	QSPIO	SLS08	P20.6	QSPIO0_CS_1	P15.2	SLSIA	QSPIO2	CPU B

2.12 Solenoid Relay

The TLE92464ED is a flexible, monolithic solenoid driver IC designed for the control of linear solenoids in automatic transmissions, electronic stability control and active suspension applications. The device includes the drive transistors and the current sensing resistors to minimize the number of external components.

Table 13 shows the solenoid relay signal connection list.

Table 14 TLE92464 Signal List

CPU	Module	Signal	Pin	Comment
CPU A	I/O	EN	P33.3	
CPU A	I/O	DRV0	P34.1	
CPU A	I/O	DRV1	P34.2	
CPU A	I/O	DRV2	P34.4	
CPU A	I/O	DRV3	P34.5	
CPU A	I/O	FAULTN	P14.10	
CPU A	QSPI2	CSN	P34.3	SLSO10
CPU A	QSPI2	SCK	P15.8	
CPU A	QSPI2	SI	P15.6	
CPU A	QSPI2	SO	P15.7	
CPU A	Reset	/RESN	P10.2	Reset input

2.13 General Purpose LEDs

Each of the CPUs supports one own RGB LED and 4 general purpose LED connected to the pins listed in Table 15 and Table 16.

Table 15 LEDs CPU A

CPU	Module	Signal	Pin	Comment
CPUA		BLUE	P13.0	
CPUA		BLUE	P11.13	
CPUA		BLUE	P11.14	
CPUA		BLUE	P13.3	
CPUA		GREEN	P00.9	
CPUA		RED	P00.8	
CPUA		BLUE	P00.12	

Table 16 LEDs CPU B

CPU	Module	Signal	Pin	Comment
CPUB		BLUE	P14.6	
CPUB		BLUE	P14.8	
CPUB		BLUE	P13.0	

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CPUB		BLUE	P13.3	
CPUB		GREEN	P00.9	
CPUB		RED	P00.8	
CPUB		BLUE	P00.12	

2.14 Extension Header CPU B

The extension Header X1101 is a raspberry pi 3 like connector and is connected to CPU B. It allow to use extension Boards used on raspberry pi on that Board. The +5V of the Board will generate a +3,3V of a separate LDO. Both supply voltages are protected by diodes against reverse supply form the extension Board.

Table 17 Extension Header CPU

CPU	Module	Signal	Pin	Pin on Header
CPUB	PWR	+3V3_EXT		1
CPUB	PWR	+5V		2
CPUB	I2C	SDA	P11.13	3
CPUB	PWR	+5V		4
CPUB	I2C	SDC	P11.14	5
CPUB	GND	GND		6
CPUB	Bluetooth	BT_WAKE	P33.1	7
CPUB	Bluetooth	BLE_TXD	P32.5	8
CPUB	GND	GND		9
CPUB	Bluetooth	BLE_TXD	P32.5	10
CPUB	Bluetooth	BLE_RTS	P33.4	11
CPUB		PCM_CLK	P33.6	12
CPUB	WiFi	WIFI_SDIO_D3	P20.11	13
CPUB	GND	GND		14
CPUB	WiFi	WIFI_SDIO_SCLK	P15.1	15
CPUB	WiFi	WIFI_SDIO_CMD	P15.3	16
CPUB	PWR	+3V3_EXT		17
CPUB	WiFi	WIFI_SDIO_D0	P20.8	18
CPUB	SPI	SPI_MOSI	P10.3	19
CPUB	GND	GND		20
CPUB	SPI	SPI_MISO	P10.1	21
CPUB	WiFi	WIFI_SDIO_D1	P20.8	22
CPUB	SPI	SPI_CLK_B	P10.2	23
CPUB	SPI	SPI_C0	P10.4	24
CPUB	GND	GND		25
CPUB	SPI	SPI_C1	P11.10	26
CPUB	I2C	I2C_ID_Data	P13.2	27
CPUB	I2C	I2C_ID_CLK	P13.1	28
CPUB	Bluetooth	BLE_BT_RST_N	P32.7	29
CPUB	GND	GND		30
CPUB	WiFi	WIFI_WL_REG_ON	P20.12	31
CPUB	Timer	PWM	P33.7	32
CPUB	Bluetooth	BLE_HOST_WAKE	P33.2	33

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Hardware description



CPUB	GND	GND		34
CPUB		PCM_SYNCH	P32.2	35
CPUB	Bluetooth	BLE_CTS	P33.5	36
CPUB	WiFi	WIFI_SDIO_D2	P20.10	37
CPUB		PCM_OUT	P32.3	38
CPUB	GND	GND		39
CPUB		PCM_IN	P33.3	40

3 Software initialization sequence

The 24V Automotive Gateway-V1.0 does not need a special sequence to start-up. Both TC3xx will boot up. The Ethernet Switch is configured via the connected EEPROM, the GREFCLK for CPU A is generated automatically by clock generator so that the Ethernet networks boots up as well.

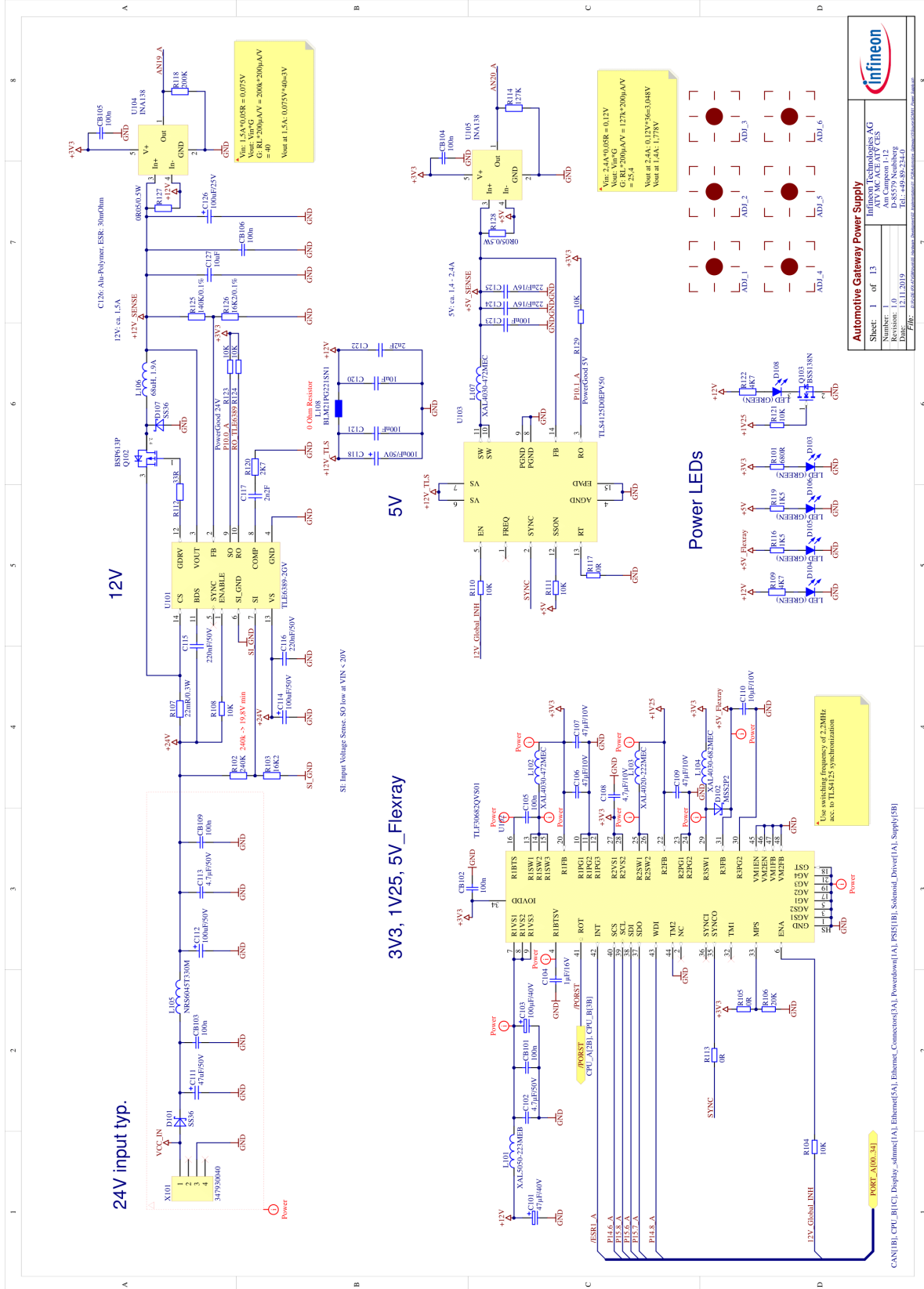
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Schematic and PCB



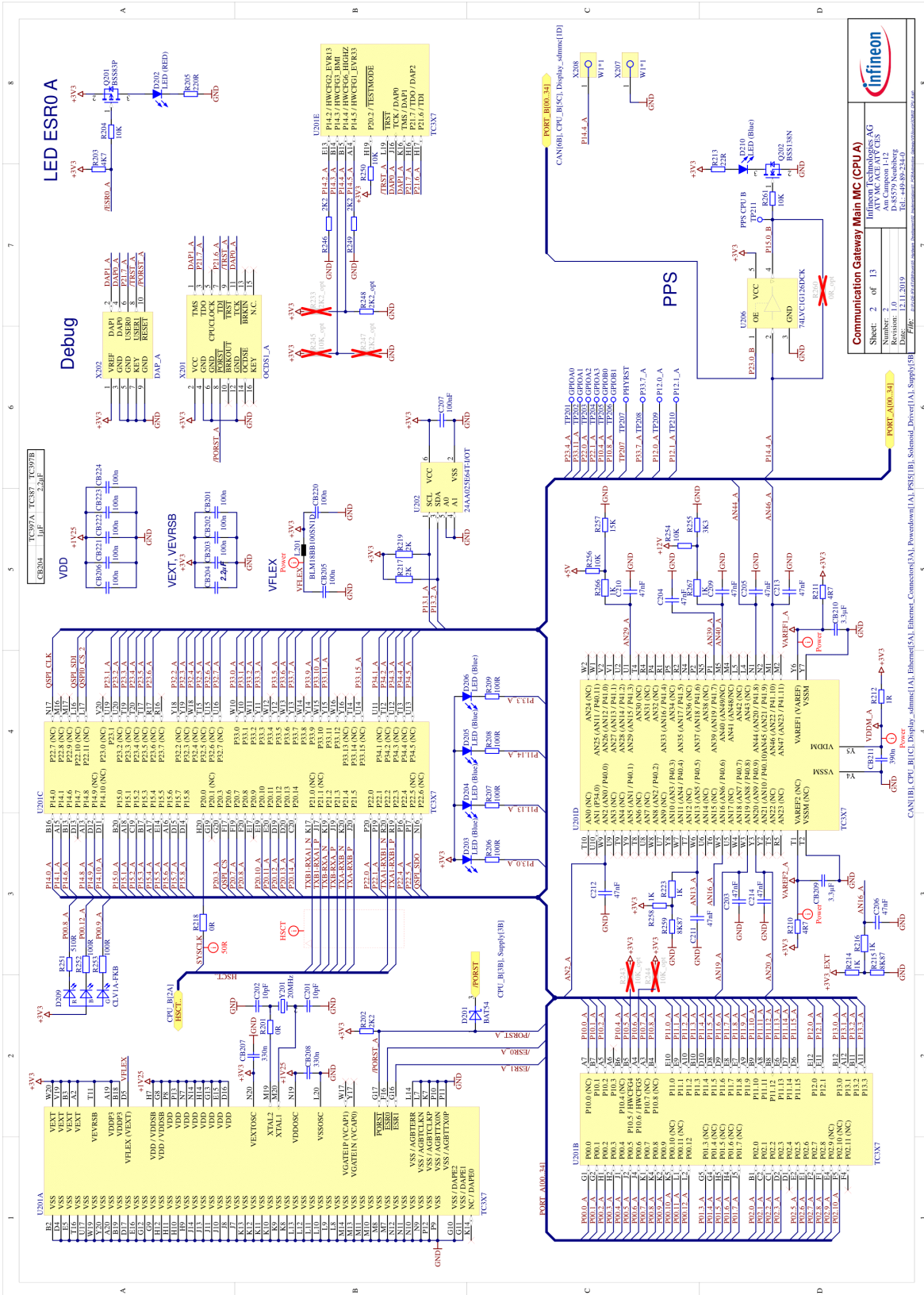
4 Schematic and PCB



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Schematic and PCB



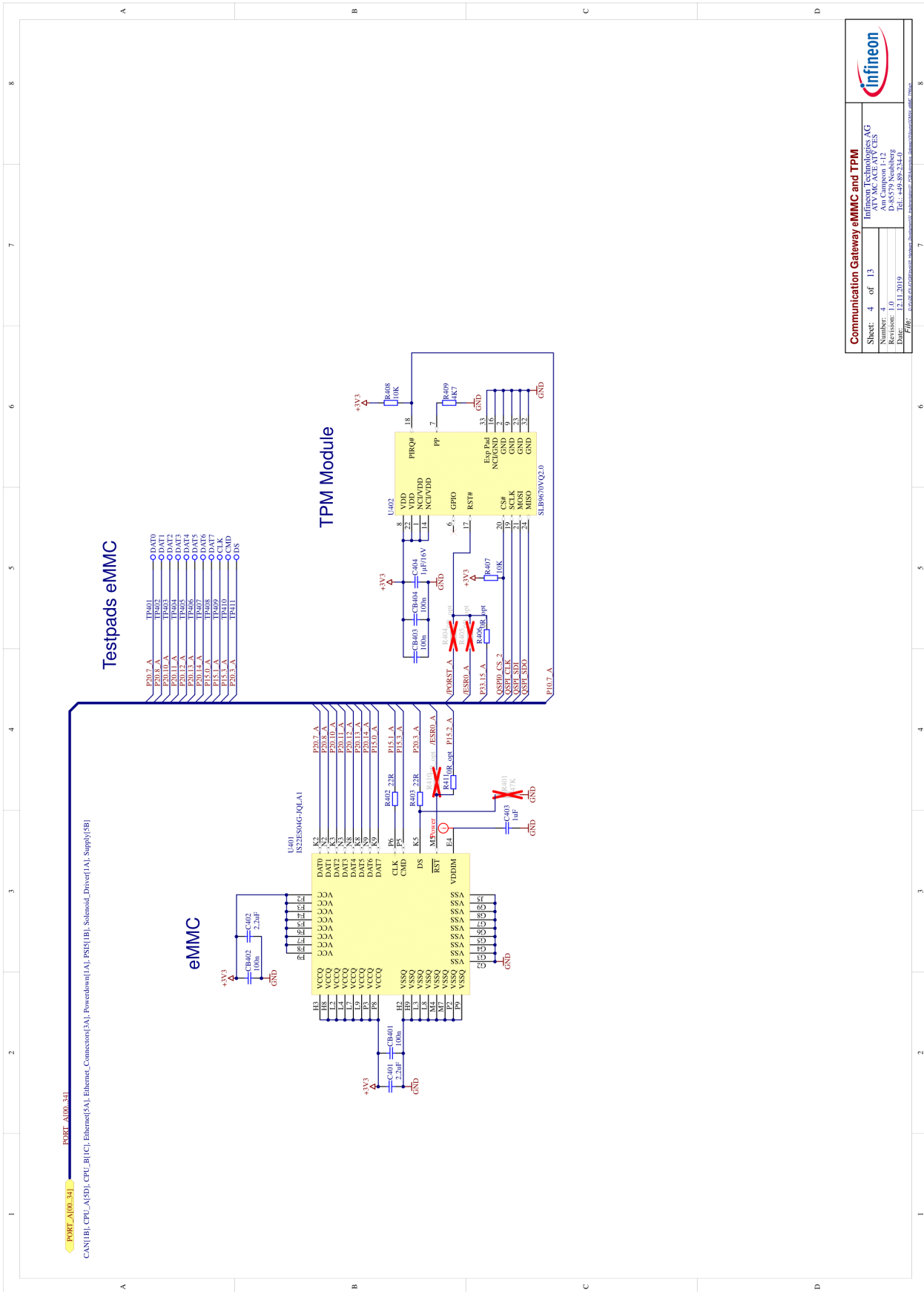
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 Number: 1.0
 Date: 12.11.2019
 File: 24V Automotive Gateway Main IC (CPUA) (Rev. 1.0) (13.11.2019).sch

24V Automotive Gateway-V1.0

For AURIX™ family

Schematic and PCB

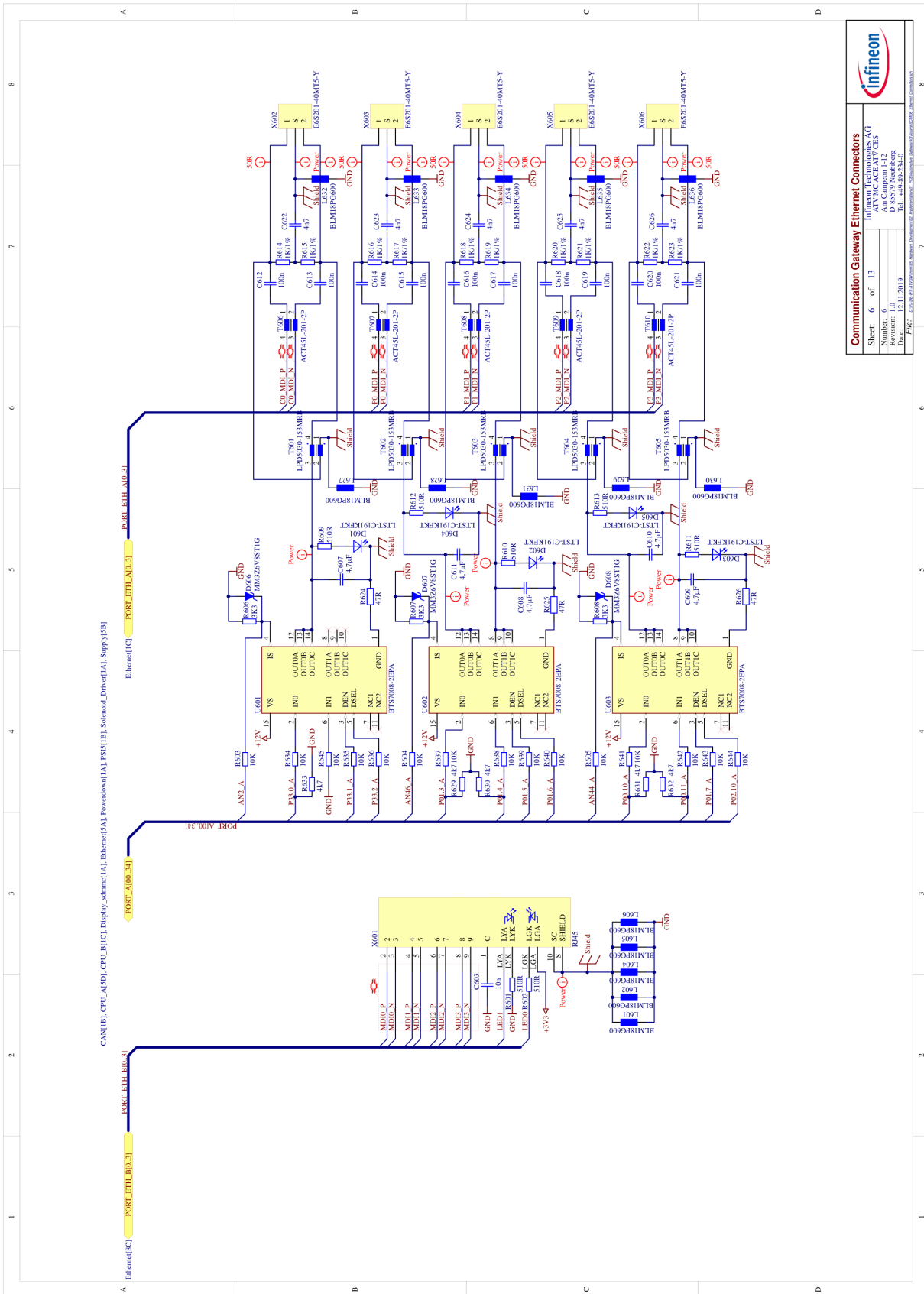


Infineon	
Communication Gateway eMMC and TPM	
Sheet: 4	of 13
Infineon Technologies AG Am Campeon 1-12 D-85579 Neuburg Tel.: +49-89-234-0	
Number: 4	Revision: 1.0
Date: 12.11.2019	

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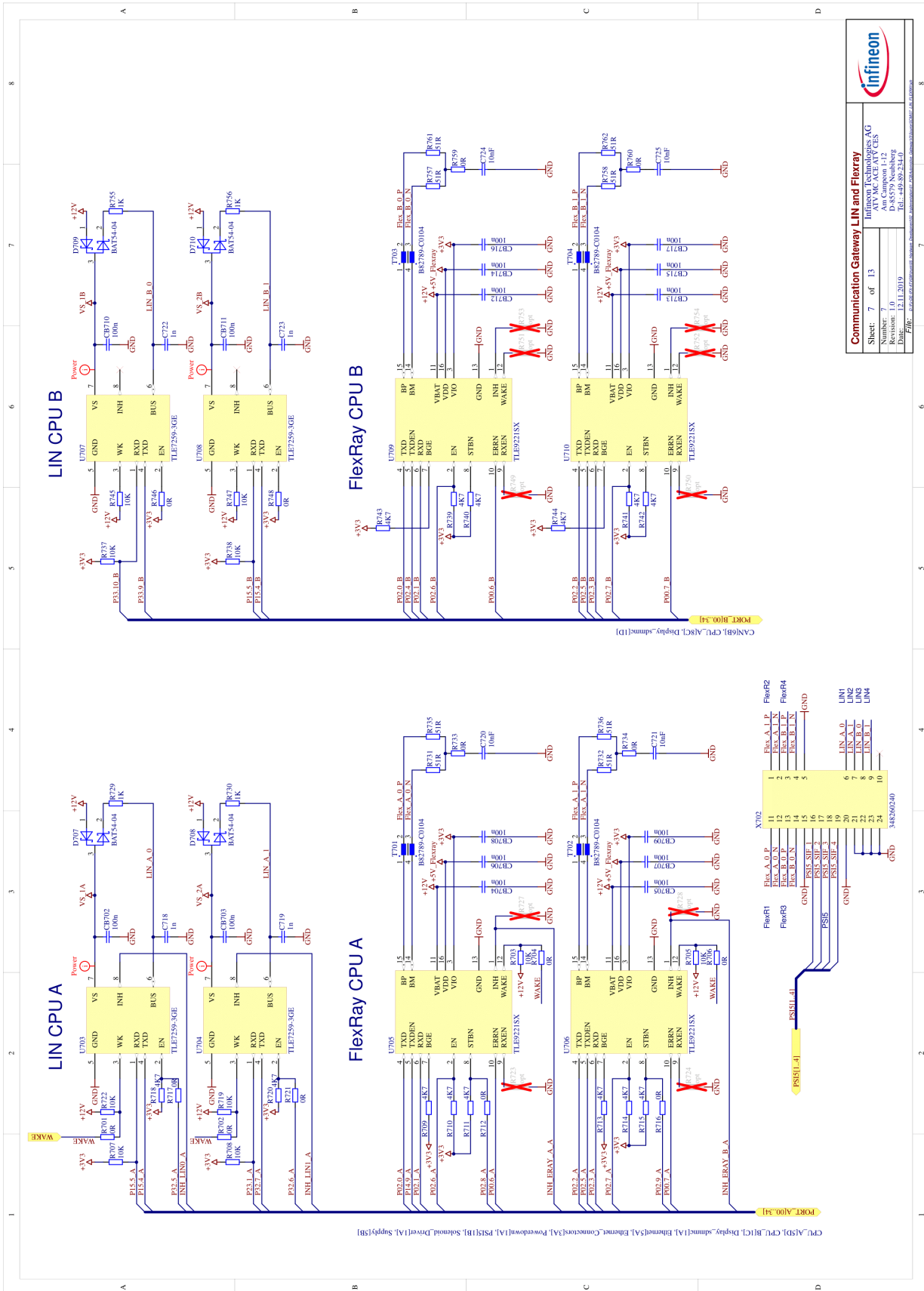


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Schematic and PCB



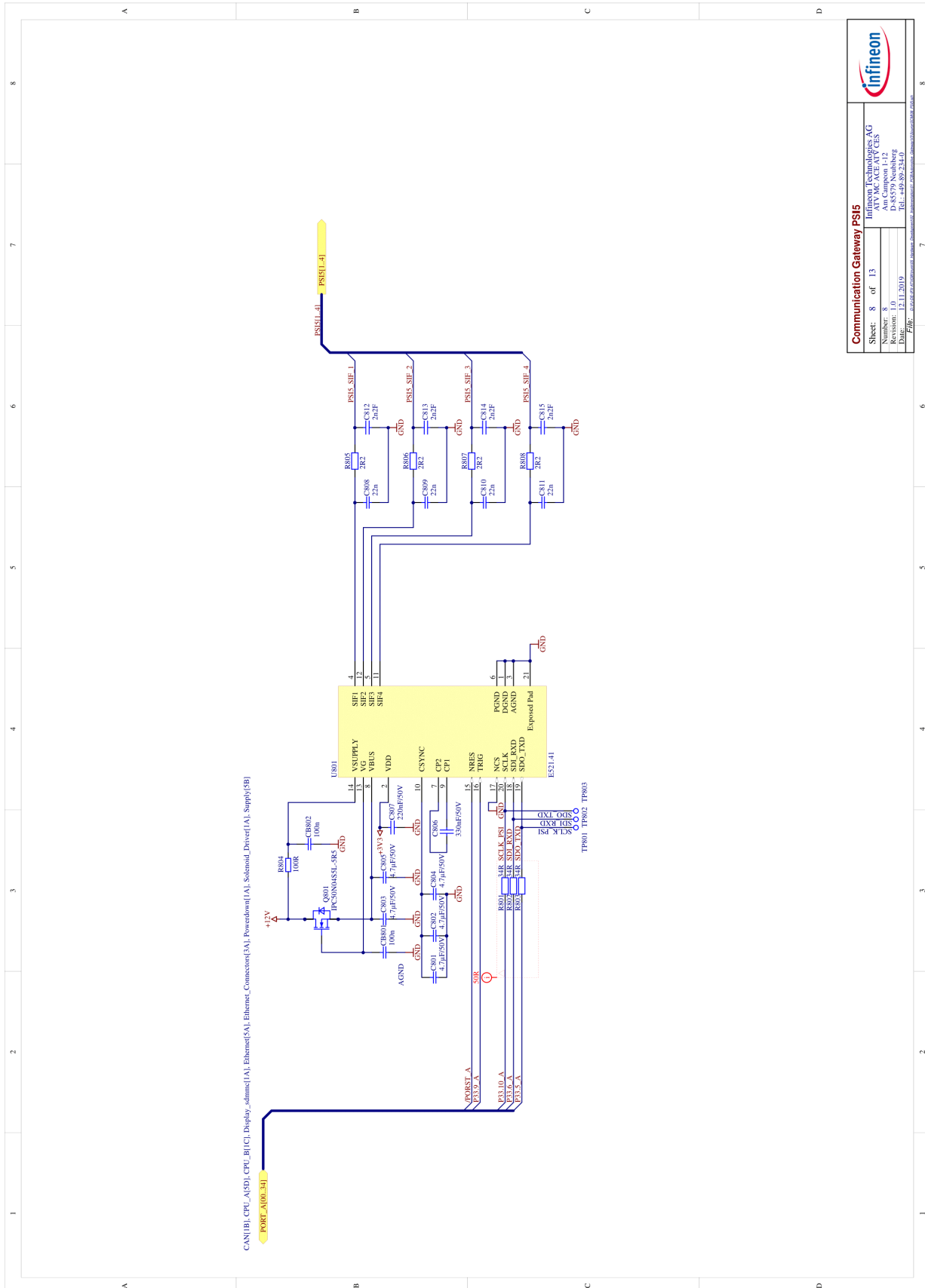
Communication Gateway LIN and Flexray

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 Revision: 1.0
 Number: 7 of 13
 Date: 2010-10-28
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24V Automotive Gateway-V1.0

For AURIX™ family

Schematic and PCB

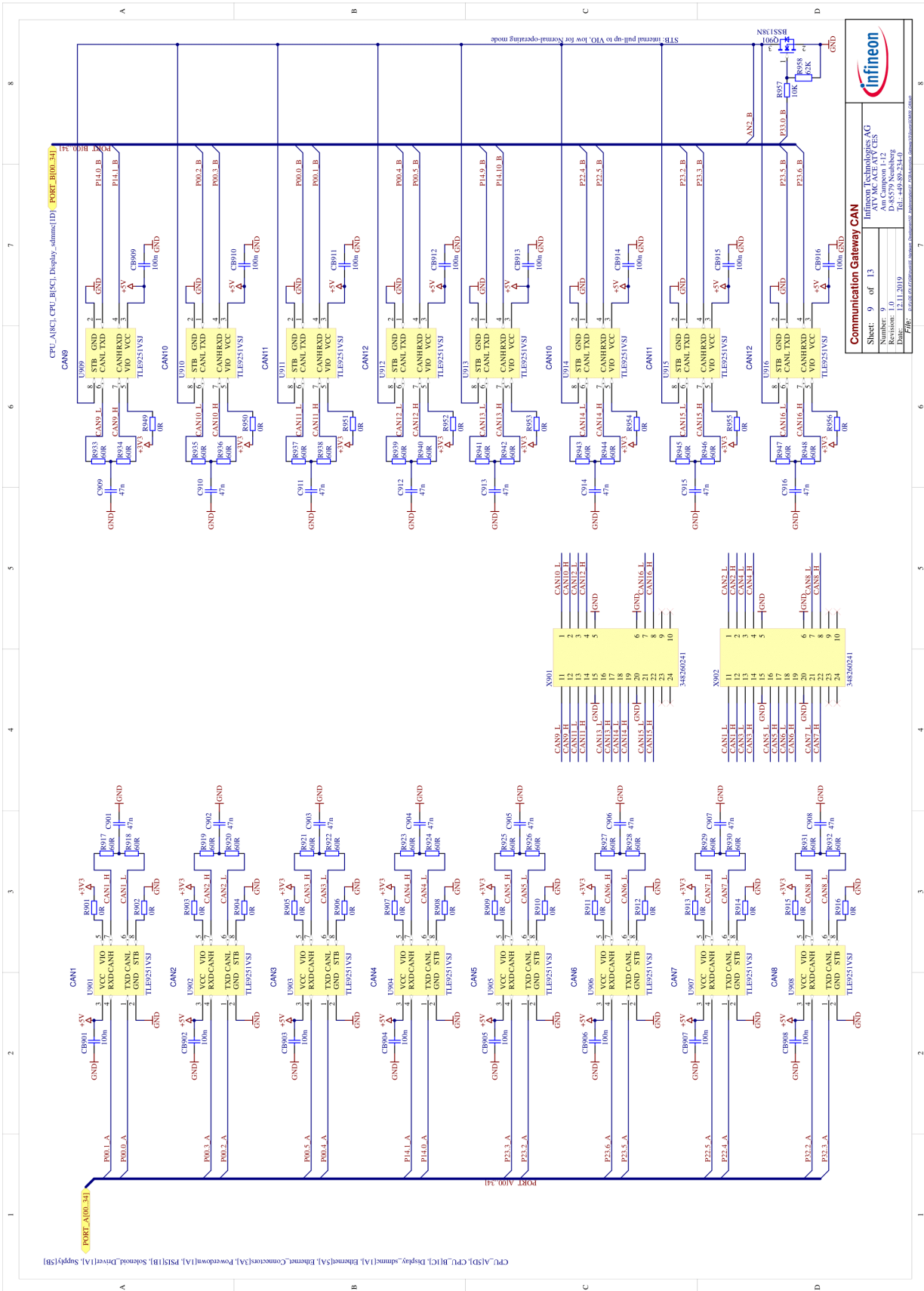


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Sheet: 8	of 13
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Fax: +49 924 724 24 10	
File: 24V_Auto_GW_V1.0_Schematic_PCB.dwg	

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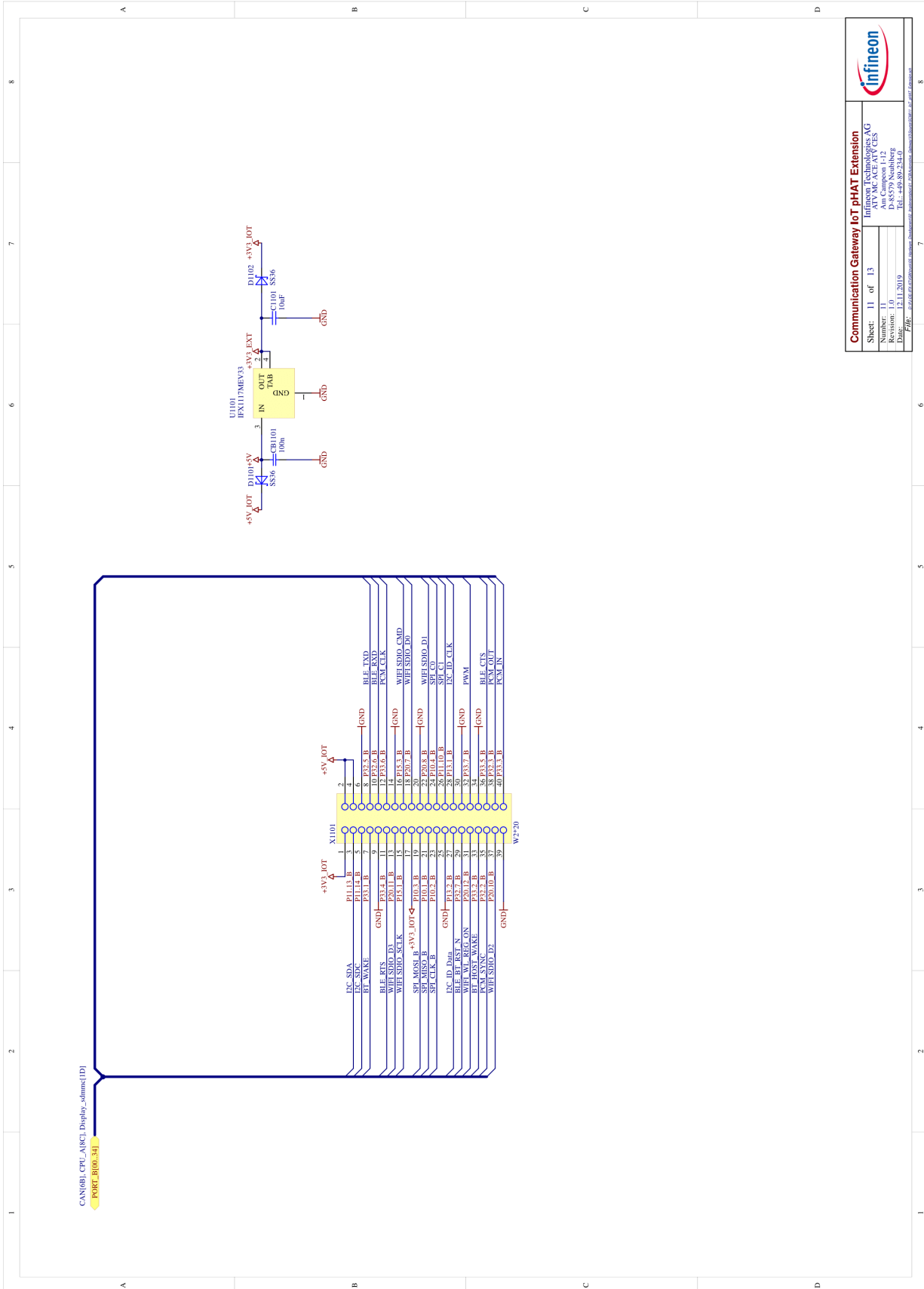
Sheet: 9 of 13
 Number: J1
 Revision: 1.0
 Date: 2010-10-28

Communication Gateway CAN

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Schematic and PCB



Communication Gateway IoT pHAT Extension

Sheet: 11 of 13
 Number: 11
 Revision: 1.0
 Date: 2019-10-28




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5 Appendix

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Molex Connector information

Power Supply	CAN	LIN / Flexray
<p>Molex Part Number: 347910040</p>  <p>Mini50 Unsealed Receptacle, Single Row, Non-Bridged, 4 Circuits, Polarization Option A, Black</p>	<p>Molex Part Number: 348240245</p>  <p>Mini50 Unsealed Receptacle, Dual Row, Non-Bridged, 24 Circuits, EcoPaXX Resin, Polarization Option B, Gray</p>	<p>Molex Part Number: 348240244</p>  <p>Mini50 Unsealed Receptacle, Dual Row, Non-Bridged, 24 Circuits, EcoPaXX Resin, Polarization Option A, Black</p>



Revision history

Major changes since the last revision

Page or reference	Description of change
All pages	First release.

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**Document reference
Manual**

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