Customer training workshop TRAVEO™ T2G audio subsystem

Q2 2023

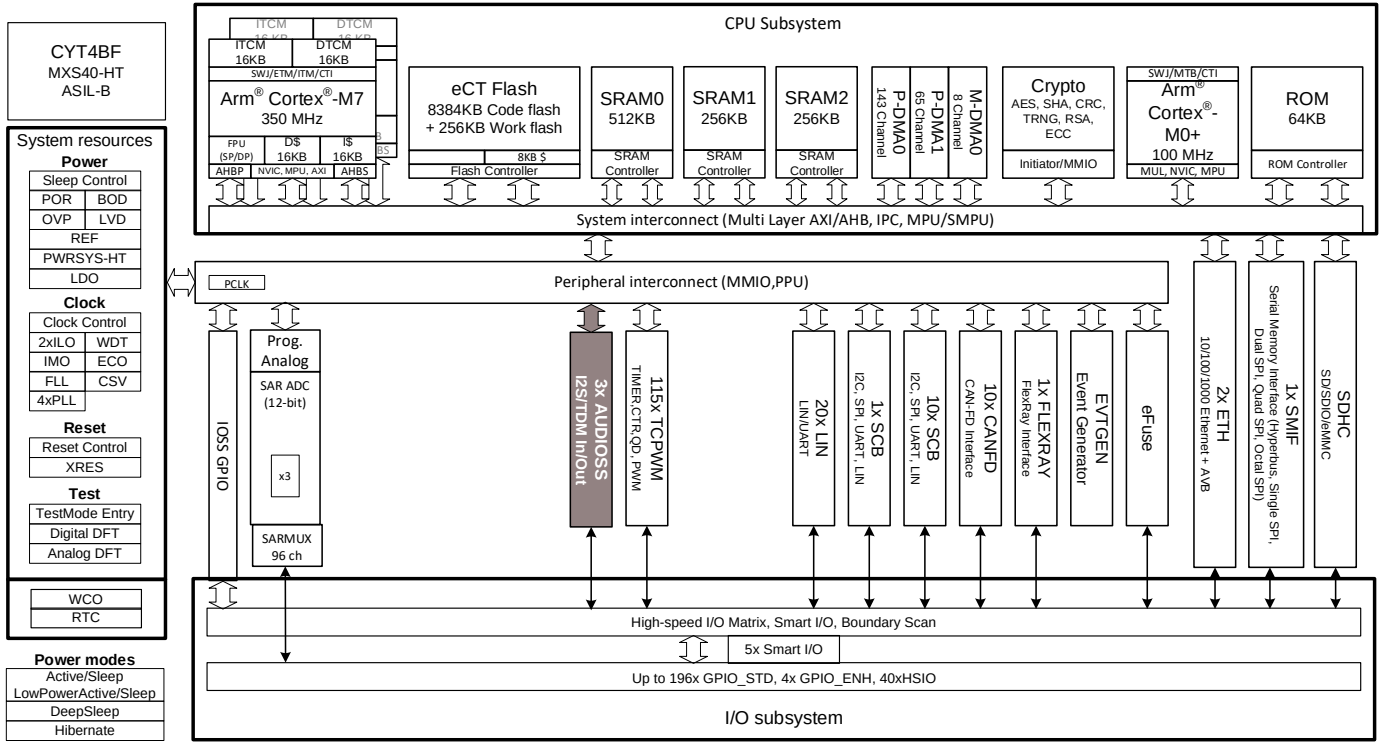
Target product

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
TRAVEO™ T2G Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
TRAVEO™ T2G Automotive Body Controller High	CYT4BF	Up to 8384KB

Introduction to TRAVEO™ T2G Body Controller High

› Audio subsystem is part of peripheral blocks



Hint Bar

Review TRM chapter 34 for additional details

Audio subsystem overview

- Audio subsystem supports:
  - Standard Inter-IC Sound Bus (I^2S) format
  - Left Justified (LJ) format
  - Time Division Multiplexed (TDM) format

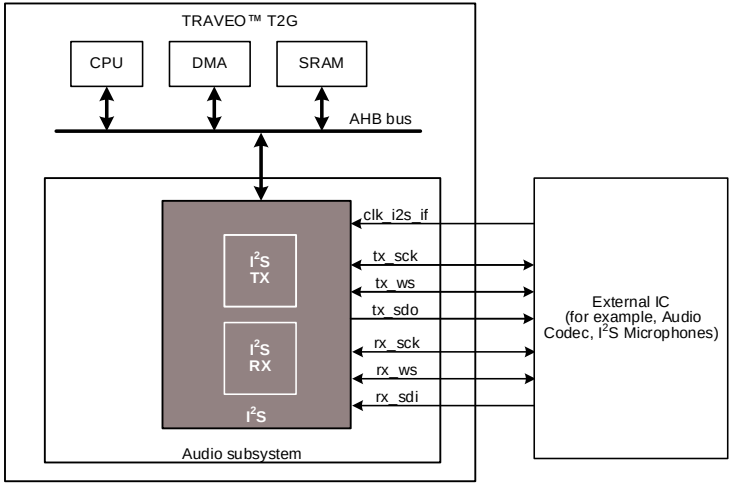
- Features
  - Master/Slave mode operation
  - Data word length of 8, 16, 18, 20, 24, and 32 bits per channel
  - Channel length of 8, 16, 18, 20, 24, and 32 bits per channel (channel length fixed at 32 bits in TDM format)
  - Clock divider for generating the standard audio sampling rates
  - Two hardware FIFO buffers
  - Watchdog timer

Hint Bar

Review TRM chapter 34 for additional details

Audio subsystem block diagram

- Audio subsystem components
  - I²S block (TX and RX)
    - Standard I²S format
    - Left justified (LJ) format
    - Time division multiplexed (TDM) format
    - Clocking polarity and delay options
    - Interfacing with audio codecs
    - Clock/Divider
    - MCLK output function
    - FIFO buffer
    - Watchdog timer
    - Interrupt



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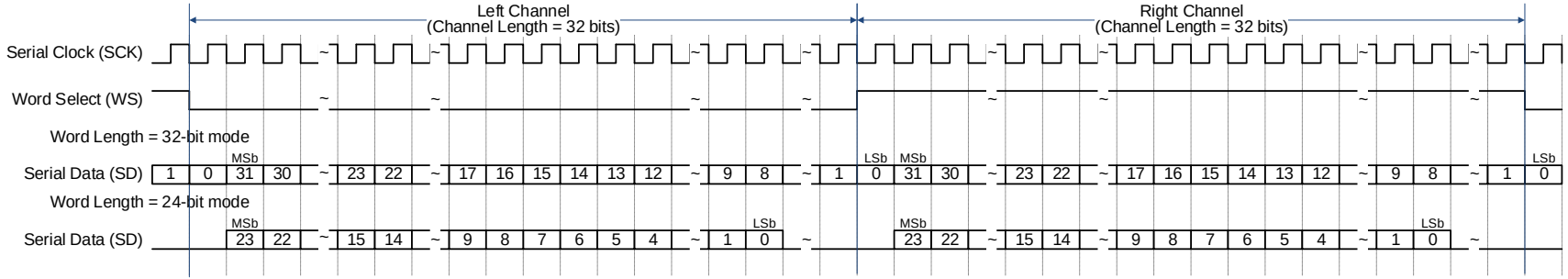
Review TRM section 34.2 for additional details

Standard I²S format

› Channel length = 32 bits (Word length = 32 bits and 24 bits)



› Word length and channel length combinations

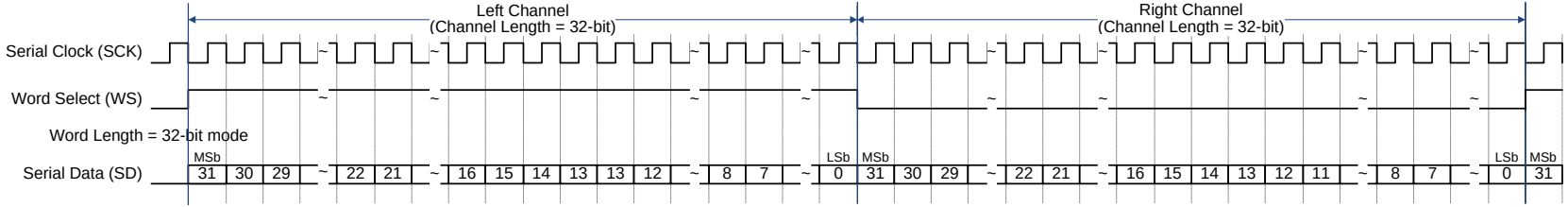
		Word Length					
		8-bit	16-bit	18-bit	20-bit	24-bit	32-bit
Channel Length	32-bit	Valid	Valid	Valid	Valid	Valid	Valid
	24-bit	Valid	Valid	Valid	Valid	Valid	Invalid
	20-bit	Valid	Valid	Valid	Valid	Invalid	Invalid
	18-bit	Valid	Valid	Valid	Invalid	Invalid	Invalid
	16-bit	Valid	Valid	Invalid	Invalid	Invalid	Invalid
	8-bit	Valid	Invalid	Invalid	Invalid	Invalid	Invalid

WS signal:

- LOW for left channel
- HIGH for right channel
- WS signal transitions a one-bit clock (SCK) early, relative to the start of the channel data (coincides with the LSb of the previous channel)

Left justified (LJ) format

- Channel length = 32 bits



WS signal:

- HIGH for left channel
- LOW for right channel
- WS signal transitions coincide with the start of the channel data

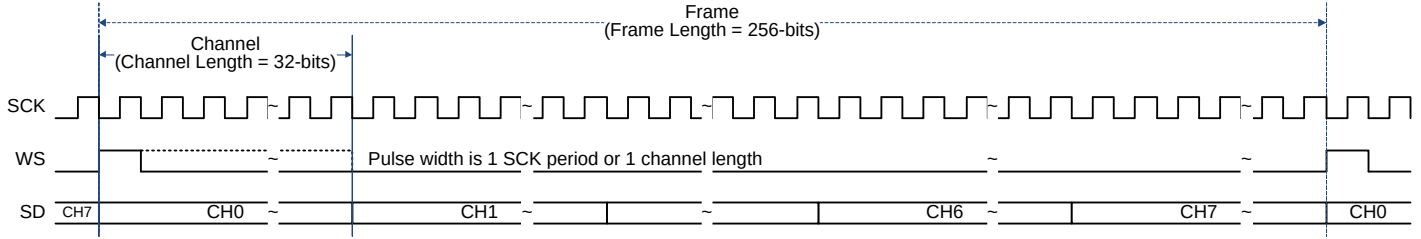
Time division multiplexed (TDM) format

- Up to eight channels per frame
- Channel length is fixed at 32 bits
- Two format types
  - TDM Mode A format
  - TDM Mode B format

Time division multiplexed (TDM) format types

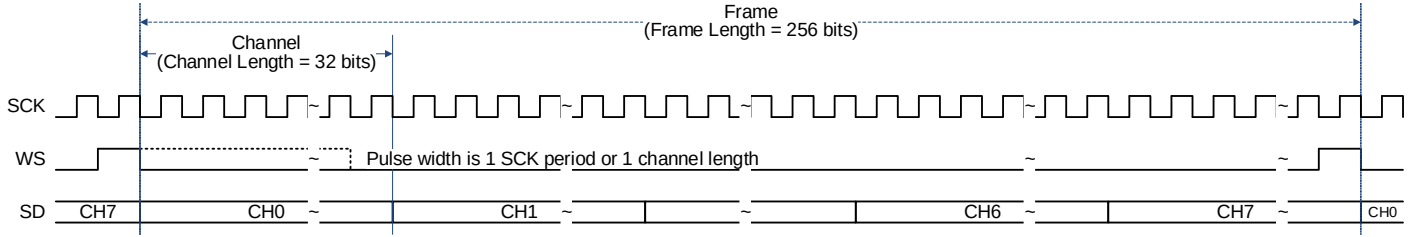
› TDM Mode A format:

WS rising edge signal to signify that the start of frame coincides with the start of CH0 data



› TDM Mode B format:

WS rising edge signal to signify that the start of frame is one-bit clock (SCK) early, relative to the start of CH0 data (coincides with the last bit of the previous frame)



Clocking polarity and delay options for TX block

- Alleviates any timing issues in the system involving PCB signal propagation delays
  - TX block configuration for Master mode

TX Block Configuration	Clock Polarity Register	Description
	I2S_TX_CTL.SCKO_POL	
(1)	0	Serial data is transmitted off the SCK falling edge
(2)	1	Serial data is transmitted off the SCK rising edge

  - TX block configuration for Slave mode

TX Block Configuration	Clock Polarity Register	Delay Option Register	Description
	I2S_TX_CTL.SCKI_POL	I2S_TX_CTL.B_CLOCK_INV	
(1)	0	0	Serial data is transmitted off SCK falling edge
(2)	0	1	Serial data is transmitted off SCK rising edge that is 0.5 SCK cycles before (1)
(3)	1	0	Serial data is transmitted off SCK rising edge
(4)	1	1	Serial data is transmitted off SCK falling edge that is 0.5 SCK cycles before (3)

Hint Bar

Review TRM section 34.4 and Register TRM for additional details

Clocking polarity and delay options for RX block

- Alleviates any timing issues in the system involving PCB signal propagation delays
  - RX block configuration for Master mode

RX Block Configuration	Clock Polarity Register	Delay Option Register	Description
	I2S_RX_CTL.SCKO_POL	I2S_RX_CTL.B_CLOCK_INV	
(1)	0	0	Serial data is captured by SCK rising edge
(2)	0	1	Serial data is captured by SCK falling edge that is 0.5 SCK cycles after (1)
(3)	1	0	Serial data is captured by SCK falling edge
(4)	1	1	Serial data is captured by SCK rising edge that is 0.5 SCK cycles after (3)

  - RX block configuration for Slave mode

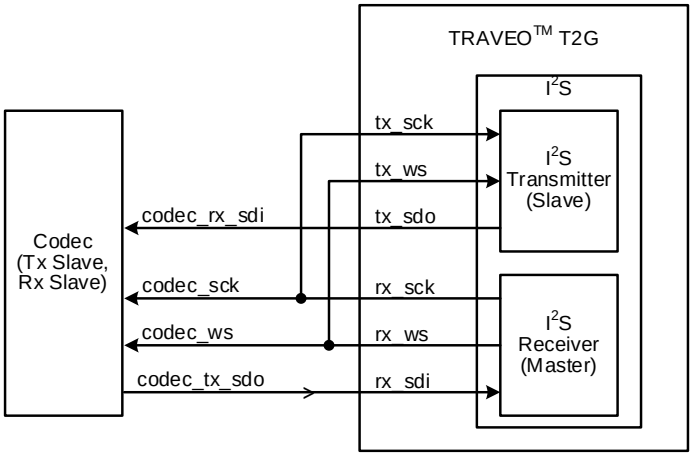
RX Block Configuration	Clock Polarity Register	Description
	I2S_RX_CTL.SCKI_POL	
(1)	0	Serial data is captured by SCK rising edge
(2)	1	Serial data is captured by SCK falling edge

Hint Bar

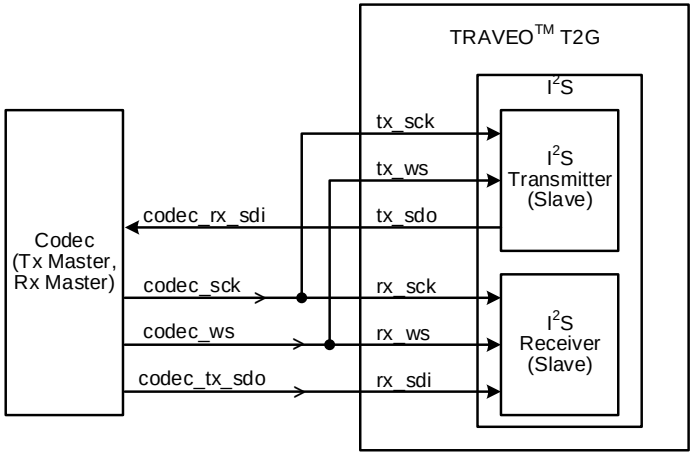
Review TRM section 34.4 and Register TRM for additional details

Interfacing with audio codecs

› Connections for codecs with separate WS and SCK signals for RX and TX directions



› Connections for codecs with common WS and SCK signals for RX and TX directions



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Review TRM section 34.5 for additional details

Clock

› The I²S unit has three clock inputs

Signal	Description
CLK_GRx[1]	System clock. This clock is used for the AHB slave interface, control, status, and interrupt registers, and also clocks the DMA trigger control logic.
CLK_HFx[2]	I²S internal clock. This clock is used for I²S TX/RX blocks; it is asynchronous with the CLK_GRx.
CLK_I2S_IF	I²S external clock. This clock is provided from an external I²S bus host through a port pin. It is used instead of CLK_HFx to synchronize I²S data to the clock used by the external I²S bus host.

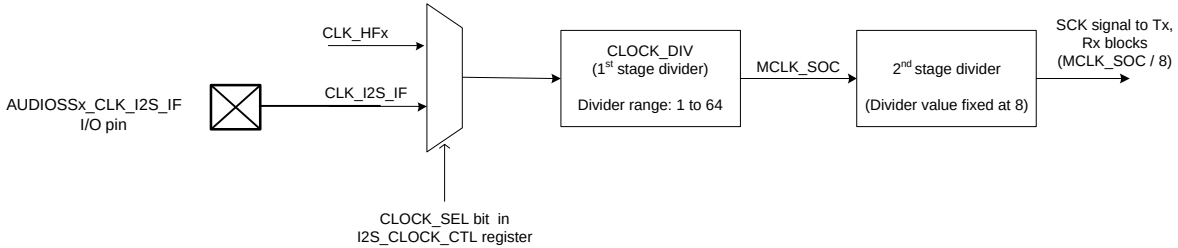
Hint Bar

Review TRM section 34.6 for additional details

[1] It is connected to CLK_GR8 in CYT4BF. For other devices, refer to the respective device datasheet.
[2] It is connected to CLK_HF5 in CYT4BF. For other devices, refer to the respective device datasheet.

Clock

- Clock divider
  - In Master mode, the SCK and WS signals are generated either using the internal CLK_HFx or external CLK_I2S_IF clocks
  - In Slave mode, the internal clock (MCLK_SOC) frequency should be eight times the frequency of the input SCK



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Review TRM section 34.6 and Register TRM for additional details

Example for I²S clock divider settings

› I²S clock divider values for standard audio sampling rates

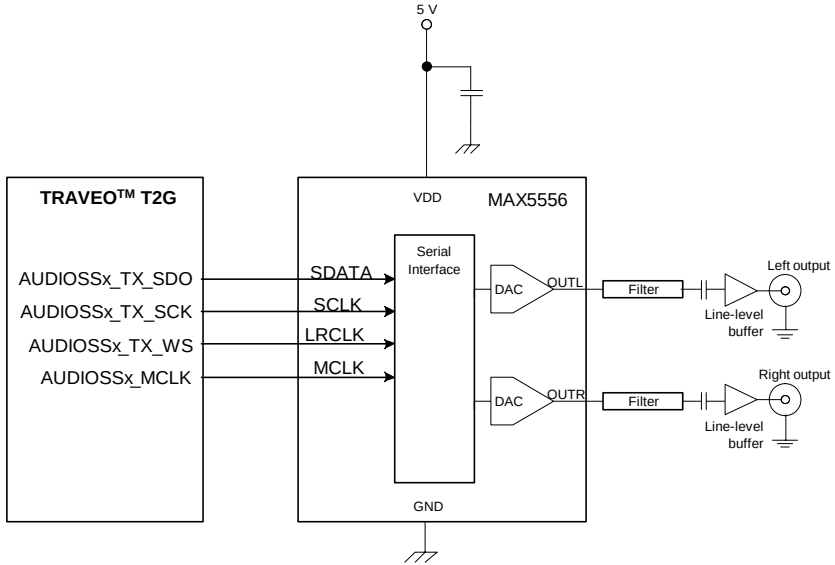
Sampling Rate (SR) [kHz]	WORD_LEN [bits]	SCK (2 x WORD_LEN x SR) [MHz]	CLK_HFx [MHz]	CLK_HFx/SCK (Total Divider Ratio)	CLK_CLOCK_DIV +1 (First Divider)	Second Stage Divider (Fixed at 8)
8	32	0.512	49.152	96	11	8
16	32	1.024	49.152	48	5	8
32	32	2.048	49.152	24	2	8
48	32	3.072	49.152	16	1	8
44.1	32	2.8224	45.1584	16	1	8

Hint Bar

Review TRM section 34.6 and Register TRM for additional details

MCLK output function

- The I²S unit generates an MCLK output signal for external codecs
  - The MCLK output signal is generated only when the following conditions are met:
    - CTL.TX_ENABLE or RX_ENABLE = 1 (I²S is enabled)
    - CLOCK_CTL.CLOCK_SEL = 0 (I²S clock is from internal clock: CLK_HFx)
    - CLOCK_CTL.MCLK_DIV = 0, 1, 2, or 3 (Division ratio: 1, 2, 4, or 8)
    - CLOCK_CTL.MCLK_EN = 1 (MCLK output enabled)



FIFO buffer

› The I²S block has two FIFO buffers – one each for TX and RX, respectively

Feature	TX FIFO	RX FIFO
Architecture	256 depth FIFOs for up to 32-bit data elements	
Data register	I2S_TX_FIFO_WR	I2S_RX_FIFO_RD
Data format	Right-aligned	Right-aligned Receive data is extended by zeros or the sign-bit
Trigger control register for DMA	I2S_TR_CTL.TX_REQ_EN	I2S_TR_CTL.RX_REQ_EN
Trigger level	When the TX FIFO has less entries than I2S_TX_CTL.TRIGGER_LEVEL, a transmitter trigger event is generated	When the RX FIFO has more entries than I2S_RX_CTL.TRIGGER_LEVEL, a receiver trigger event is generated

I2S_RX_CTL.BIT_EXTENSION = 0

Extended by “0”

I2S_RX_FIFO_RD register format for 24-bit word length

	read data format of I2S_RX_FIFO																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									MSb																						LSb
Word Length = 24-bit mode not Bit extension	fixed "0"								23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit extension	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

I2S_RX_CTL.BIT_EXTENSION = 1

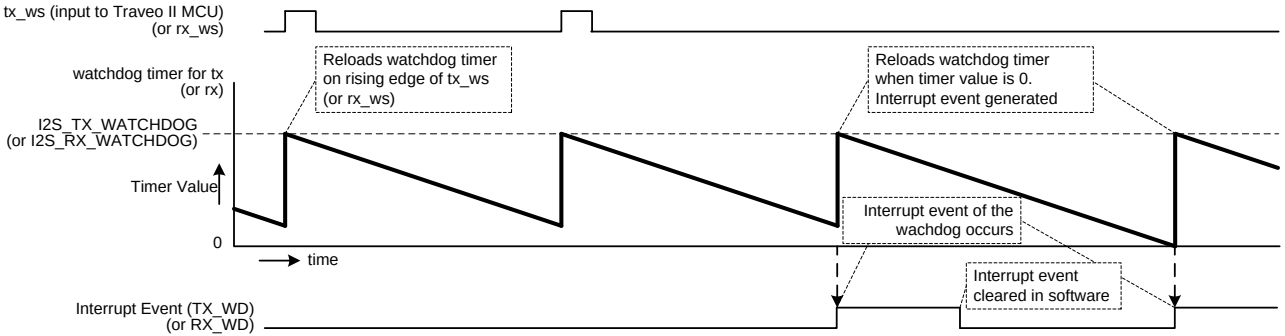
Extended by sign bit (if MSb is ‘1’, then it is extended by ‘1’; if MSb is ‘0’ then it is extended by ‘0’)

Hint Bar

Review TRM section 34.7 and Register TRM for additional details

Watchdog timer

- TX and RX blocks have independent watchdog timers
  - Clocked by CLK_PERI and generates an interrupt if the WS input is idle for more than the configured time period
  - Available only in slave mode - external master drives WS input line (tx_ws or rx_ws)[1]



- Advantage
  - Can be used to detect signal transmission issues, master device issues, or if the master has halted communication

Hint Bar

Review TRM section 34.9 and Register TRM for additional details

Watchdog Timer Reload Value Register

- I2S_TX_WATCHDOG

- I2S_RX_WATCHDOG

Watchdog Timer Enable Register

- I2S_TX_CTL.WD_EN

- I2S_RX_CTL.WD_EN

[1] If the master drives the same word select signal to both tx_ws and rx_ws lines, then only one of the watchdog timers can be enabled to cause the interrupt event.

Interrupt

- An I²S interrupt can be triggered by any of the following events

TX interrupt	Set condition
TX_TRIGGER	Less entries in TX FIFO than I2S_TX_CTL.TRIGGER_LEVEL
TX_NOT_FULL	TX FIFO is not full
TX_EMPTY	TX FIFO is empty
TX_OVERFLOW	Attempt to write to a full TX FIFO
TX_UNDERFLOW	Attempt to read from an empty TX FIFO
TX_WD	TX watchdog event occurs

RX interrupt	Set condition
RX_TRIGGER	More entries in RX FIFO than I2S_RX_CTL.TRIGGER_LEVEL
RX_NOT_EMPTY	RX FIFO is not empty
RX_FULL	RX FIFO is full
RX_OVERFLOW	Attempt to write to a full RX FIFO
RX_UNDERFLOW	Attempt to read from an empty RX FIFO
RX_WD	RX watchdog event occurs

Hint Bar

Review TRM section 34.8 and Register TRM for additional details

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Revision History

Revision	ECN	Submission date	Description of change
**	6396260	11/28/2018	Initial release
*A	6596897	06/17/2019	Added note descriptions in all pages Updated page 3, 6, 7, 8, 12, 13, 14
*B	7034551	10/28/2020	Updated page 2, 3
*C	7400288	10/14/2021	Updated page 1 to 5, 12, 16
*D	7882305	03/16/2023	Updated page 15