CCU6_PWM_Generation_1 for KIT_AURIX_TC297_TFT

Generation of PWM via CCU6

AURIX™ TC2xx Microcontroller Training
V1.0.1

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Scope of work

Three center aligned Pulse Width Modulated (PWM) signals with fixed frequency and different duty cycles are generated using CCU6.

The code example uses the Timer T12 of CCU6 and its three compare modules to generate three PWM signals with a frequency of 20 kHz and different duty cycles (25%, 50% and 75%). T12 is configured to count up and down and the three signals are center aligned.
The generated PWM signals are sent to the pins available on the board and can be observed with an oscilloscope.

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Introduction

- The Capture/Compare Unit 6 (CCU6) is a 16-bit capture and compare unit specially designed for motor control purposes.
- CCU6 contains multiple timer modules. Their count values are compared with reference values in order to generate PWM signals.
- Timer 12 (T12) is provided with three comparators. By synchronizing them, up to three synchronized PWM signals can be generated. These signals can be center aligned or edge aligned.

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Hardware setup

This code example has been developed for the board KIT_AURIX_TC297_TFT_BC-Step. Three oscilloscope probes are needed to observe the generated PWM signals. These need to be connected to the three output port pins.

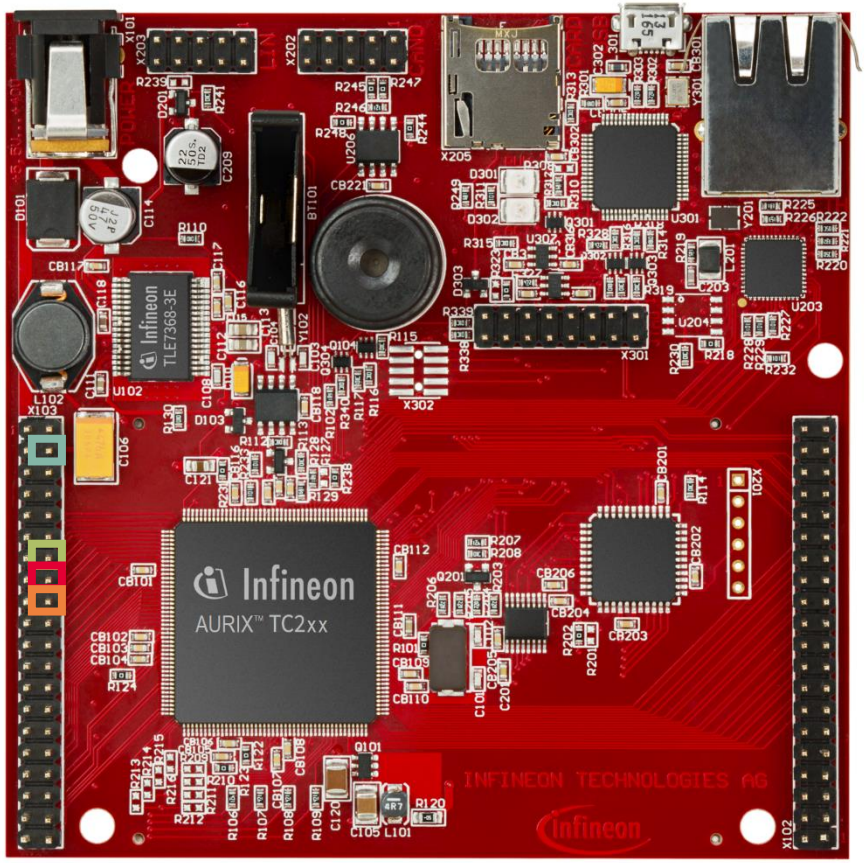
	X103		
VCC_IN	1	2	V_UC(+5V)
GND	3	4	GND
P33.10	5	6	P33.9
P14.8	7	8	P14.7
P14.6	9	10	P10.6
P10.7	11	12	P10.4
P02.0	13	14	P02.1
P02.2	15	16	P02.3
P02.4	17	18	P02.5
P02.6	19	20	P02.7
P02.8	21	22	P00.0
P00.1	23	24	P00.2
P00.3	25	26	P00.4
P00.5	27	28	P00.6
P00.7	29	30	P00.8
P00.9	31	32	P00.10
P00.11	33	34	P00.12
AN45	35	36	AN44
AN17	37	38	AN16
AN25	39	40	AN24

Ground

Channel 1

Channel 2

Channel 3



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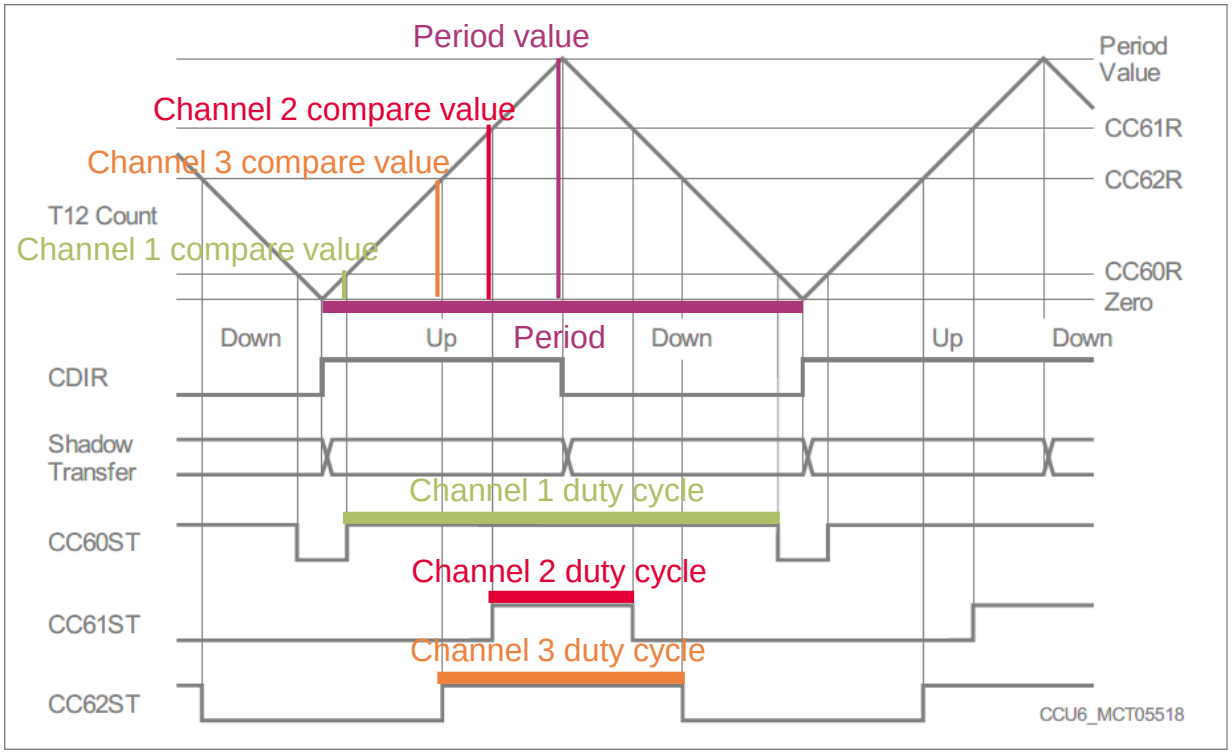
Implementation

Duty cycle and period

In this example, center-aligned PWM signals are generated. Therefore, the timer must be configured to count up and down, as shown in the figure below.



- Compare values are in **inverse relation** to the duty cycle values
- When compare value is equal to zero, the duty cycle is equal to 100%
- When compare value is equal to the period, the duty cycle is equal to 0%

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Implementation

Disabling and enabling global interrupts

Interrupts should be **temporarily disabled** during the initialization phase using the function ***IfxCpu_disableInterrupts()***. This is needed in order to avoid preemption caused by peripherals which have not been configured yet.

Interrupts are then **re-enabled** using the function ***IfxCpu_restoreInterrupts()*** at the end of the initialization phase, which also restores the initial state of the interrupts.

The above functions are provided by the iLLD header ***IfxCpu.h***.

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Implementation

Configuring the CCU6

To properly configure the CCU6 module for generating PWM signals with the iLLDs, a timer and the PWM High/Low driver need to be configured.

The functions and structures used to configure the timer and the driver can be found in the iLLD header ***IfxCcu6_PwmHl.h***.

Configuring the Timer

To properly configure the timer to generate PWM signals, an instance of the structure ***IfxCcu6_TimerWithTrigger_Config*** is created.

Firstly, default values are assigned to the timer configuration via the function ***IfxCcu6_TimerWithTrigger_initConfig()***.
Out of this structure, the following parameters are changed:

- the frequency of the PWM signals, which needs to be set to the desired value
- the timer count mode, which must be set to ***IfxStdIf_Timer_CountDir_upAndDown*** in order to enable the generation of center-aligned PWM signals

To apply the configuration, the function ***IfxCcu6_TimerWithTrigger_init()*** is finally used.

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Implementation

Configuring the PWM High/Low driver

In the driver configuration the output pins and the duty cycles are set. Furthermore, the compare modules of the three channels are configured.

To configure the driver, an instance of the structure ***IfxCcu6_PwmHl_Config*** is first initialized with default values using the function ***IfxCcu6_PwmHl_initConfig()***. The previously configured timer is then assigned to it, together with the desired output pins.

Since the PwmHl library supports the use of multiple compare channels, it is also necessary to specify the number of used channels (***config.base.channelCount = 3***).

The user configuration is applied with the function ***IfxCcu6_PwmHl_init()*** and the alignment mode of the generated PWM signals is then set with the function ***IfxCcu6_PwmHl_setMode()***, passing the parameter ***Ifx_Pwm_Mode_centerAligned***.

It is important to execute the last two instructions in the right order, because the function ***IfxCcu6_PwmHl_init()*** always resets the mode to the default value.

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Implementation

Configuring the PWM High/Low driver

The compare values for the three channels responsible for generating the desired duty cycles need to be calculated and passed as an array of the type ***Ifx_TimerValue*** to the ***IfxCcu6_PwmHl*** driver using the function ***update()***.

This last function updates only the internal state of the driver, but not the timer. For this reason, it is necessary to update the timer manually with the function ***IfxCcu6_TimerWithTrigger_applyUpdate()***, which enables the transfer of the compare values to the three channels.

Finally, the timer and the generation of the PWM signals can be started using the function ***IfxCcu6_TimerWithTrigger_run()***.

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Implementation

Duty cycle calculation example

Target: Find the correct compare value V_{cmp} to produce a PWM signal with period P = 50 microseconds and 25% duty cycle.

- CCU6 module base frequency F_{CC6} = 100 MHz
- Desired PWM period T = 50 microseconds which corresponds to a frequency of F_{PWM} = 20 kHz
- The period duration in ticks is P = F_{CC6} / F_{PWM} = 100 MHz / 20 kHz = 5000 ticks. This is the number of ticks that the timer has to count to produce the desired period.
- The desired duty-cycle is 25% of the period, which corresponds to 1250 ticks.
- The duty-cycle is **inversely proportional** to the relative **compare value** as explained in the previous slide. Therefore, the compare value can be found with:

$$V_{cmp} = P - \text{dutycycle} = 5000 - 1250 = \mathbf{3750}$$

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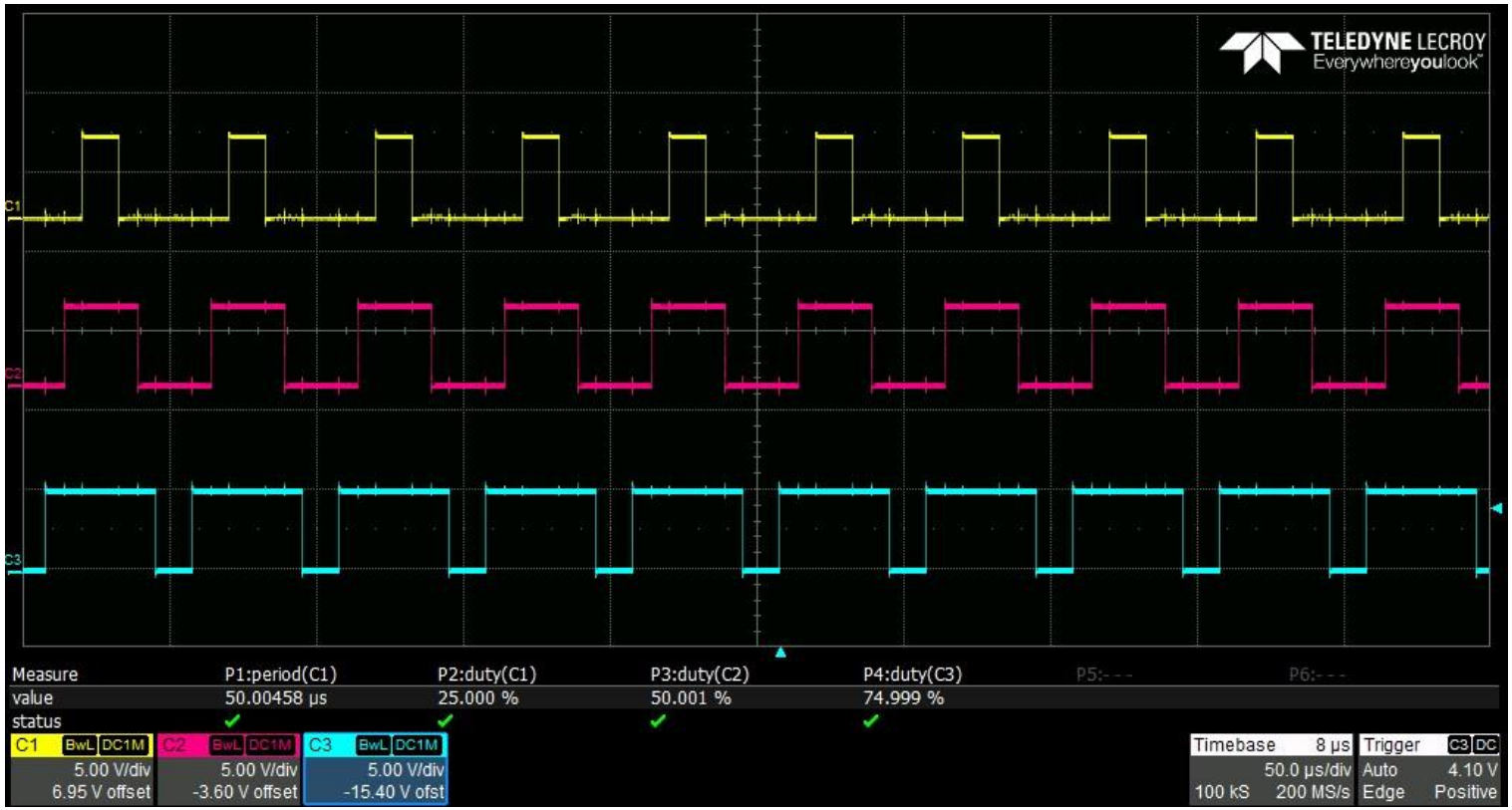
Run and Test

After code compilation and flashing the device, observe the oscilloscope screen.
Three center-aligned PWM signals can be observed, with the configured duty cycles and a period of 50 us each.



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References

- AURIX™ Development Studio is available online:
- https://www.infineon.com/aurixdevelopmentstudio
- Use the *„Import...“* function to get access to more code examples.

- More code examples can be found on the GIT repository:
- https://github.com/Infineon/AURIX_code_examples

- For additional trainings, visit our webpage:
- https://www.infineon.com/aurix-expert-training

- For questions and support, use the AURIX™ Forum:
- https://www.infineonforums.com/forums/13-Aurix-Forum

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Revision history

Revision	Description of change
V1.0.1	Update of version to be in line with the code example’s version
V1.0.0	Initial version

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